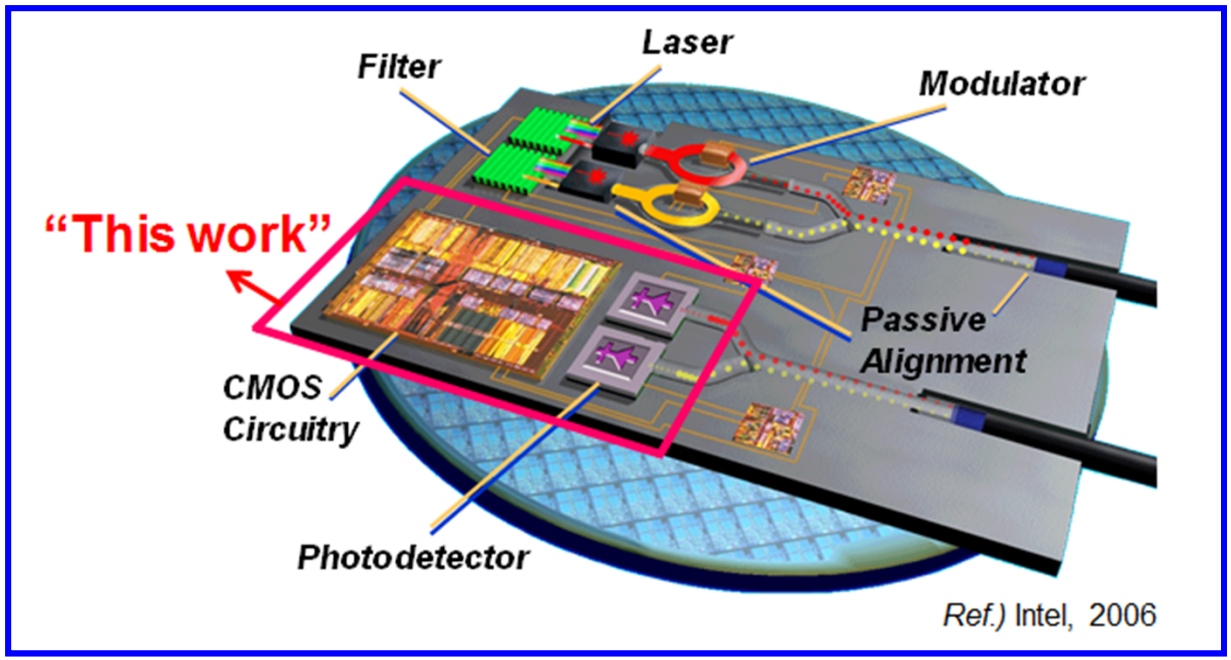
# CMOS / BiCMOS Optoelectronic Receiver

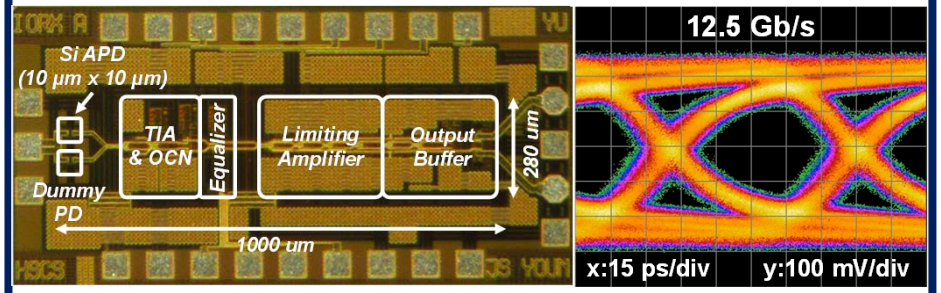
- Si Optoelectronic Receiver for Optical Interconnect Applications
  - **High-speed** optoelectronic receiver with signal-to-noise ratio (SNR) analysis
  - **Low-power** optoelectronic receiver with adaptive equalizer




- Chip Fabrication
  - IHP 0.25-μm SiGe:C BiCMOS technology
  - SAMSUNG 65nm CMOS technology (IDEC MPW 104$^{th}$, 117$^{th}$)

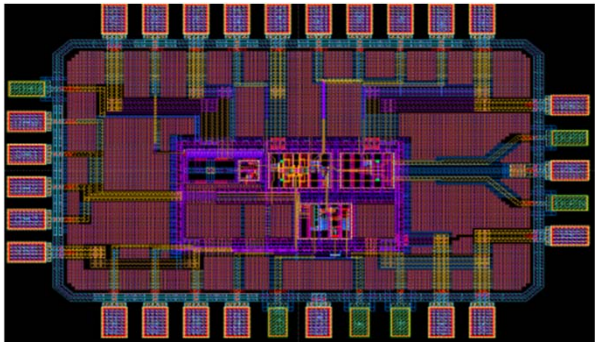
# CMOS / BiCMOS Optoelectronic Receiver

## High-Speed Optoelectronic Rx




- IHP SiGe BiCMOS 250nm
- Chip out: 2011.8
- Transimpedance amp., equalizer, limiting amp.
- 12.5-Gb/s optical data transmission with BER less than $10^{-12}$ at incident optical power of -7 dBm.

## Low-Power Optoelectronic Rx



- Samsung CMOS 65nm (IDEC MPW 117th)
- Chip out: 2013.6 (expectation)
- Transimpedance amp., equalizer, limiting amp., and adaptation block

❖ **International Journal**

- 10-Gb/s 850nm CMOS OEIC receiver with a silicon avalanche photodetector (*Journal of Quantum Electronics*, Feb., 2012)
- An integrated 12.5-Gb/s optoelectronic receiver with a silicon avalanche photodetector in standard SiGe BiCMOS technology (*Optics Express*, Dec., 2012)

❖ **International Conference**

- A 12.5-Gb/s SiGe BiCMOS optical receiver with a monolithically integrated 850-nm avalanche photodetector (*OFC/NFOEC*, Los Angeles, USA, Mar., 2012)
- Bit-error rate analysis of integrated optoelectronic receiver (*Photonics Global Conference*, Singapore, Dec., 2012)