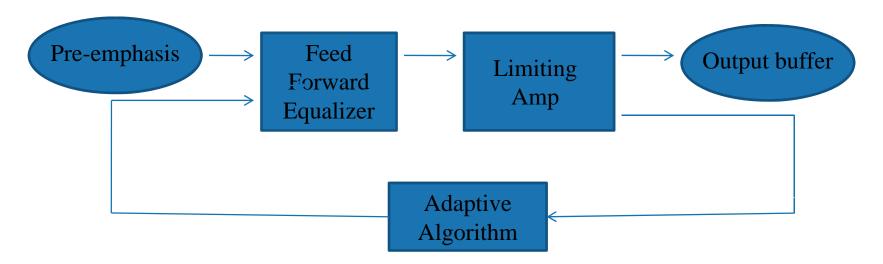


- Topic
 - Development of SerDes IP based on 65nm CMOS
- ✤Team member
 - Team member: K.C Choi, C.K Seong, Y.S Park and W.S Kim
 - CDR (Clock and Data Recovery) part: K.C Choi
 - PLL (Phase-Locked Loops) part: Y.S Park
 - Equalizer part: C.K Seong and W.S Kim
- Sponsor
 - Samsung Electronics



✤ 2.7Gb/s Adaptive Feed forward Equalizer

✤ Basic Structure



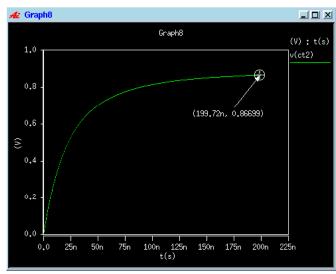
Adaptive Equalizer

0

✤ Eye diagram

•0 •

YONSEI UNIVERSITY



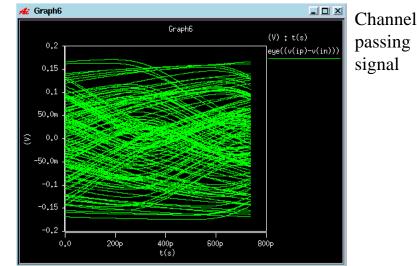
Craph7
Graph7
(V) : t(s)
eye((v(out3p)-v(out3n)))
€ 0.0
0.2
0.2
0.0
0.2
0.0
0.2
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0
0.0<

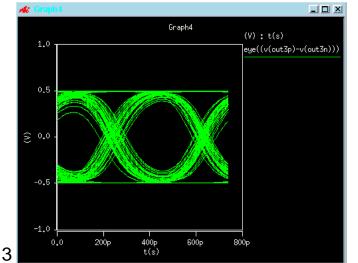
VGA coefficient adaptation

Equalizer

adaptation

start





Equalizer adaptation end