ITC-CSCC 2007

The 22nd International Technical Conference on Circuits/Systems, Computers and Communications

Proceedings Volume 1

July 8 - 11, 2007
Paradise Hotel, Busan, Korea

2. Design an Active Antenna Using an Equivalent Model
Cheolsoo Lee, Agency for Defense Development, Korea;
Jeongki Pack, Chungnam National University, Korea

3. An Effect of SAR Image Quality due to the Variation of Azimuth FM Rate
Chul H. Jung, Min S. Choi, Young K. Kwag, Korea Aerospace University, Korea

4. Implementation of Diplexer Embedded Active Integrated Antennas
Joonil Kim, Jinwoo Chang, Wontaek Lee, Yong Jee, Sogang University, Korea

5. Evaluation of ITU-R Recommendation P.1546 and Consideration for New Correction Factor

Chang-Hoon Lee, Young-Woo Kwak, Seong-Cheol Kim, Seok-Hee Bae, Seoul National University, Korea

6. Fast Fading Characteristics for LOS Path Loss in a Building
Supachai Phaiboon, Suripon Somkuarnpanit, King Mongkut's Institute of Technology Ladkrabang, Thailand

7. Forest Stem Volume Estimation Based on VHF-Band Backscatter Model at the Individual Tree Level
Anatoliy A. Kononov, Min-Ho Ka, Korea Polytechnic University, Korea

Monday, July 9, 13:00 - 15:00
MD2: Analog Circuits 2

Chair: Kazuhiro Shouno, University of Tsukuba, Japan

1. (Invited Paper) Low Power 6-b CMOS Folding-Interpolating A/D Converter
Danh-Cuong Do, Zhi-Yuan Cui, Nam-Soo Kim, Chungbuk National University, Korea

2. A Study of Phase-Noise Characteristics of Fr Oscillator Focusing on Output Position
Takeshi Imaike, Yukinori Sakuta, Yoshifumi Sekine, Nihon University, Japan

3. A Novel Low-Voltage CMOS Voltage Reference Circuit Insensitive to V_{DD} and Temperature Variations
Akira Nakajima, Takahiro Inoue, Akio Tsuneda, Kazuki Iwata, Kumamoto University, Japan

4. A Low Glitch 10-b CMOS DAC
Young-Ki Park, Do Danh Cuong, Zhi-Yuan Cui, Nam-Soo Kim, Chungbuk National University, Korea

5. A Simple Bridge Resistance Deviation-to-Frequency Converter for Resistive Sensor Bridges
Po Lee, Min-Young An, Chang-soo Won, Jin-Woong Jung, Won-Sup Chung, Sang-Hee Son, Cheongju University, Korea

6. A Gain-Adjustable Class AB Bipolar Linear Transconductor
Seong-Hoon Kim, Min-Young An, Po Lee, Jin-Woong Jung, Won-Sup Chung, Sang-Hee Son, Cheongju University, Korea

7. A 12-Ch 60-Gb/s Advanced Common-Gate Trans-Impedance Amplifier Array
K. Park, Woo-Young Choi, Yonsei University, Korea;
W. S. Oh, S. C. Lee, Korea Electronics Technology Institute, Korea

Monday, July 9, 13:00 - 15:00
ME2: RF Circuits 1

Chair: Sang-Gug Park, Uiduk University, Korea

1. (Invited Paper) An UltraWideBand BALUN on Thin Film Substrate using MCM-D Technology
Ji-Min Maeng, Sang-Sub Song, Kwang-Seok Seo, Seoul National University, Korea;
Chan-Sei Yoo, Kwang-Hoon Lee, Jae-Hyun Yoon, Dongsu Kim, Woo-Sung Lee, Korea Electronics Technology Institute, Korea;
Hee-Seok Lee, Samsung Electronics Co., Ltd., Korea

2. RFID System with AES Cipher Function
Hiroaki Miyoshi, Sharp Corp, Japan;
Isao Shirakawa, University of Hyogo, Japan;
Kenji Matsumura, KCS Corporation, Japan

3. Bias and Device Optimization for 0.13-μm CMOS Low-Noise Amplifier Design
Ickhyun Song, Hakchul Jung, Hee Sauk Jhon, Hyungcheol Shin, Seoul National University, Korea

4. Differential VCO with Diodes Feedback Using InGaP/GaAs HBT Technology
Bhanu Shrestha, Seong Soo Cho, Jun Gil Kang, Nam Young Kim, Kwangwoon University, Korea

5. A Triplexer Module with a GPS SAW Filter and a Cellular SAW Duplexer
Dongsu Kim, Jong In Ryu, and Jun Chul Kim, Korea Electronics Technology Institute, Korea

6. Impedance-Transforming Lumped-Baluns Consisting of Left-Handed Small Impedance Transformers
Hee-Ran Ahn and Bumman Kim, POSTECH, Korea

7. Novel GCPW-to-Embedded LTCC Rectangular Waveguide Transition for V-band System-on-Package Applications
Jae Jin Lee, Ki Chan Eun, Dong Yun Jung, Seong Jun Cho, and Chul Soon Park, Information and Communications University, Korea

Monday, July 9, 13:00 - 15:00
MF2: Watermarking 2

Chair: Adisorn Leelasantitham, UTCC, Thailand

1. (Invited Paper) Novel Reversible Difference Expansion Watermarking Algorithm for Triplet
Sachnev Vasiliy, Hyoung Joong Kim, Hana Know, Korea University, Korea

2. An Analysis of Intra-Prediction of H.264 for Digital Watermarking
Joon-Soo Ha, Hyun-Jun Choi, Ji-Sang Yoo, Dong-Wook Kim, Kwangwoon University, Korea;
Young-Ho Seo, Hansung University, Korea

3. 3D VRML Animation Watermarking
Hye-Jung Chang, Ki-Ryong Kwon, Pukyong National University, Korea;
Seong-Geun Kwon, Samsung Electronics Co. Ltd., Korea;
Eung-Joo Lee, Tae-il Jeong, Suk-Hwan Lee, TongMyong University, Korea;
Jae-Seung Lee, Korea Aerospace Research Institute, Korea

A 12-Ch 60-Gb/s Advanced Common-Gate Trans-Impedance Amplifier Array

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Abstract: In this paper, a 12-channel 60-Gb/s advanced common gate (ACG) trans-impedance amplifier (TIA) is realized in a 0.18-μm standard CMOS technology. The post-layout simulation results demonstrate that a single channel ACG TIA achieves 56-dBΩ trans-impedance gain (TZ gain), 5-Gb/s operations with 3-GHz bandwidth for 1.5-pF input parasitic capacitance including photodiode capacitance and ESD protection pad capacitance, and 34-pA/sqrt(Hz) input noise spectral density that corresponds to -18-dBm sensitivity for 10^{-12} BER. Total power consumptions is 48-mW from a single 1.8-V supply. The whole chip occupies the area of 4.55 x 1.49mm^2 including ESD protection pads.

1. Introduction

In an optical receiver, the front-end preamplifier is the most critical component affecting the whole system speed and noise-sensitivity. Traditionally, Ⅲ－Ⅴ materials such as GaAs and InP have been exploited to realize this preamplifier for high speed applications due to their high cutoff frequency and low noise characteristics. However, silicon deep-submicron CMOS technologies become more necessary to realize more cheap optical systems.

The inductive-peaking technique is very popular methods to enhance the bandwidth, such as LC-ladder filter configuration. The previous work said the inductive-peaking technique can achieve about 3 times larger bandwidth[1],[2]. However, passive inductor has very large area, for example, only 1-nH inductor demonstrates about 0.2 x 0.2mm^2. Therefore we exploit the bond-wire inductance as an inductor of the LC-ladder filter.

In this paper, we describe the design of a 12-ch 60-Gb/s advanced common-gate TIA array exploiting LC-ladder filter network, which is realized by bond-wire inductance, in a 0.18-μm standard CMOS technology.

2. TIA Design

The conventional common-source TIA has a number of tradeoffs between bandwidth, photodiode capacitance, TZ gain, and sensitivity. Especially, since the photodiode capacitance siginificantly limits the bandwidth, the efficient input configuration for the isolation from the photodiode capacitance is essential for the high speed operation. It is well known that the common-gate input configuration and its modified version can achieve better isolation of the photodiode capacitance than other configurations.

Figure 1. shows the entire block diagram of the proposed TIA, where all building blocks are designed to be differential so that common-mode noises can be effectively reduced. It consists of LC-ladder filter network, the CG input stage including local feedback stage, the common-source voltage-gain stage, and the DC offset cancellation output buffer. The first-order LC-ladder filter network consists of C_{PD}, bond-wire inductance, and on-chip capacitor (ESD protection pad capacitance + inserted capacitance). For the minimum peaking and optimal data transmission, inserted capacitor is determined into 0.1-pF for 1-pF photodiode capacitance and 1.6-nH estimated bondwire inductance. One input of the TIA is connected to a PIN photodiode and the other is connected to an off-chip capacitor (C_X) of which value is selected to be same as that of the photodiode.

The input impedance of the conventional CG stage is $\sim 1/g_{m1}$. However, the conventional CG stage cannot totally isolate the input parasitic capacitance due to the poor device characteristics of the CMOS such as small g_m. Figure. 2 shows the CG TIA including local feedback stage. This input configuration provides the virtual-ground input impedance of $1/(1+g_{mB}R_B)g_{m2}$, where $(1+g_{mB}R_B)$ is the voltage gain of the local feedback stage.

3. TIA Layout and performance summary

Post-layout simulations were conducted for the proposed advanced CG TIA by using a 0.18-μm standard CMOS technology. The total input parasitic capacitance becomes 1.5-pF including a 1-pF photodiode parasitic capacitance and a 0.5-pF ESD protection diode capacitance. As shown in Figure. 3, the 12-ch 60-Gb/s ACG TIA array was carefully laid out to eliminate the unexpected effects such as common-mode noise, signal delay, and crosstalk. Substrate contacts and well contacts are used between each channel for channel crosstalk isolation. The entire chip occupies the area of 4.55 x 1.49mm^2 including ESD protection diode pads.

Figure 4. illustrates the frequency response of the CG TIA, exhibiting 3-GHz bandwidth and 56-dBΩ TZ gain with 0.8-dB peaking. The bandwidth is optimized considering tradeoffs between noise and ISI performance for 5-Gb/s operations. As shown in Figure. 5, the average input noise spectral density is achieved to be ~34-pA/sqrt(Hz), which corresponds to the optical sensitivity of -18-dBm for 10^{-12} BER. The eye diagram for 5-Gb/s input stream is shown in Figure. 6.

4. Conclusion

A 12-channel 60-Gb/s differential advanced CG TIA array has been implemented in a standard 0.18-μm CMOS technology. Each channel consists of input LC-ladder filter networks and advanced CG TIA with DC-balanced output

buffer. The input parasitic capacitance, the bondwire inductance, and inserted on-chip capacitor are used in ladder filter networks, whereas the conventional inductive-peaking techniques exploit the passive inductor, which has very large area. Inserting only 0.1-pF on-chip capacitor, it can be found that the -3-dB bandwidth of the propopsed filter networks is 1.25-times than that without inserting capacitance. And advanced CG input configuration including local feedback stage can achieve more effective isolation from the input parasitic capacitance than the conventional input stage.

References

[1] Chia-Hsin Wu, Chih-Hun Lee, Wei-Sheng Chen, and Shen-Iuan Liu, "CMOS wideband amplifiers using multiple inductive-series peaking technique," *IEEE Journal of Solid-State Circuits, vol. 40, p. 548-552, Feb. 2005.*

[2] Ju-Hyoung Mun, Sung Min Park, and Myung-Ryoog Nam, "Four-Channel CMOS photoreceiver array for parallel optical interconnnects," *IEEE International Symposium on Circuits and Systems, p. 1529-1532, 2005.*

[3] Jun-De Jin, Hsu, and S.S.H., "40-Gb/s transimpedance amplifier in 0.18-um CMOS technology," *Solid-State circuit conference, ESSCIRC, 2006.*

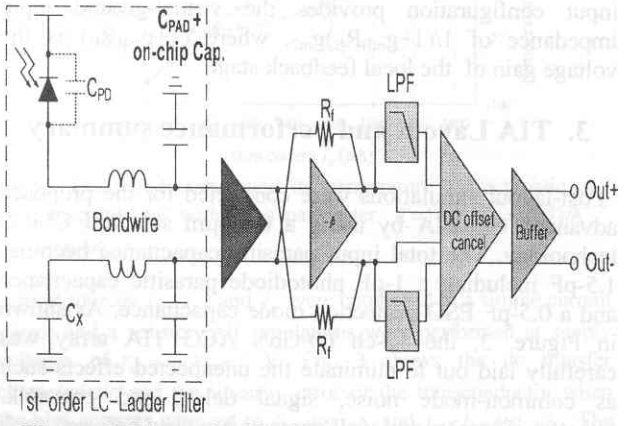
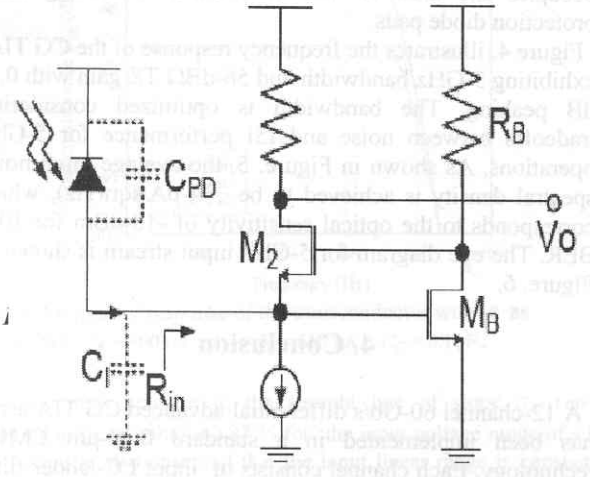


Figure. 1. The entire block diagram of the proposed TIA



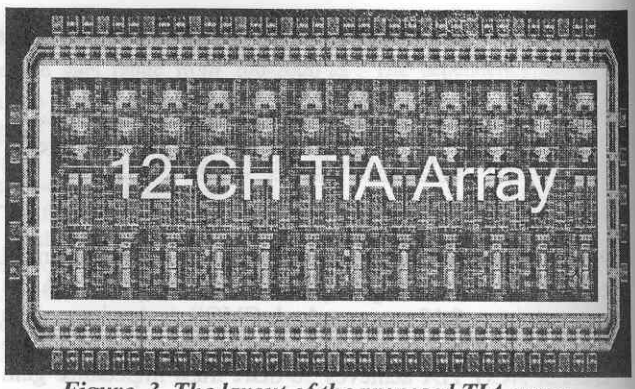


Figure. 3. The layout of the proposed TIA array

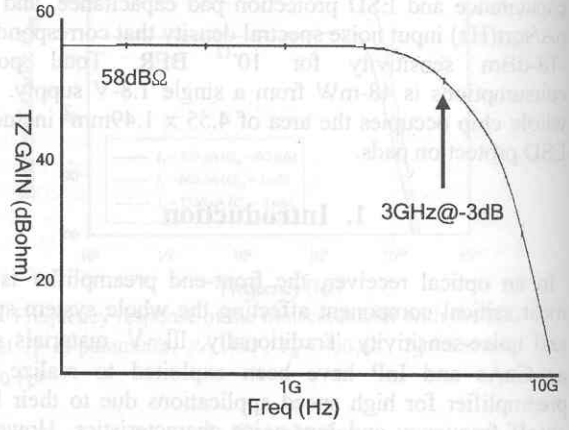


Figure. 4. The frequency response

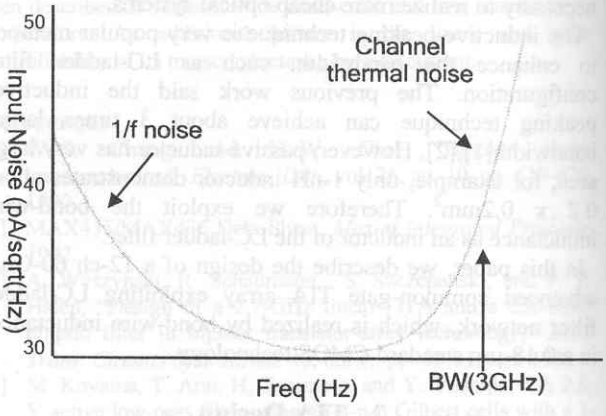


Figure. 5. Input Noise Spectral Density

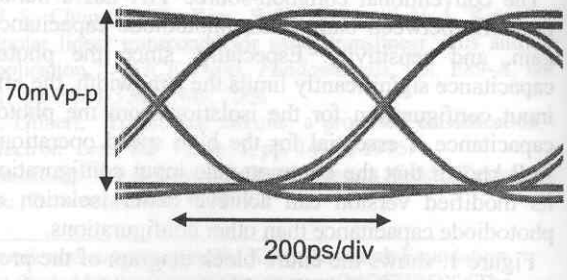


Figure. 6. The block diagram of the entire system