Bias Voltage Optimization of Vertical PN-Junction Photodetectors Fabricated in Standard CMOS Technology

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Abstract - We present vertical PN-junction photodetectors fabricated from standard 130 nm complementary metal-oxide-semiconductor (CMOS) process for applications in optical data transmission and optical interconnects. We experimentally observe that the bandwidth and responsivity of the photodetector are enhanced when the applied bias voltage is close to the reverse breakdown voltage. The fabricated photodetector has 3-dB bandwidth of 2.3 GHz and responsivity of 0.11 A/W at the optimum bias voltage.

1. Introduction

With increasing bitrates, optical interconnects and short-distance optical access networks are widely investigated. High volume and wide deployment of optical links indispensably require low-cost optical transceivers. For the optical transmitters, low-cost 850 nm AlGaAs/GaAs vertical-cavity surface-emitting lasers (VCSELs) are readily available. As a counter part, CMOS-based optical receivers are a strong candidate because low-cost, high-volume manufacturability is available and monolithic integration of a photodetector and receiver circuits is possible [1].

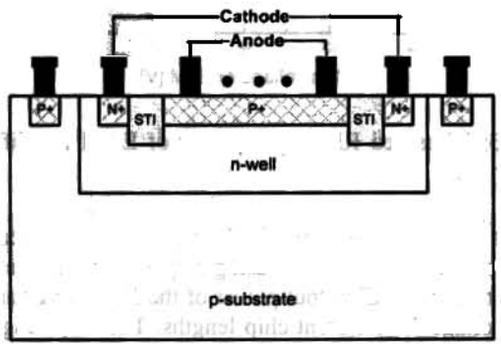
In spite of these advantages of CMOS-based optical receivers, there are inherent drawbacks of silicon material and CMOS process, which are not optimized for photodetector. Due to the indirect bandgap structure, silicon has large penetration depth, which is about 14 ㎛ under 850nm optical illumination [1]. However, CMOS compatible photodetectors have a narrow depletion region formed by PN junction between source/drain diffusion and n-well region resulting in low responsivity. In addition, low carrier mobility in silicon compared with InGaAs, which is used for conventional 1550 nm photodetectors, makes it difficult to realize high-speed photodetectors.

In order to overcome the bandwidth-efficiency product limit in CMOS compatible photodetectors, several approaches have been reported. Vertical p-i-n photodiodes with a low-doped epitaxial layer has been realized. With the help of large depletion width, high quantum efficiency of 44 % at the wavelength of 850 nm has been obtained [2]. However, this modified CMOS process induces an additional device fabrication cost and can affect the performance of CMOS electronic circuits. Another approach has implemented lateral p-i-n photodiodes on a silicon-on-insulator (SOI) substrate [3]. With elimination of the substrate diffusion current, high-speed photodetectors can be achieved. Nonetheless, SOI substrates are not commonly used in standard CMOS processes because of high costs.

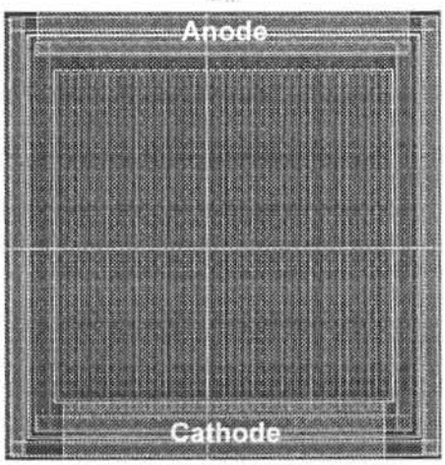
In this paper, we review the design consideration of CMOS compatible photodetectors for high-speed operation and report vertical PN-junction photodetectors fabricated by standard CMOS logic technology, DongbuAnam 130 nm CMOS process. Optimization of the bias voltage for high bandwidth-efficiency product of the photodetector is performed.

2. Photodetector structure

The speed of photodetectors are limited by RC time



(a)



(b)

Figure 1: (a) Schematic cross-section and (b) layout of fabricated photodetector.

constant (t_{RC}), transit-time in depletion region (t_{tr}) and diffusion time in charge neutral region (t_D) as explained in below equations [4].

$$t_{RC} = (R_S + R_L) \cdot C_J$$
$$t_{tr} = l_D / v$$
$$t_D = l_0^2 / 2D$$

where R_S is series resistance of photodetector, R_L is load resistance, C_J is junction capacitance of PN-junction photodiode, l_D is thickness of depletion region, v is carrier velocity, which can be replaced by saturation velocity (v_s) when high electric field is applied, l_0 is length of charge neutral region and D is diffusion constant of silicon. Among these speed-limiting time constants, diffusion time and transit-time dominantly affect the 3-dB bandwidth of the photodetector based on CMOS process [1].

In CMOS compatible photodetectors, two PN-junctions can be formed, which are P+/n-well and n-well/p-substrate junction [5, 6]. Consequently, different photodetector structure, which incorporates one or two PN junctions, can be possible. Photodetectors utilize two PN junctions have large photocurrent due to the wide depletion region, though slow response time in consequence of carrier diffusion process in the substrate region. On the other hand, photodetectors exploit only one PN junction, P+/n-well, can have fast response time with removal of the diffusion component even though small photocurrent. For high-speed operation, it is note that the lateral diffusion path should be also considered because it can degrade the bandwidth of photodetector as explained above equation. For example, if the electrons suffer from diffusion length of 1 ㎛, the time constant and corresponding 3-dB bandwidth of diffusion current are about 12.8 ns and 1.24 GHz, respectively. As a result, the electrode spacing, which directly constrain the diffusion length, has to be carefully designed for high-speed operation.

Figure 1 shows cross-sectional diagram and layout of fabricated photodetectors. In order to eliminate the slow diffusion current in substrate region, we only use vertical P+/n-well junction and the multi-finger electrode and narrow finger space of 0.5 ㎛ are formed to collect the photogenerated carriers effectively without going through the lateral diffusion path. The active area of photodetector is about 30×30 ㎛^{2} and the salicide process is blocked for the optical window.

3. Simulation

In order to examine the dominant photocurrent components including drift and diffusion currents dependent on the device structure, we simulated the photodetector using two-dimensional process simulator TSUPREM4 and device simulator MEDICI. Figure 2 (a) shows the cross sectional diagram for the simulation. To reduce simulation time, device structure of photodiode is simplified in the simulation. Instead of multi-finger electrode, single electrode is used and optical

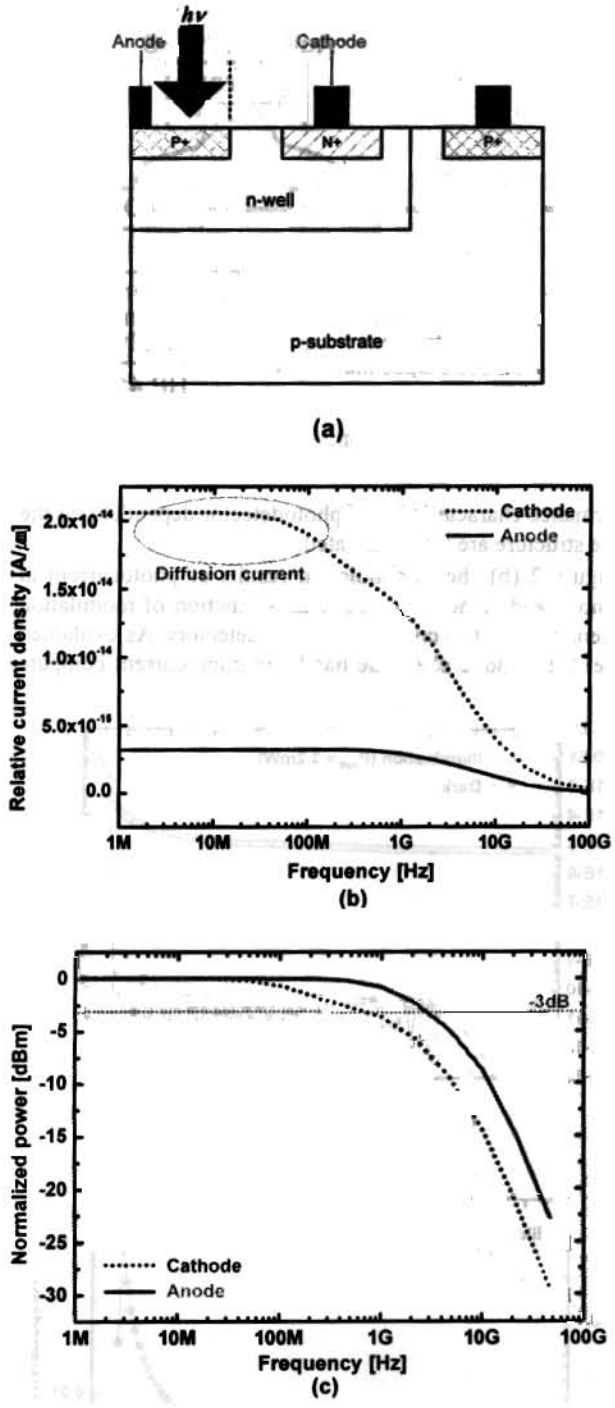


Figure 2: (a) Schematic cross-section for simulation. (b) Anode and cathode current density as a function of modulation frequency. (c) Normalized detected power as a function of modulation frequency.

illumination was done within P+ region in accordance with fabricated device as shown in figure 1 (a). Due to the lack of information related to the device fabrication condition, commonly known CMOS process parameters are used for the simulation [7]. Although the simplification and approximation are applied to the simulation, it is believed that the overall

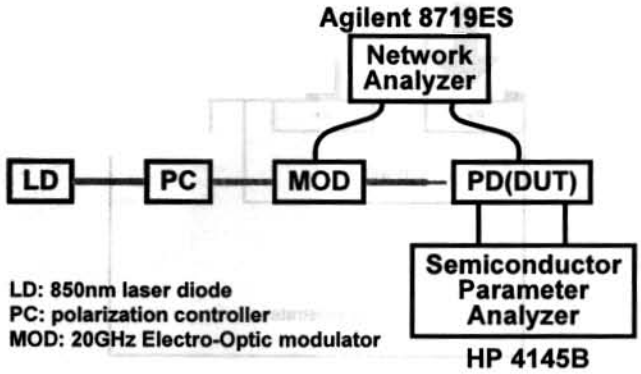


Figure 3: Experimental setup.

performance characteristics of photodetector dependent on the device structure are well estimated.

Figure 2 (b) shows simulation results of photocurrent at the anode and cathode electrode as a function of modulation frequency in CMOS compatible photodetectors. As explained above, the cathode electrode has large photocurrent compare

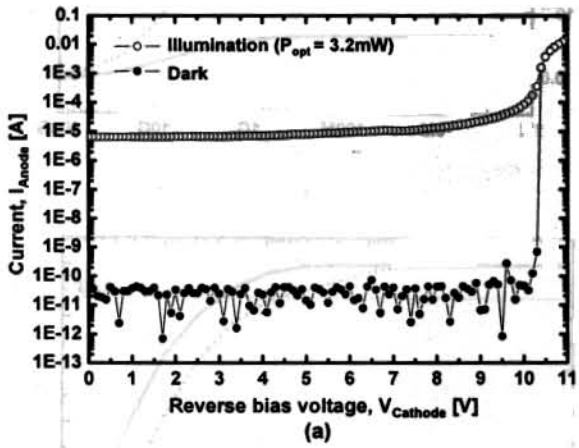


Figure 4: (a) I-V characteristics of the photodetector under dark and illumination condition. The incident optical power is 3.2 mW. (b) Photocurrent and responsivity as a function of applied bias voltages.

with the anode one because photogenerated carriers are collected by both P+/n-well and n-well/p-substrate PN junctions. However, it can be seen that photocurrent at cathode electrode has low frequency components, which are attributed to diffusion path in the p-doped substrate. Figure 2 (c) shows normalized photodetected power at the cathode and anode electrode as a function of modulation frequency. It is clearly observed that the 3-dB bandwidth of cathode photocurrent is lower than anode one due to slow diffusion current. As a consequence, it is desirable to use the photocurrent from anode electrode for high-speed operation in CMOS compatible photodetectors.

4. Experiment and result

Figure 3 shows experimental setup for the characterization of the photodetector performance. The wavelength of 850nm optical signal was generated by laser diode (LD) and then inserted into polarization controller and 20 GHz electro-optic modulator. The optical coupling was performed using single-

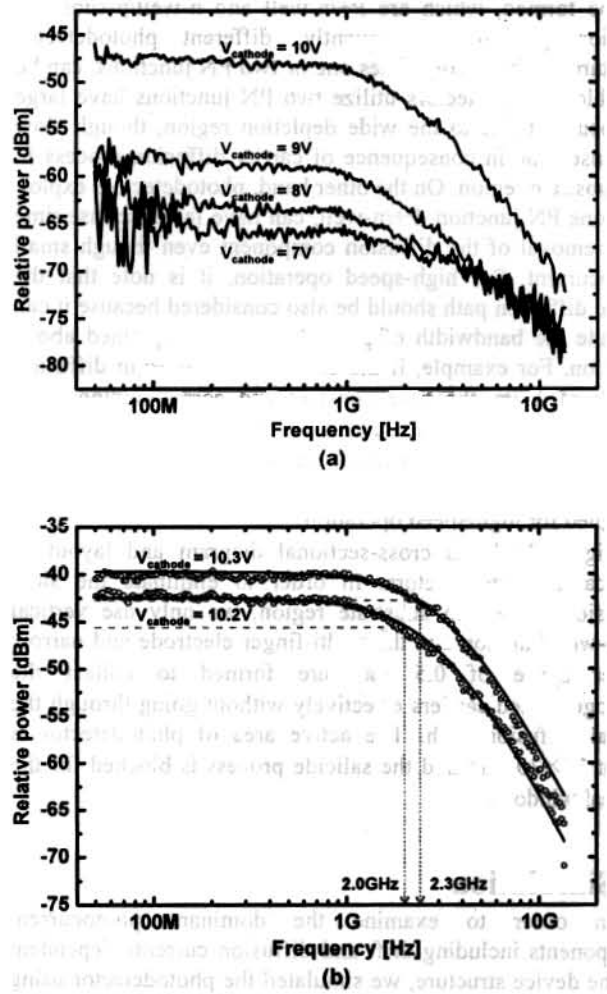


Figure 5: Optical modulation responses of the photodetector (a) at different bias voltages and (b) around the reverse breakdown voltages. The hollow circles represent measured data and solid lines indicate fitting results.

mode lensed-fiber and all measurements were done on wafer. For the accurate measurement of optical modulation response, 13.5 GHz vector network analyzer was used and bias voltage of the device was supplied by semiconductor parameter analyzer.

Figure 4 shows I-V characteristics with and without optical illumination and calculated photocurrents and external responsivity, which includes optical coupling loss. The responsivity is defined as the ratio between the photocurrents and incident optical power at the output of the fiber. In figure 4 (b), it can be seen that photocurrent and responsivity increases with the increasing reverse bias voltage due to enhanced depletion width of PN-junction. At the reverse voltage above 10.3V, reverse breakdown occurs and responsivity has the maximum value of 0.11 A/W as shown in figure 4 (b). This high responsivity can be explained by the avalanche gain process, which is attributed to the increased carrier concentration under optical illumination. Despite the avalanche gain process under optical illumination, the photodetector has low dark current of about 700 pA at the reverse bias voltage of 10.3 V.

Figure 5 shows the optical modulation response of the fabricated photodetector at different bias voltages. When applied reverse voltage increases, the detected power increases as in the I-V characteristics of the photodetector. Interestingly, it can be observed that, bandwidth and responsivity are maximized at the bias voltage close to the reverse breakdown voltage as shown in figure 5 (b). This enhanced bandwidth is believed due to reduced transit-time in the high electric field region.

5. Conclusion

We fabricated CMOS-compatible vertical PN-junction photodetectors and optimize the bias voltage for high bandwidth and responsivity. At the bias voltage close to the reverse breakdown voltage, 3-dB bandwidth of 2.3 GHz and responsivity of 0.11 A/W are obtained.

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