2006 International SoC Design Conference

COEX Conference Center, Seoul, Korea
26~27 October, 2006

2006 International SoC Design Conference www.isocc.org

2.0.0.6 . I.S.O.C.C

International
SoC Design Conference

45. Design and MPW Implementation of Floating Point Ips for 3D Graphics

Jungwoo Lee, Kichul Kim, Department of Electrical & Computer Engineering, University of Seoul

46. The VLSI Design of a 92ksps 12-channel Protective Relay

Jong Kang Park, Hong Moon Wang, Chun Guan Kim, Jong Tae Kim*, School of Information and Communication Engineering, SungKyunkwan University

47. The Implementation of Sigma-Delta ADC/DAC Digital Block

JeongHwa Heo*, JeongSu Han*, SangBong Park*, NhoKyung Park**, *Information and Communication Department, Semyung University, **Information and Communication Engineering Department, Hoseo University

48. A 5-Gb/s Half-Rate Clock Recovery Circuit

Pyung-Su Han, Woo-Young Choi, Electrical and Electonic Engineering, Yonsei university

49. A Fully Integrated Class-E Amplifier for Wireless LAN Application

Chan Hyuck Park, Kyung Heon Koo, Department of Electronics Engineering, University of Incheon

50. Design of Wide-Band 0.25㎛ CMOS Mixer

Kang Ho Lee, Kang Jeon Lee, Kyung Heon Koo, Electical Engineering Department, University of Incheon

51. The Design of CMOS RF Front-end for Multi-mode/Multi-band Wireless Receiver

Bohyun Hwang, Jachoon Jung, Shinnyoung Kim, Changsik Yoo, Department of Electrical and Computer Engineering, Hanyang University

52. Pre-emphasis Transmitter for DRAM Bus System with Analog Calibration

Jungjune Park, Changsik Yoo, Department of Electronics and Computer engineering, Hanyang University

53. Implementation of Digital Part of RFID Tag

Jongho Yun, Jinsung Park, Department of Electrical Engineering Computer Science, Hanyang University

54. A 0.18um CMOS Phase Locked Loop for Fast Locking Time for 10Gbps Optical Receiver

Ju-Pyo Hong, Kwang-Il Oh, Lee-Sup Kim, Department of EECS, KAIST

55. A 3.2Gbps/pin Transmitter for DDR Memory Interface with Pulsed Latch Embedded Pre-Emphasis Circuit

Kwang-Il Oh, Ju-Pyo Hong, Lee-Sup Kim, Department of EECS, KAIST

56. A 3.2Gbps/pin Transceiver for DDR Memory Interface

Kwang-Il Oh, Byung-guk Kim, Lee-Sup Kim, Department of EECS, KAIST

17:30~17:50 **Closing Ceremony & Award Presentation** [Room311]

Session Chair :

Eui-Young Chung (Yonsei University)

A 5-Gb/s Half-Rate Clock Recovery Circuit

Pyung-Su Han
Electrical and Electronic Engineering
Yonsei university
Seoul, Korea
ps@tera.yonsei.ac.kr

Woo-Young Choi
Electrical and Electronic Engineering
Yonsei univiersity
Seoul, Korea
wchoi@yonsei.ac.kr

Abstract - *A half-rate clock recovery circuit for 5-Gb/s data rate was designed in 0.25-μm CMOS technology. The bang-bang phase detector was used for high-speed operation. The simulation results show that the half-rate clock was successfully extracted from random bit data sequence up to 6-Gb/s. In initial measurement of the fabricated chip, 2.5-GHz clock was extracted from 2.5-Gb/s PRBS 2^7-1. Further measurement will be done and presented.*

Keywords: Bang-bang phase detector, BBPD, Half-rate clock recovery.

1 Introduction

BBPD (Bang-Bang Phase Detector) is widely used for high-speed clock recovery circuits [1]. It can operate at very high frequency because of its simple structure. Also by using half-rate clocking, doubling the data-rate without increasing the clock frequency, a circuit can process two bits in one clock period. Adopting these techniques at the same time [2], very high-speed clock recovery circuits can be designed.

The conventional PLL (phase-locked loop) model can not be used for BBPLL (Bang-Bang Phase-Locked Loop) analysis because of BBPLL's nonlinearity. Instead, the BBPLL model proposed in [1] can be used. An example of BBPLL schematic diagram is shown in Fig. 1.

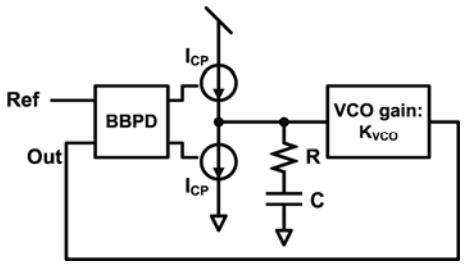

Figure 1. Bang-Bang PLL schematic diagram

This work was sponsored in part by the Ministry of Science and Technology and the Ministry of Commerce, Industry and Energy through System IC 2010 program. This work was also supported by Ministry of Commerce, Industry and Energy under IDEC Support Program (MPW, CAD) and MagnaChip Semiconductor.

2 Bang-Bang phase detector

All building blocks except for charge pumps and differential-to-single converters are designed with fully differential circuits for high-speed operation.

Fig. 2 shows designed half-rate BBPD. Data bits are sampled using Clk_I and Clk_Q. Sampled data bits, A, B and C are compared by XOR gates to determine whether the clock phase is faster or slower than data bits, generating Up and Dn signals.

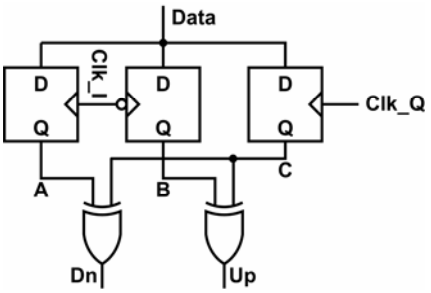

Figure 2. Half-rate Bang-Bang phase detector

3 Simulation results

The circuit was designed with 0.25-μm CMOS technology. Its operation was verified by SPICE simuation. Considering parasitic effects, 6-Gb/s random bit sequence was used for data input, which is 20% faster than target speed, 5Gb/s. Fig. 3 shows recovered clock signal overlapped with a input data eye-diagram.

4 Prototype chip

The circuit was fabricated with 0.25-μm CMOS technology. A photograph of the prototype chip is shown in Fig. 4. The core area occupies an area of 320μm × 130μm. The prototype chip was glued on a test circuit board and their terminals were connected using bonding-wires by COB (Chip On Board) technique.

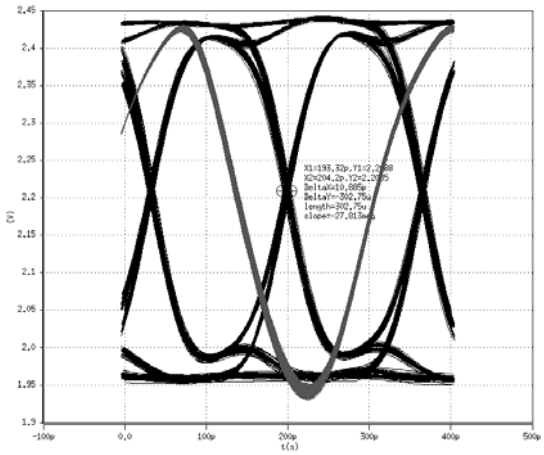

Figure 3. Recovered clock from 6-Gb/s random bit sequence and input data eye-diagram

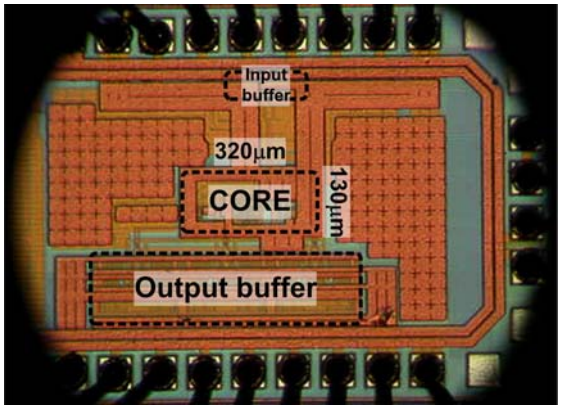

Figure 4. Prototype chip photograph

5 Measurement results

In the initial measurement, the clock recovery operation was verified using half-speed data bit pattern as input data. 2.5-GHz clock signal was successfully extracted from 2.5-Gb/s data signal. Every single bit in a half-speed bit sequence is seen as identical two bits for the clock recovery circuit. This effectively reduces clock recovery circuit's loop gain to half. Fig. 5 shows recovered clock from 2.5-Gb/s 2^7-1 PRBS. Measured jitter was 10.7ps [rms] and 69ps [p2p]. Table 1 summarizes measurement results. Full-rate clock recovery measurement using 5-Gb/s bit sequence will be done and its results will be presented.

6 Conclusions

A half-rate clock recovery circuit using a bang-bang phase detector was designed with 0.25-µm CMOS technology. Its operation was verified by SPICE simulation. A prototype chip was fabricated. In initial measurement, a half-speed data pattern was used as input data and 2.5-GHz clock was sucessfully extracted from 2.5-Gb/s 2^7-1 PRBS. Further measurement including clock recovery from 5-Gb/s bit stream will be done and the results will be presented.

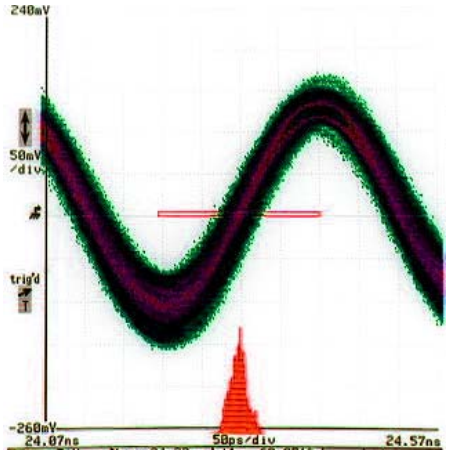

Figure 5. Recovered clock waveform @ 2.5GHz, from 2.5-Gb/s 2^7-1 PRBS

Table 1. Performance summary

Technology	0.25-µm CMOS
Chip Area	Core : 320-µm × 130-µm
VCO freq. range	1.65-GHz ~ 3.5-GHz
VCO gain	150-MHz/V ~ 550MHz/V 350-MHz/V @ 2.5GHz
Jitter @ 2.5Ghz with 2^7-1 PRBS	RMS jitter : 10.7ps P2P jitter : 69ps
Power consumption	Core : 22.5mW Input/output buffer : 250mW

References

[1] R. C. Walker, "Designing bang-bang PLLs for clock and data recovery in serial data transmission systems", in Phase-Locking in High-Performance Systems, B. Razavi, Ed: Wiley-IEEE Press, 2003, pp. 34-45.

[2] Yinghua Qiu, Zhigong Wang, Yong Xu, Jingfeng Ding, En Zhu, Mingzhen Xiong, "5-Gb/s 0.18-µm CMOS clock recovery circuit", VLSI Design and Video Technology, 2005, Proceedings of 2005 International Workshop on, 28-30 May 2005, pp. 21-23