2006 International SoC Design Conference

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International
SoC Design Conference

Hyung-Joon Chi, Jae-seung Lee, Hong-June Park, POSTECH

13:50 ~ 14:10

• A Portable and Input-Duty-Independent Multiphase lock Generator

Dognsuk Shin, Moo-young Kim, Hyunsoo Chae, Pulkit Jain, Chulwoo Kim, Korea University

14:10 ~ 14:30

• 1.25Gbps Clock/Data Recovery with a Wide Frequency Tracking

Jung Yong Lee, Jin Ku Kang, Inha University

14:30 ~ 14:50

• A 5-Gb/s Half-rate Clock Recovery Circuit in 0.25-um CMOS Technology

Pyung-Su Han, Woo-Young Choi, Yonsei Unviersity

14:50 ~ 15:10

• Asynchronous Wrapper Design based on Hybrid Ternary Data Encoding Scheme

Young-IL Lim, Je-Hoon Lee, Kyoung-Rok Cho, Chungbuk National University

13:30 ~ 15:10 Session 15 [Room 320A]

Communication SoC III

Session Chair :

Jaehee You (Hongik University)

Myung-Sub Lim (Chonbuk National University)

13:30 ~ 13:50

• An FPGA Implementation of MML-DFE for Spatially Multiplexed MIMO Systems

Tae Ho Im, Kyu In Lee, Ki Cheol Jeong, Chang Hwan Park, Sungwook Yu, Jae Kwon Kim, Yong Soo Cho, Chung Ang University, Yonsei University

13:50 ~ 14:10

• A Design Implementation of IEEE 802.11a WLAN

Sang-In Kim, Je-Hoon Lee, Kyoung-Rok Cho, Chungbuk National University

14:10 ~ 14:30

• Low Complexity Modified Euclid's Algorithm for Reed-Solomon Decoder

Hyoungjin Yun, Jaehyun Baek, Myung Hoon Sunwoo, Ajou University

14:30 ~ 14:50

• System Level Prototyping of DSP for DVB-T Receiver

Shin-Yo Lin, Wei-Hsiang Su, Tsung-Han Tsai, National Central University

14:50 ~ 15:10

• An Optimal RSA Crypto-processor Design Based on Montgomery Algorithm

Seok-Won Heo, Yong-Surk Lee, Yonsei University

13:30 ~ 15:10 Session 16 [Room 320B]

SoC Testing and Verification II

Session Chair :

Sang-Bock Cho (University of Ulsan)

Byeong Min (Samsung Electronics)

13:30 ~ 13:50

• An Efficient Diagnosis Method using Pattern Comparison

Hyungjun Cho, Joohwan Lee, Yoseop Lim, Sungho Kang, Yonsei University

13:50 ~ 14:10

• A Fault Tolerant Carry Select Adder with Modular Self Checking Scheme

Gunbae Kim, IlWoong Kim, Ilgweon Kang, Sungho Kang, Yonsei University

14:10 ~ 14:30

• The Scalable and Reconfigurable DFT for Embedded A/MS Cores

A 5-Gb/s Half-rate Clock Recovery Circuit in 0.25-μm CMOS Technology

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Abstract – *A half-rate clock recovery circuit for 5-Gb/s data rate was designed in 0.25-μm CMOS technology. The bang-bang phase detector was used for high-speed operation. The simulation results show that the half-rate clock was successfully extracted from random bit data sequence up to 6-Gb/s. In initial measurement of the fabricated chip, 2.5-GHz clock was extracted from 2.5-Gb/s PRBS 2^7-1. Further measurement will be done and presented.*

Keywords: Bang-bang phase detector, BBPD, Half-rate clock recovery

1 Introduction

BBPD (Bang-Bang Phase Detector) is widely used for high-speed clock recovery circuits [1]. Because of its simple structure, it can operate at very high frequencies and has become an essential building block in a serial link system where data rate is extremely high. Half-rate clocking is another popular technique for high-speed data transmission applications. Using both rising and falling edges of clock, a circuit can process two bits in one clock period, doubling the data-rate without increasing the clock frequency. Adopting two techniques at the same time [2], very high-speed clock recovery circuits can be designed.

The conventional PLL (phase-locked loop) model can not be used for BBPLL (Bang-Bang Phase-Locked Loop) because of BBPLL nonlinearity. Instead, the BBPLL model proposed in [1] can be used. An example of BBPLL schematic diagram is shown in Fig. 1. The voltage drop across the resistor caused by the charge pump current makes an instantaneous frequency jump in the output clock. The output clock phase change due to the frequency jump can be calculated by integrating frequency jump over time, as expressed in (1). Then this current is accumulated in the capacitor, and it generates a voltage slope. This also causes phase change in output clock. It is expressed in (2). T is the clock period. According to [1], to achieve stability in a BBPLL, (1) should be much larger than (2) by a factor of more than 20.

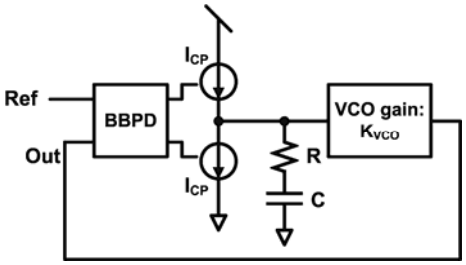

Figure 1. An example of BBPLL schematic diagram

$$\theta_R = 2\pi K_{VCO} I_{CP} RT \tag{1}$$

$$\theta_C = 2\pi \int_0^T \left(K_{VCO} \frac{I_{CP}}{C} t \right) dt = \frac{\pi K_{VCO} I_{CP} T^2}{C} \tag{2}$$

2 Building blocks

All building blocks except for charge pumps and differential-to-single converters are designed with fully differential circuits for high-speed operation.

2.1 VCO

A VCO delay cell and its bias circuit were designed. They are shown in Fig. 2. Two control voltages are used for its coarse and fine control, so that a wide oscillation range can be achieved, while VCO gain is kept low.

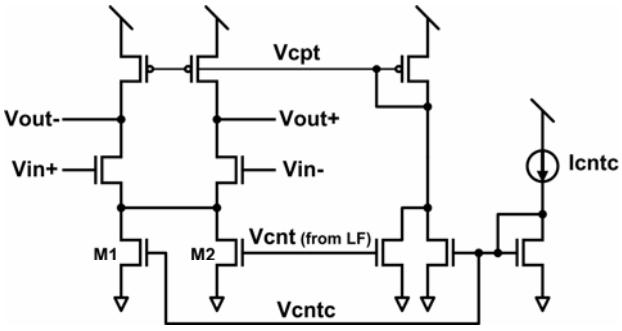

Figure 2. VCO delay cell and bias circuit

The coarse tuning voltage, Vcntc, is determined by an external bias current Icntc and it is used for initial frequency acquisition. After frequency acquisition, it can be kept fixed. Then Vcnt finely controls output clock frequency. To achieve a low VCO gain and a larege tuning range at the same time, M1 is sized much larger than M2. Vcpt is generated using a copy of VCO cell bias current so that output swing level is relatively constant over wide VCO tuning ranges.

2.2 VCO

A four-stage ring oscillator was designed with the delay cells and it is shown in Fig. 3. It generates two clock signals of which phases are separated by 90°. That is, Clk_I is in-phase clock and Clk_Q is quadrature clock. Buffers are used to isolate capacitive loads at the delay cells output from the circuits connected to the VCO.

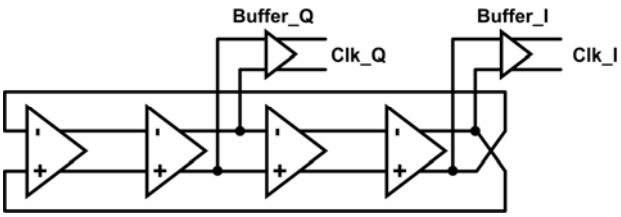

Figure 3. I/Q clock generating VCO

2.3 BBPD

Fig. 4 shows designed half-rate BBPD. Data bits are sampled using Clk_I and Clk_Q. Sampled data bits, A, B and C are compared by XOR gates to determine whether the clock phase is faster or slower than data bits, generating Up and Dn signals.

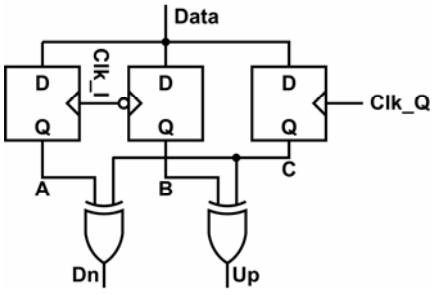

Figure 4. Half-rate bang-bang phase detector using I/Q clock

Fig. 5 shows detailed signal waveforms of half-rate BBPD in operation. When the loop is locked, rising and falling edges of Clk_I are at the center of bit intervals and rising edges of Clk_Q are at bit boundaries. When clock lags behind data, 75% of Dn signal (A⊕C) in a clock period becomes low, because rising edges of Clk_I and Clk_Q come in the same data bit interval, therefore A and C have the same logic value. 75% of Up signal (B⊕C) in a clock period becomes high if the B and C are different. If data bits stay unchanged, it becomes low. 25% of Up and Dn signals can be regarded as random values and in a long term, and they will eventually cancel out. In case that clock leads data, it works in the opposite way. As a result, when data bit switches, the direction of phase error is observed in Up and Dn signals. The effective gain of the half-rate BBPD is smaller by a factor of 0.5×0.75 than original BBPD in BBPLL, assuming that the possibility of data bit switching is 50%

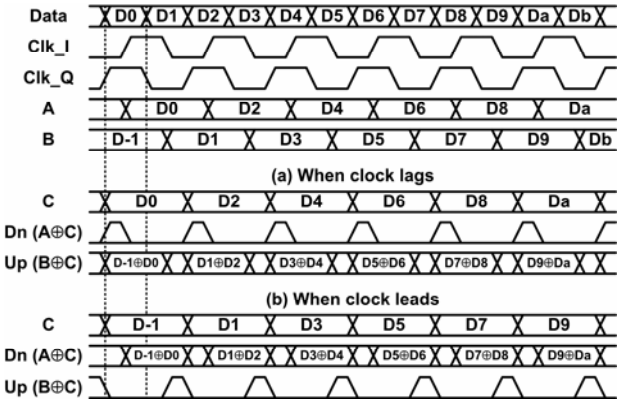

Figure 5. Operation of half-rate BBPD

2.4 Charge pump

Fig. 6 shows the designed charge pump. To minimize the mismatch between Up and Dn currents, a feedback amplifier is used [3]. It makes the voltages at output node (Vcnt) and node xx the same, trying to make both sides of charge pump have the same bias condition. By doing this, usable range of Vcnt can be extended dramatically. Cc is added for feedback loop stability.

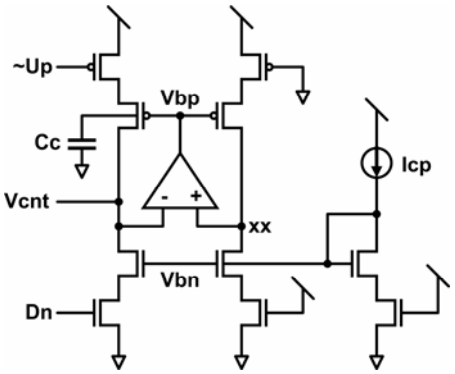

Figure 6. Charge pump and bias circuit

2.5 Clock recovery circuit

Using building blocks described in the previous sections, a half-rate clock recovery circuit was designed.

Its schematic diagram is shown in Fig. 7. Because the BBPD shown in Fig. 5 detects phase error based on even numbered bits, D0, D2, D4, and so on, it utilizes only half of data transitions. As shown in Fig. 7, another BBPD for odd numbered bits, D1, D3, D5, and so on, was used.

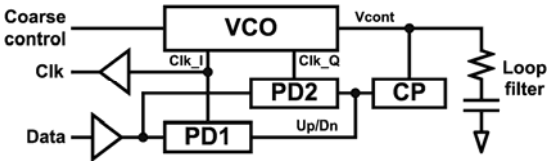

Figure 7. Schematic diagram of clock and data recovery circuit

R and C values for the loop filter were determined using (1) and (2) and their values are shown in Table. 1.

Table 1. Loop filter parameters

VCO gain	500MHz/V
θ_R	0.5%
R for loop filter	500Ω
$\theta_R/\theta c$	More than 100
C for loop filter	120pF

3 Simulation results

The circuit was designed with 0.25-μm CMOS technology. Its operation was verified by SPICE simuation. Considering parasitic effects, 6-Gb/s random bit sequence was used for data input, which is 20% faster than target speed, 5Gb/s. Fig. 8 shows recovered clock signal overlapped with a input data eye-diagram.

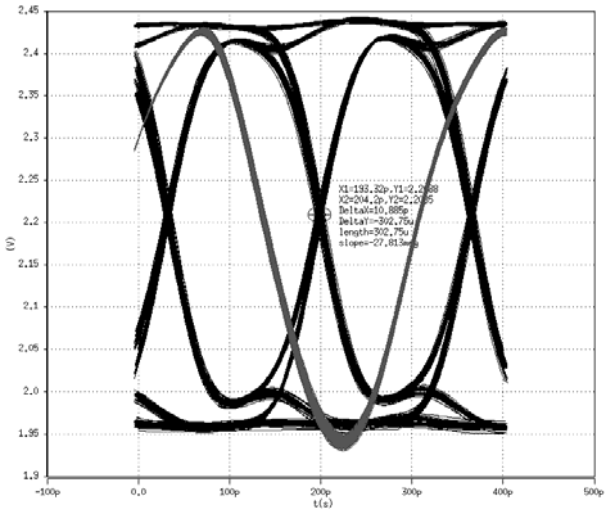

Figure 8. Recovered clock from 6-Gb/s random bit sequence and input data eye-diagram

4 Prototype chip

The circuit was fabricated with 0.25-μm CMOS technology. A photograph of the prototype chip is shown in Fig. 9. The core area occupies an area of 320μm × 130μm. The prototype chip was glued on a test circuit board and their terminals were connected using bonding-wires by COB (Chip On Board) technique.

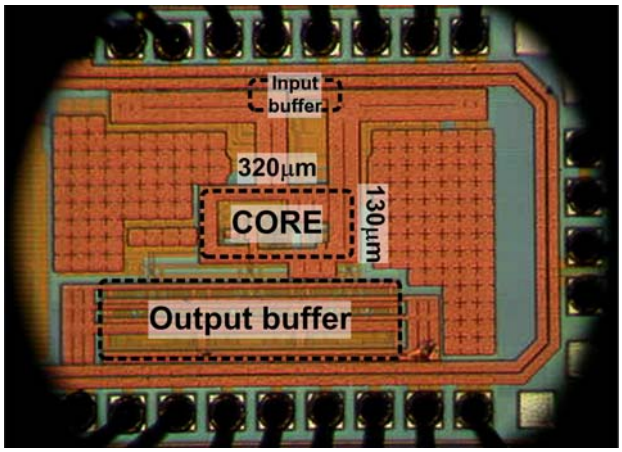

Figure 9. Prototype chip photograph

5 Measurement results

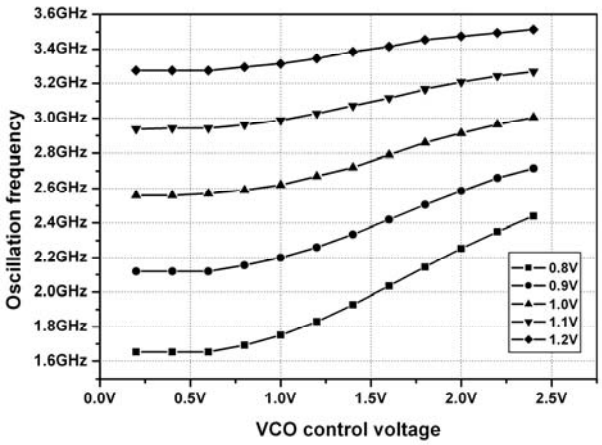

Figure 10. Mesured plot of control voltage to oscillation frequency transfer of fabricated VCO, depending on its coarse tuning voltage

The VCO oscillation frequency range of prototype chip was measured and plotted in Fig. 10. Frequency was measured using a spectrum analyzer while the coarse and fine control voltages were being swept. Each curve on Fig. 10 represents a coarse control voltage as shown in the legend. VCO gains for each curve were also calculated and plotted in Fig. 11. It ranges from 150MHz/V to 550MHz/V.

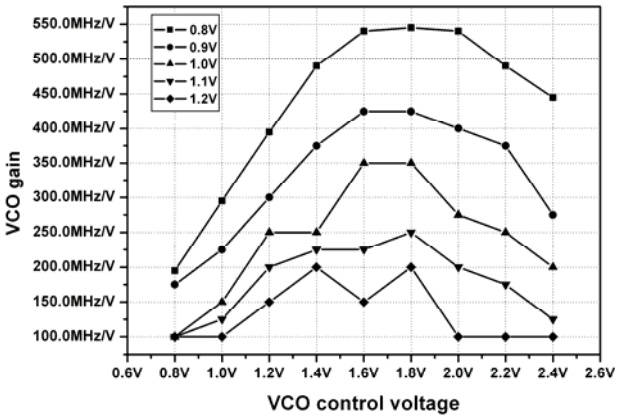

Figure 11. Measured VCO gain curve depending on coarse tuning voltage

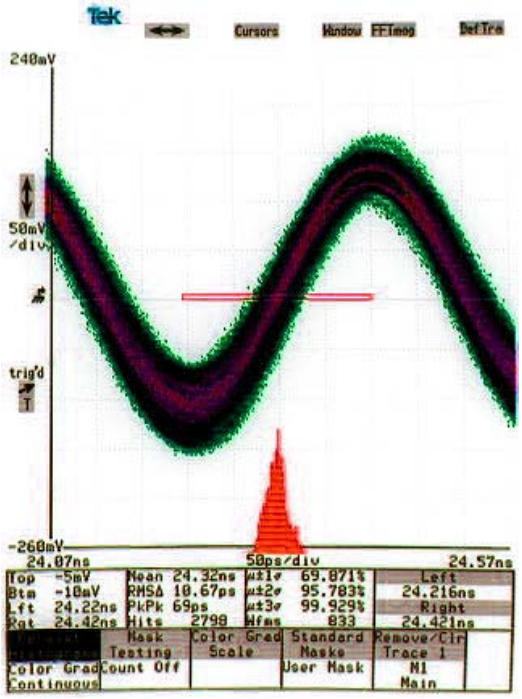

Figure 12. Recovered clock waveform @ 2.5GHz, from 2.5-Gb/s 2^7-1 PRBS

In the initial measurement, the clock recovery operation was verified using half-speed data bit pattern as input data. 2.5-GHz clock signal was successfully extracted from 2.5-Gb/s data signal. Every single bit in a half-speed bit sequence is seen as identical two bits for the clock recovery circuit. This effectively reduces clock recovery circuit's loop gain to half. Fig. 12 shows recovered clock from 2.5-Gb/s 2^7-1 PRBS. Measured jitter was 10.7ps [rms] and 69ps [p2p]. Table 2 summarizes measurement results. Full-rate clock recovery measurement using 5-Gb/s bit sequence will be done and its results will be presented.

Table 2. Performance summary

Technology	0.25-μm CMOS
Chip Area	Core : 320-μm × 130-μm
VCO freq. range	1.65-GHz ~ 3.5-GHz
VCO gain	150-MHz/V ~ 550MHz/V 350-MHz/V @ 2.5GHz
Jitter @ 2.5Ghz with 2^7-1 PRBS	RMS jitter : 10.7ps P2P jitter : 69ps
Power consumption	Core : 22.5mW Input/output buffer : 250mW

6 Conclusions

A half-rate clock recovery circuit using a bang-bang phase detector was designed with 0.25-μm CMOS technology. Its operation was verified by SPICE simulation. A prototype chip was fabricated. In initial measurement, a half-speed data pattern was used as input data and 2.5-GHz clock was sucessfully extracted from 2.5-Gb/s 2^7-1 PRBS. Further measurement including clock recovery from 5-Gb/s bit stream will be done and the results will be presented.

7 Acknoldgement

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References

[1] R. C. Walker, "Designing bang-bang PLLs for clock and data recovery in serial data transmission systems", in Phase-Locking in High-Performance Systems, B. Razavi, Ed: Wiley-IEEE Press, 2003, pp. 34-45.

[2] Yinghua Qiu, Zhigong Wang, Yong Xu, Jingfeng Ding, En Zhu, Mingzhen Xiong, "5-Gb/s 0.18-μm CMOS clock recovery circuit", VLSI Design and Video Technology, 2005, Proceedings of 2005 International Workshop on, 28-30 May 2005, pp. 21-23

[3] Jae Shin Lee, Woo Kang Jin, Dong Myung Choi, Gun Sang Lee, Suki Kim, "A wide range PLL for 64x speed CD-ROM & 10x speed DVD-ROM", Consumer Electronics, 2000. ICCE. 2000 Digest of Technical Papers. International Conference on, 13-15 June 2000, pp. 98-99.