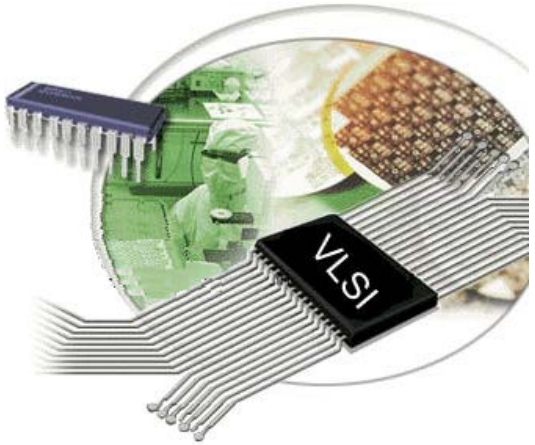
2006년도 SOC 학술대회

- 일시 : 2006년 5월 27일(토)
- 장소 : 숭실대학교 형남공학관



- 주최 : 대한전자공학회 SoC 설계 연구회
- 주관 : 숭실대학교 정보통신연구소
- 후원 : IEEE SSCS/EDS Joint Chapter of Seoul Section
  삼성전자, Nanno solutions Inc., Core logic Inc.,
  다이나릿시스템, 한백전자, 휴인스, FCI, 리버트론

사단법인 대한전자공학회
The Institute of Electronics Engineers of Korea

S11 Video Signal Processing for H.264 Ⅱ

14:20 ~ 16:00 113호 좌장 : 손채봉 교수 (광운대)

H.264/AVC 움직임 보상을 위한 참조버퍼 관리의 효율적 구현
김종태, 공진흥 (광운대)

H.264/AVC 움직임 보상기 설계
김준형, 홍민철, 이찬호, 이성수, 노태문, 여순일, 김종대 (숭실대)

H.264/AVC 복호기에서 움직임 보상기와 연계한 효율적인 인트라 예측기 아키텍쳐
박종식, 이성수, 홍민철, 이찬호, 노태문, 여순일, 김종대 (숭실대)

서브-샘플링을 이용한 H.264 인트라 예측기의 효율적 구현
이기섭, 이범철, 조중휘 (인천대)

움직임 벡터의 국부적 통계 특성을 이용한 저전력 H.264/AVC 움직임 추정기
양현철, 이성수, 홍민철 (숭실대)

다중연산구조기반의 고밀도 성능향상을 위한 움직임추정의 디인터레이싱 방법
이강환 (한국기술교육대)

S12 Video/Audio Signal Processing Ⅱ

14:20 ~ 16:00 103호 좌장 : 이광엽 교수 (서경대)

SoC 하드웨어 설계를 위한 얼굴 인식 알고리즘의 고정 소수점 모델 구현 및 성능 분석
김영진, 정성윤, 정용진 (광운대)

Real-time Human Object Segmentation in Video Sequences Using a Spatio-Temporal Watershed Transform
김지수, 이태호, 이혁재 (서울대)

생체신호의 특징점 검출 알고리즘과 생체정보 검출 시스템의 구현
손상혜, 정인철, 장영조 (한국기술교육대)

얼굴 검출을 위한 SoC 하드웨어 구현 및 검증
이수현, 정성윤, 정용진 (광운대)

초음파센서와 임베디스 시스템을 이용한 물체인식
김갑성, 문철홍 (광주대)

S13 SIP/SOP related circuits, packaging, process, modeling, and etc. Ⅰ

14:20 ~ 16:00 104호 좌장 : 김부균 교수 (숭실대)

세라믹 시스템모듈의 기술동향 (invited)
김종희 (요업기술원)

SOP구현을 위한 미세라인 회로형성 기술 동향
강남기 (전자소재패키징연구센터)

V band filter using multilayer MCM-D Technology
유찬세, 송상섭, 김동환, 서광석 (서울대)

Embedded PCB 기술의 현황과 응용
조한서, 이두환, 홍종국, 류창섭, 유제광 (삼성전기)

LTCC 다층회로에 구현된 60 GHz RF 단일 집적 송신기
박철순, 정동윤, 은기찬, 송원영, 이영철 (한국정보통신대)

S14 Communication and Network Processor

14:20 ~ 16:00 107호 좌장 : 임혜숙 교수 (이대)

Dual-binary CTC와 Max-Log-MAP을 이용한 터보코덱 구현
공현섭, 박형준, 트롱안, 임웅철, 김진상, 조원경, 김영일 (경희대)

펑처링을 이용한 RC-LDPC 부호기의 하드웨어 설계
박봉수, 이대균, 정봉길, 조용범 (건국대)

Hybrid H-matrix을 이용한 DVB-S2 LDPC 복호기 구조
박재근, 이찬호 (숭실대)

Adaptation Algorithm of Decision Feedback Equalizer with First Post-Cursor Cancellation for Backplane Serial Links
이기혁, 최우영 (연세대)

FFT를 기반으로한 반송 주파수 추정기 구현
지미옥, 이승준 (이화여대)

Adaptation Algorithm of Decision Feedback Equalizer with First Post-Cursor Cancellation for Backplane Serial Links

Ki-Hyuk Lee and Woo-Young Choi
Dept. of Electrical and Electronic Engineering, Yonsei University
Seoul, Korea 120-749
Email: kyuk2@yonsei.ac.kr

***Abstract*- In multi-gigabit per second systems, due to speed limitation, decision feedback equalization with first post-cursor cancellation can cause additional pattern dependent jitters with conventional LMS adaptation algorithm. Combining LMS algorithm and edge equalization, effects of first tap feedback delay is relieved and more compromised timing and voltage margin is obtained. The result is verified through behavioral simulation.**

I. INTRODUCTION

As the demand for higher data throughput increases, the demand for the I/O speed between chips or systems as well as the core speed is growing faster. However, one of the major obstacles of the high speed data links is inter-symbol interference (ISI) which is caused by frequency dependent loss of the channel. ISI induces extracted clock jitters and reduces data decision margins causing higher bit error rate. To mitigate these deteriorations, many equalizing techniques like pre-emphasis, receiver-side continuous-time filter and decision feedback equalizer (DFE), are applied to the high speed backplane transceivers. Among these, decision feedback equalizer has advantages of that it does not boost noise and crosstalk compared to receiver-side continuous-time filter and does not need an extra back channel for adaptation compared to pre-emphasis circuits [1-4]. However, because of speed limitation, many DFE circuits suffer from large decision feedback delays and employ loop-unfolding or speculative techniques to mitigate them, which introduce unwanted loading in signal and clock path and complicate the clock and data recovery circuit design [1-3]. This paper presents the problem of a simple DFE structure with a direct first tap cancellation using conventional least mean square (LMS) algorithm and introduces other adaptation algorithms, edge equalization and joint of them to relieve the feedback delay problem.

II. DFE AND TIMING CONSTRAINT

Fig. 1 shows a system model of receiver equalizer for behavior simulation. It is composed of feed-forward equalizer (FFE) for partial boosting gain instead of transmitter pre-emphasis, variable gain amplifier (VGA) to control low frequency gain, decision feedback equalizer with one tap decision feedback for first-post cursor cancellation, digital adaptation circuit to control the dc gain and equalizer tap weights and clock recovery circuit. All of the blocks are composed of sub-components and simulated with CPPSIM.

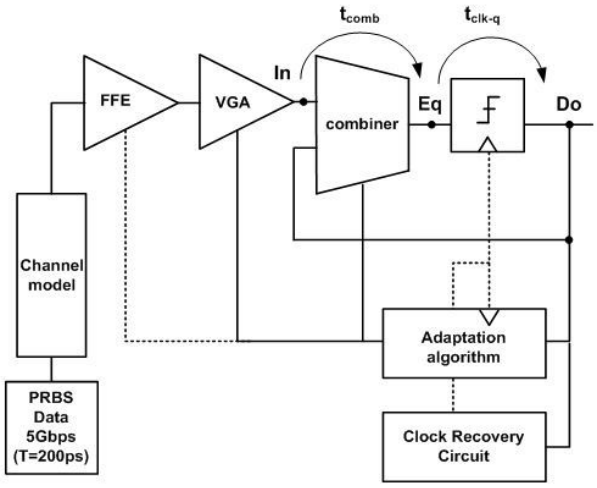


Fig. 1. System model for behavior simulation

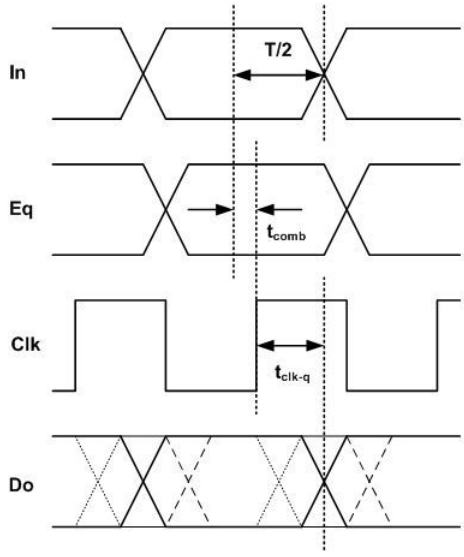


Fig. 2. Timing diagram of data signal in a decision feedback circuit.

Critical timing path in decision feedback are shown in Fig.1 and the timing diagrams of the data signals are in Fig. 2. Propagation delays of the combiner and the decision circuit

are noted by t_{comb} and t_{clkq}, respectively. Usually t_{clkq} dominates total delays of the decision feedback and a strong

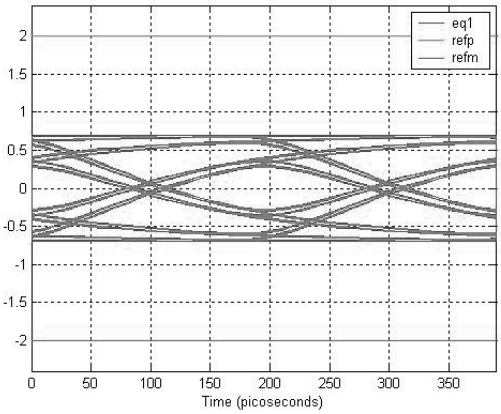


Fig. 3. Input signal eye diagram with ISI after feed forward equalizer

function of the input signal amplitude. They should satisfy the following timing constraint for the properly equalized eye.

$$t_{comb} + t_{clkq} \le T/2 \qquad (1)$$

The gain of the feed forward equalizer is set to the fixed value and the dc gain of the variable gain amplifier is controlled by LMS algorithm for each adaptation algorithm. Fig. 3 shows data eye diagram after feed forward equalizer, which is partially compensated by FFE and still has ISI.

III. ADAPTATION ALGORITHM OF DFE

A. LMS algorithm

The Least Mean Square algorithm is the most popular algorithm which minimizes mean square error at the center of the received eye.

$$C_k^{n+1} = C_k^n - \mu \cdot sign[e_n(t)] \cdot sign[r_n(t+kT)]\Big|_{t=nT} , \qquad (2)$$

where

$$e_n(t) = r_n(t) - d_n(t) \qquad . \qquad (3)$$

C_k^n represents the tap coefficient where k is a tap number and n is an update index. $r_n(t)$ is received signal and $d_n(t)$ is reference signal level. μ is a programmable update magnitude. Convergence of the tap weights over time and the equalized eye diagram after convergence are shown in Fig. 4. c0 is the weight of dc gain and controls the VGA before the combiner. c1 is the tap weight of the decision feedback for the first post-cursor ISI. Eye diagram in Fig. 4 is the results after convergence when the delays of the feedback, tcomb and tclkq, are 30ps and 80ps. Because of the large feedback delay and finite slew rate, eye diagram after convergence has another form of pattern dependent jitter although vertical voltage margin at the center of the eye is optimized to the reference voltage level.

B. Edge equalization

For edge or jitter equalization, full rate clock or quadrature half rate clock is needed to sample the data transition edge. Then two data edge samples in two consecutive data transition are used to decide if the signal is under-equalized or over-equalized [4, 5]. Fig. 5 shows the convergence of the tap coefficients and the equalized eye diagram with the same propagation delay of the decision feedback using the algorithm after the convergence. As the error is sampled at the data transition edge, the tap coefficient is optimized for minimum jitter and the eye diagram shows very low jitters. However, the voltage margin at the center of the eye does not improve much compared to the LMS algorithm.

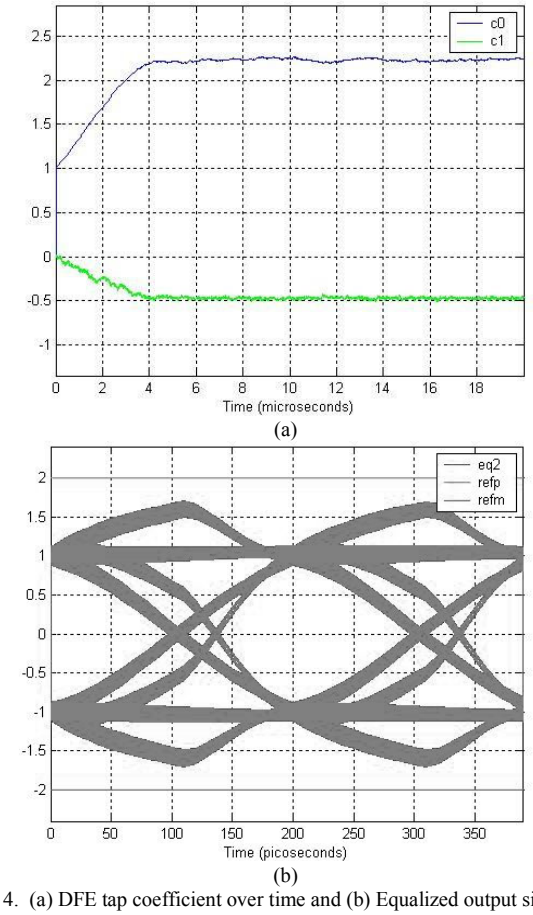
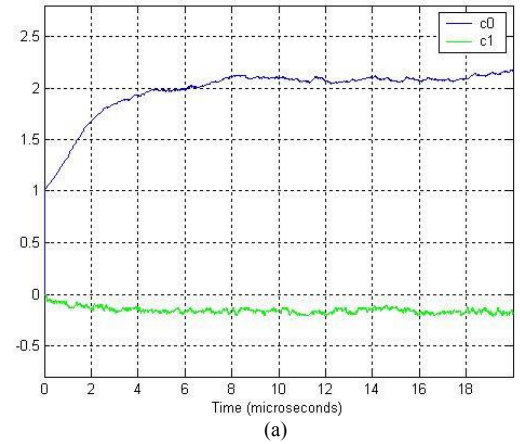


Fig. 4. (a) DFE tap coefficient over time and (b) Equalized output signal eye through conventional LMS algorithm.



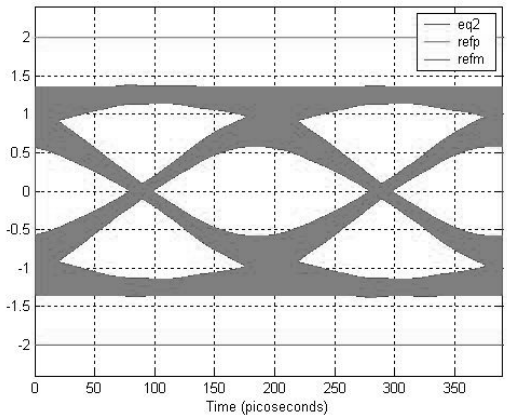


Fig. 5. (a) DFE tap coefficient over time and (b) Equalized output signal eye with edge equalization algorithm.

C. *Joint adaptation algorithm*

Alternatively iterating the tap coefficients with LMS algorithm and edge equalization algorithm, timing jitter and voltage margin can be compromised [5]. Fig. 6 shows the tap coefficients and equalized eye diagram with joint adaptation method at the same conditions. Both voltage margin and timing jitter are improved compared to input signal, although they are not the optimum value.

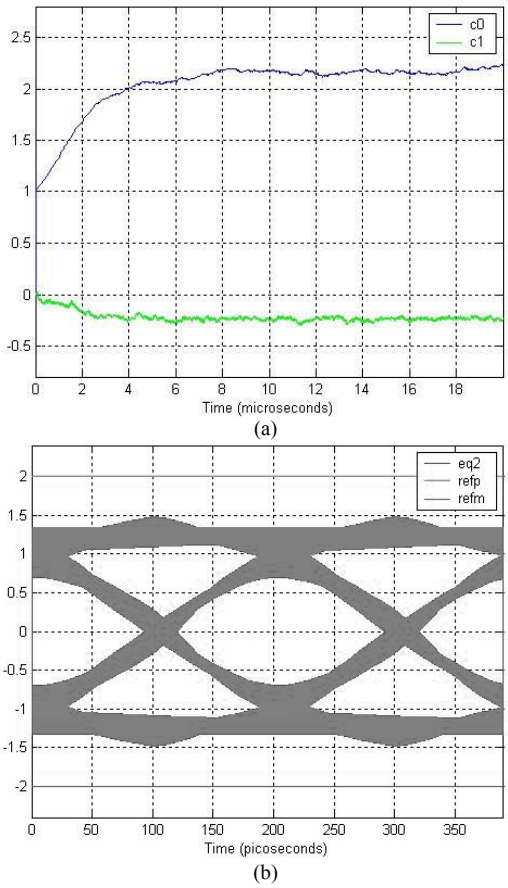


Fig. 6. (a) DFE tap coefficient over time and (b) Equalized output signal eye with joint adaptation algorithm

IV. DISSCUSSION

Fig. 7 shows timing jitter and voltage margin for each adaptation algorithm depending on the total decision feedback delay, $t_{comb}+t_{clkq}$. As LMS algorithm is optimized to minimize the magnitude error at the center of the eye, voltage margin is almost constant for the different delays. However, timing jitter increases greatly as the decision feedback delay increases. On the other hand, for edge equalization algorithm, timing jitter does not increase much for a large feedback delay, but voltage margin is greatly degraded. Thus, at the speed limitation, it is necessary to consider a tradeoff between the timing margin and the voltage margin and to choose the coefficient adaptation algorithm. In the application of a large crosstalk and noise, voltage margin is also important as much like timing jitter for clean recovery clock. Thus, in the large process and temperature variation, at the speed limitation, the joint adaptation algorithm will shows compromised and robust performance for the decision feedback equalizer with first post-cursor cancellation. Although above results are obtained for one tap decision feedback, it can be applied to the equalizer which has many taps, because a first post cursor feedback is usually dominant in the inter-symbol interference and is at the edge of process speed.

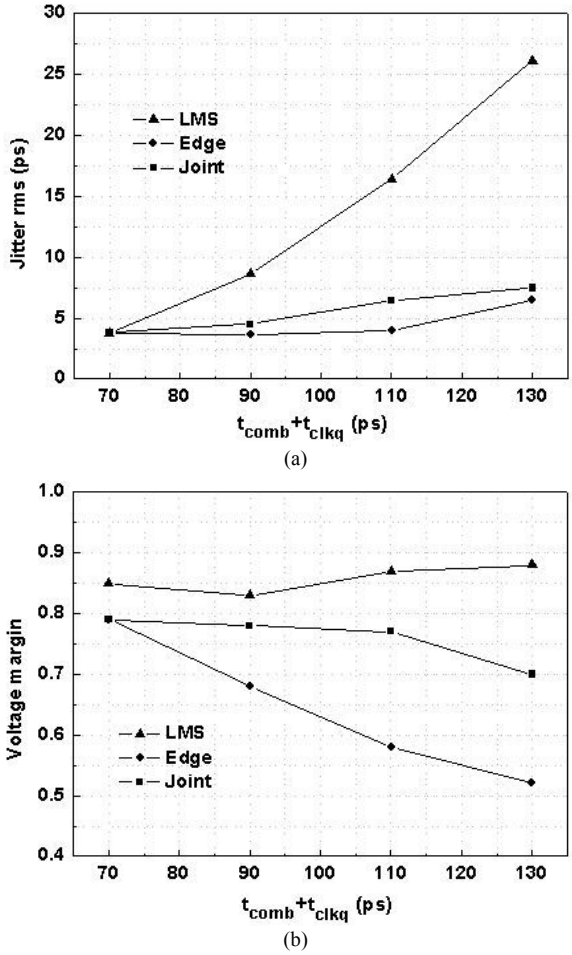


Fig. 7. (a) RMS jitter and (b) voltage margin of equalized signal varying the decision feedback delay for each adaptation algorithm

V. CONCLUSION

In high speed serial links, it is difficult to meet the feedback delay requirement for decision feedback equalizer. Through the behavior level simulations, it is confirmed that large timing delay causes large pattern dependent jitters when the tap weights are adapted according to the LMS algorithm. It can be relieved with the other adaptation algorithm like edge equalization with little voltage margin improvement. Joint adaptation algorithm combining both of them can obtain more compromised results with timing jitter and voltage margin.

ACKNOWLEDGMENTS

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