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30. 1-Gb/s CMOS Low-Voltage Differential Signaling Receiver and Fail-Safe Circuit for Display Applications

Kwang-Chun Choi, Pyung-Su Han, Woo-Young Choi, Department of Electrical and Electronic Engineering, Yonsei University

1-Gb/s CMOS Low-Voltage Differential Signaling Receiver and Fail-Safe Circuit for Display Applications

Kwang-Chun Choi **Pyung-Su Han** **Woo-Young Choi**
Department of Electrical and Electronic Engineering
Yonsei University
Seoul, Korea.
c3kc@tera.yonsei.ac.kr

Abstract – *1-Gb/link Low-Voltage Differential Signaling (LVDS) receiver is designed. It provides the rail-to-rail input range and high gain up to 1-Gb/s data rate. Fail-safe circuit, consisting of pull-up resistors and a comparator, can detect failure state of link such as open, tri-stated, or shorted line. Designed the circuits were fabricated using 0.18-μm CMOS technology.*

Keywords: CMOS integrated circuit, LVDS, low-voltage differential signaling, fail-safe, display application

1 Introduction

High definition flat panel displays are very common nowadays. Consequently data channels between graphic data sources and display panels require very wide bandwidth usually exceeding several Gb/s.

Low-voltage differential signaling (LVDS) standard [1] is a very attractive solution for high-speed I/O interface application because of its high throughput, low EMI, and low power consumption.

In this paper, LVDS input buffer design for display interface is presented. LVDS input buffer is implemented with Baze's amplifier [2] for the input stage and high-gain differential amplifier for the gain stage. Baze's amplifier provides rail-to-rail input common mode range. The high-gain amplifier gives large gain and full-swing CMOS logic level output signal.

The Fail-safe circuit monitors LVDS link, and it detects link failure to prevent consequent malfunction. For example, when LVDS cable is detached, or the signal line is broken for some reason the receiver will see noise signals captured by the cable. Designed as high-gain amplifier, LVDS receiver will amplify the noise to generate logic level signals. To prevent this, LVDS receivers for display application must include the fail-safe circuit [3].

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All circuits are implemented in a 1.8-V 0.18-μm CMOS technology. The interface is simulated up to 1Gb/s NRZ signal with pseudo-random bit sequence (PRBS).

2 Schematics of circuits

2.1 LVDS input buffer

Fig. 1 shows designed LVDS input buffer circuit.

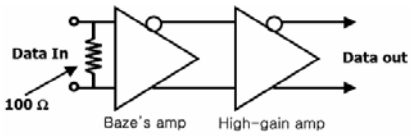

Figure 1. LVDS input buffer

Baze's ampilfier is used for the first stage. Fig. 2 depicts schematic of Baze's ampilfier.

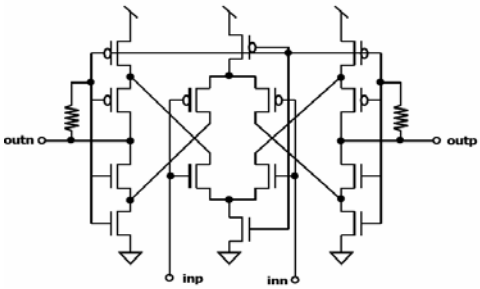

Figure 2. Baze's amplifier [2]

It utilizes NMOS and PMOS differnetial pair to provide rail-to-rail input range. Its self-biased scheme makes circuit structure very simple [2].

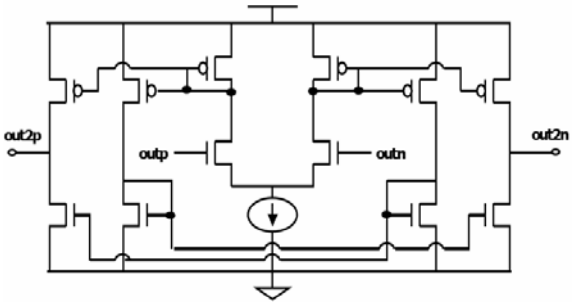

Figure 3. 2-stage mirrored differential OTA

Fig. 3 shows two-stage high-gain amplifier schematic. This architecture is of common knowledge.

2.2 Fail-safe circuit

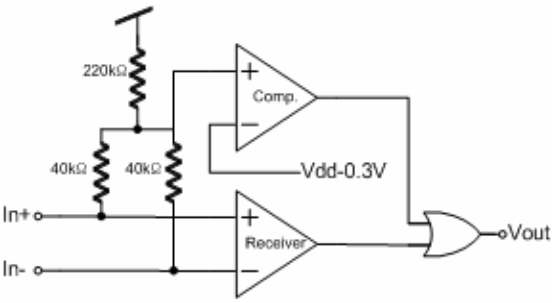

Figure 4. Pull-up resistor fail-safe circuit. [3]

Fail-safe circuit is shown in fig. 4. When either of 'In+' and 'In-' is open or tri-state for channel failure, the input terminal voltage is pulled-up to Vcc through the 220KΩ resistor. The comparator detects pull-up and prevents meaningless noisy output by making 'Vout' high. This process requires small delay to be done. However the delay can be controlled by adjusting output resistance and capacitance at the node to be pulled-up.

3 Chip Layout

Designed chip is implemented in 0.18-μm CMOS process. Fig. 5 shows prototype chip layout.

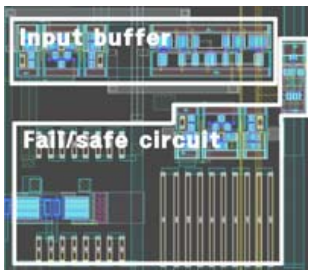

Figure 5.LVDS receiver layout.

4 Simulation results

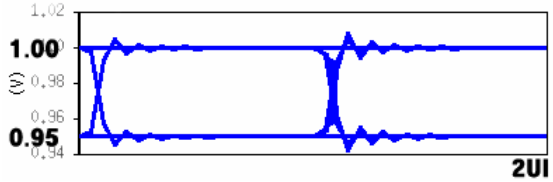

Figure 6 (a). Input eye-diagram @ 1-Gb/s

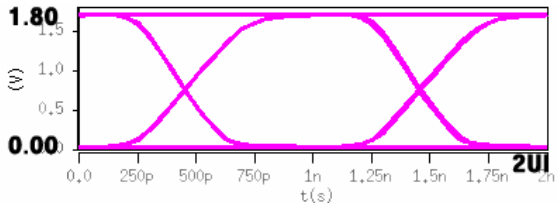

Figure 6 (b). Output data eye-diagram : 1-Gb/s

To confirm the LVDS input buffer, simulation is done. Fig. 6 (a) shows input data eye-diagram of LVDS input buffer and Fig. 6 (b) shows output data. We can see that output swing is large even though input swing is very small. Furthermore designed input buffer shows the same behavior when input common-mode voltage is low or high.

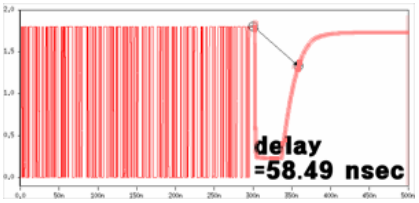

Figure 7. Output of receiver with shorted line

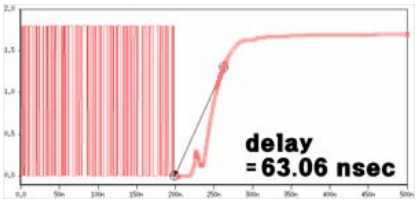

Figure 8. Output of receiver with tri-stated line

Fig. 7 and 8 show behavior of the fail-safe circuit. When input fails, output of the receiver become high after some delay about 60 nsec.

5 Conclusions

LVDS input buffer and fail-safe circuits were designed, and their operation was verified by SPICE simulation. Designed LVDS receiver can operate up to 1Gb/s. Fail-safe circuit sucessfully detected channel failure in simulation. Prototype chip is being fabricated with 0.18μm CMOS technology.

The characteristics of designed LVDS receiver is summarized in Table. 1.

Table 1. Characteristic of LVDS receiver

Supply voltage	1.8V
Data rate	1-Gb/s NRZ
DC gain	51.9dB
Power consumption	10.95mW
Maximum delay to detect failure state	80 nsec
Cell size	0.016 mm^2

References

[1] IEEE Standard for Low-Voltage Differential Signaling (LVDS) for Scalable Coherent Interface (SCI) , 1596.3 SCI-LVDS Standard , IEEE Std. 1596.3-1996, 1994.

[2] M. Bazes, et al. "Two Novel Fully Complementary Self-biased CMOS Differential Amplifiers", IEEE J. Solid-State Circuits, vol. 26, pp165-168. Feb, 1991.

[3] http://www.industrialcontroldesignlin.com/howto/175004696, Understanding LVDS Fail-Safe Circuits.