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1.25/2.5-Gb/s Dual Bit-Rate Burst-Mode Clock Recovery Circuit Using Gated-Oscillators

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Abstract - *A burst-mode clock recovery circuit with a novel dual-mode structure is presented. It utilizes two gated-oscillators to align recovered clock edges to data. It can operate in double data-rate mode in which both rising and falling edges of recovered clock are used. To enable this, gated-oscillator reset-phase control scheme is introduced to switch the starting phase of gated-oscillator dynamically between 0° and 180° according to current clock phase. A prototype chip was designed with 0.18μm CMOS technology, whose 1.25/2.5-Gb/s dual-mode clock recovery operation is successfully verified by SPICE simulation.*

Keywords: Burst mode, Clock recovery, Gated oscillator, Multi bit-rate.

1. Introduction

In burst-mode transmission systems, fast clock-acquisition is very important so that preamble bit sequence can be minimized and transmission throughput maximized. Various circuit techniques and clock recovery schemes [1] [2] have been proposed for achieving it. Among them, gated-oscillator approach [1] provides simplest structure with instantaneous locking characteristics. It is especially attractive for such burst-mode applications as LAN (Local Area Network) and PON (Passive Optical Network) in which jitter accumulation is not a major problem [3] since they are used for short-distance transmission and, consequently, do not require repeaters. All-pass characteristics of gated-oscillator-based clock recovery scheme allow tracking of jitters of all frequency, resulting in decent jitter tolerance up to very high frequency. [4].

Frequency mismatch between gated-oscillators limits maximum run-length of CID (Consecutive Identical Digit) that clock recovery circuit can process. Typically, frequency mismatches around two or three percent of operation frequency [5] are observed in standard CMOS technology. This problem can be relieved by using run-length limiting coding scheme such as 8b10b code which offers maximum CID run-length of 5bits [4].

Recently published gigabit rate PON standards (GPON and EPON) [6] [7] support 1.25-Gb/s per burst-mode transmission and it is expected to be doubled to 2.5-Gb/s in near future. Therefore, dual bit-rate clock recovery circuit that can support both 1.25-and 2.5-Gb/s can be very useful. In this paper, we presented a novel burst-mode clock recovery circuit which can operate in half-rate clocking mode, doubling its operation speed, as well as in conventional full-rate clock extraction mode.

2. Gated-oscillator based clock recovery

Gated-oscillator based clock recovery scheme was originally published in 1954 for clock generation of magnetic drum data storage [8]. After that, PLL (Phase-Locked Loop) and SAW (Surface Acoustic Wave) filter based clock recovery schemes, which can offer good jitter suppression, became dominant among long-haul, high-speed data transmission applications. Nowadays, however, it is used in burst-mode systems and in multi-channel receivers in which many receivers should be integrated on a single chip [9], because it can provide small-size and low-power consuming clock recovery circuits.

Fig. 1 shows schematic diagram of a gated-oscillator. A logic ‘gate’ is inserted in a ring oscillator to turn on and off its oscillation. When the gate is closed, or ‘Enable’ is low, the clock edge circulating in the ring oscillator is blocked by the gate stage and the oscillation stops.

The gated-oscillator in Fig. 1 has only one stable state when ‘Enable’ is low, that is with high ‘Out’. In this state, the oscillator is ready to be triggered. By setting ‘Enable’ to high, the oscillation can be resumed. An important observation here is that the oscillation is always triggered off with ‘Out’ signal going to low. That means we can set the output clock phase to a certain value, in this case, falling edge, whenever we want to do so by controlling ‘Enable’ signal.

Gated-oscillator based clock recovery utilizes this property to align clock signal to data bits. Fig. 2 depicts a gated-oscillator based clock recovery circuit example.

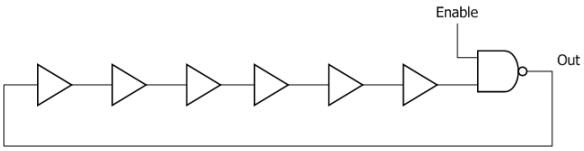

Figure 1. Schematic diagram of a gated oscillator

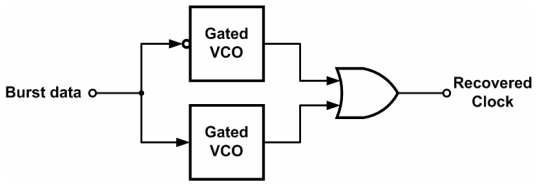

Figure 2. Gated-oscillator based clock recovery circuit

Two gated-oscillators are turned on and off alternately according to 'Burst data' to generate clock signal synchronized to data. They are tuned to the data rate clock frequency by sharing the VCO (Voltage Controlled Oscillator) control voltage of reference PLL which is locked at reference clock frequency. When 'Burst data' is high (logical one), the lower gated-oscillator is activated and generates clock, and when 'Burst data' is low (logical zero) and the upper one is activated and generates clock. Therefore each gated-oscillator covers half portions of 'Burst data'. Two half portions of clock are combined by an OR gate to generate complete clock signal. This operation is shown in Fig. 3.

3. Half-rate clock recovery

Half-rate clocking or DDR (Double Data Rate) scheme became very popular recently, especially for high-speed memory I/Os. It uses both rising and falling edges of clock signal to relieve device speed requirements.

As described in section II, gated-oscillator based clock recovery scheme utilizes clock-phase-reset-ability of gated-oscillator. Let us assume that the gated-oscillator clock recovery circuit shown in Fig. 2 has clock phase set to 180°, or rising edge, at every data transition. Then the opposite clock phase (0°), or falling edge can be used for data sampling.

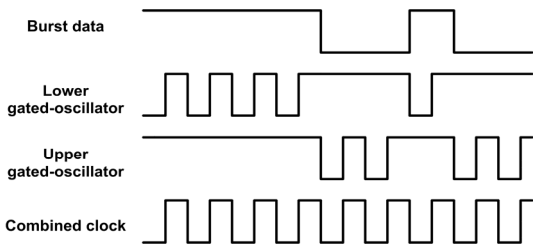

Figure 3. Clock recovery operation using a gated-oscillator pair

In half-rate clock recovery, since both rising and falling edges are used, it should be possible to set gated-oscillator phase to 180° (rising edge) or 0° (falling edge) according to the clock phase. In our design, a modified version of gated-oscillator as shown in Fig. 4 is used to enable half-rate clock operation.

Gated-oscillator in Fig. 4 uses two MUXs for its gate stages (their selection signal, used as 'Enable', is not shown in the figure). It has four stable states when deactivated, in contrast to the conventional one having only one. Combination of R0 and R1 can select one among them. The logic values of the output terminal of the gate stages are arranged by R0 and R1 during stable states. Therefore R0 and R1, called 'reset value', can select the starting phase of gated-oscillator because they are indeed the very output value O0 and O1 would have just before the oscillation starts.

Because the clock edges are to be aligned to data transition, delayed version of clock signal (O0d) should be used for data sampling in half-rate mode. After clock MUX (explained later), the total amount of delay of extracted clock is exactly a quarter of clock period (a half of bit period), giving the optimal chance for data sampling.

Fig. 5 shows clock phase definition used in this design and four possible reset phase. For example, if we make both R0 and R1 high (logical one), the gated-oscillator makes its output start at 0°. If we use low (logical zero) for R0 and R1, the oscillation will start at 180°.

A half-rate clock recovery circuit was built with the modified gated-oscillator and is depicted in Fig. 6. R_a and R_b, should be changed dynamically to make sure the gated-oscillator to oscillate half-rate frequency. This problem can be solved by using the activated one's output clock, O0, as 'reset value' of the other. This make the clock phase of oscillator can set its clock phase to 0° or 180° properly.

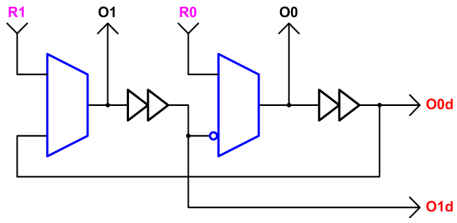

Figure 4. Modified gated-oscillator for half-clock recovery

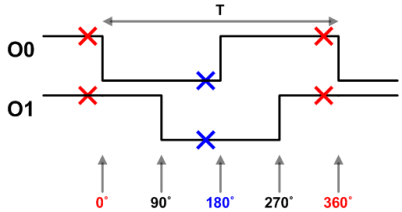

Figure 5. Clock phase definition

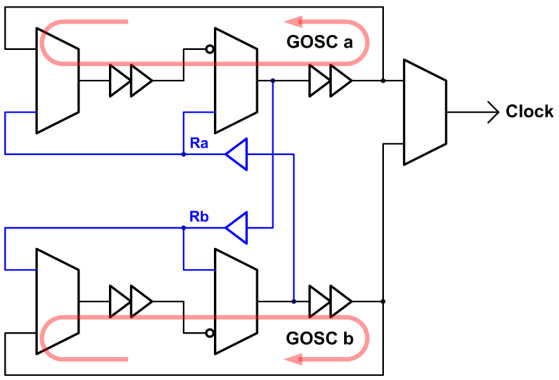

Figure 6. Half-rate clock recovery circuit

Half portions of clock signals are combined by clock MUX, instead of OR gate. OR gate cannot be used for clock combining in half-rate mode, because although when a gated-oscillator is deactivated, it would make some fake clock due to continuously changing reset value. This fake clock is screened out by the clock MUX. But in functionality, an OR gate and a MUX play the exactly same role.

4. Dual bit-rate operation

Modified gated-oscillator in Fig. 4 also can be used for full-rate clock recovery by fixing reset value to a constant logic value, e.g. logical high. Then it operates the same as the conventional one shown in Fig. 1, although it can settle faster owing to the additional gate stage (two MUXs) when the 'Enable' turns off the oscillation.

By utilizing this programmability of reset phase, the clock recovery circuit shown in Fig. 6 can be used for full-rate clock recovery as well as half-rate clock recovery. In circuit design, it was implemented by adding two MUXs with a constant value on their one input (not shown in Fig. 6) in reset value path. They are controlled by external mode-selection signal.

5. Simulation result

Clock recovery circuits described so far and a replica PLL for frequency tuning were designed with 0.18μm CMOS technology, and its functionality was verified by SPICE simulation.

Fig. 7 shows 1.25-Gb/s input bit stream, recovered clock signal and retimed data bits when it operates in full-rate clock recovery mode. MATLAB-generated random bit sequence was used for data input.

Fig. 8 shows 2.5-Gb/s input bit stream, recovered half-rate clock signal, data sampled at rising edges and falling edges when it operates in half-rate clocking mode.

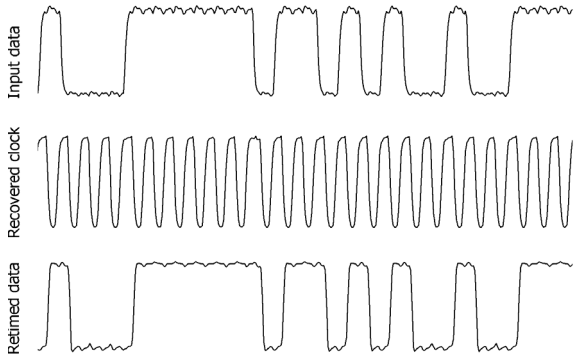

Figure 7. Input data, recovered clock and retimed data waveforms from 1.25-Gb/s full-rate clock recovery simulation

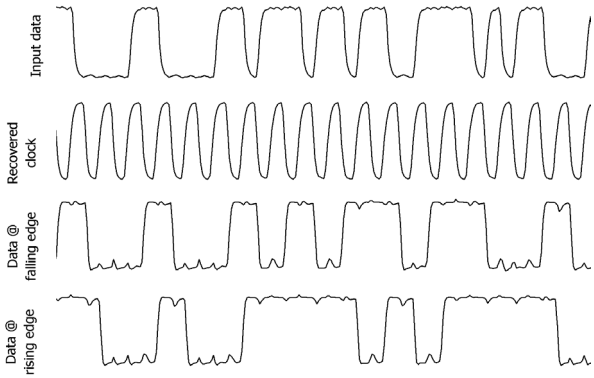

Figure 8. Input data, recovered clock and retimed data waveforms from 2.5-Gb/s full-rate clock recovery simulation

PWD in recovered clock waveform after several CIDs was observed. It was caused by clock phase drift due to frequency mismatch between clock-recovering gated-oscillators and replica oscillator in PLL and would result in deterministic jitter. 0.18UI and 0.21UI of peak-to-peak deterministic jitter were estimated for each of 1.25-Gb/s and 2.5-Gb/s operation by the simulation results, when maximum run-length of CID was 5bits. Data bits were correctly retimed because enough timing margin for data-sampling is secured even with this amount of jitter.

6. Prototype chip and measurement result

Fig. 9 is microscopic photograph of fabricated prototype chip. Clock recovery core occupies only 160μm x 250μm and replica PLL requires 310μm x 250μm.

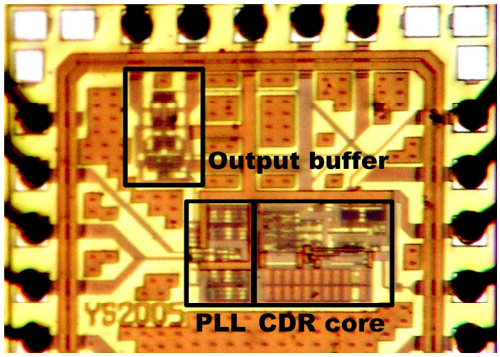

Figure 9. Layout of the the prototype chip

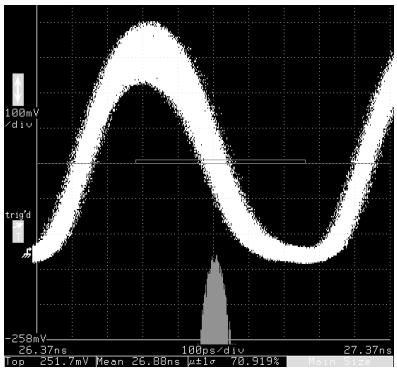

Figure 10. Recovered clock from 1.25Gbps 2^7-1 PRBS

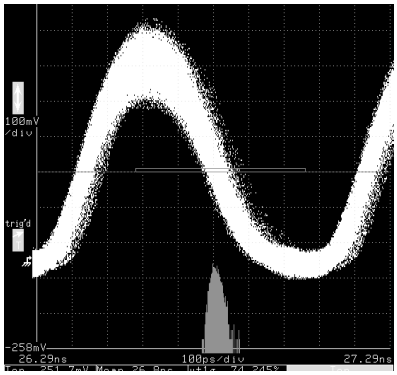

Figure 11. Recovered clock from 2.5Gbps 2^7-1 PRBS

Figure 10 and 11 show recovered clock waveforms from 2^7-1 PRBS pattern at 1.25Gbps/2.5Gbps each. Because data source is virtually free from jitter, observed peak-to-peak jitter of around 100ps was purely from clock recovery circuit itself.

Figure 12 shows burst-mode operation of prototype chip. Intentional phase drift were made by substitution of PRBS patterns by 55bits of 0's. Instantaneous phase alignment operation was observed at the end of stuffed 0's where following data transition occurred.

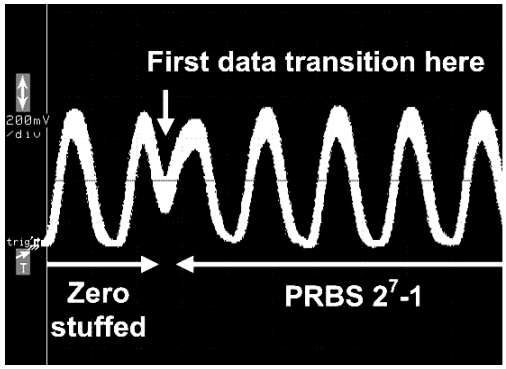

Figure 12. Instantaneous phase alignment

7. Conclusions

A novel structure of burst-mode clock recovery circuit was proposed. It can operate in half-rate clock frequency mode, which doubles the operation speed, as well as full-rate clock recovery. The two operation modes can be switched simply by external selection signal. Proposed circuit was designed with 0.18μm CMOS technology and prototype chip was fabricated.

Some PWD was observed in simulation, which was caused by clock phase drift due to frequency offset between oscillators in clock recovery circuit and replica PLL. This problem can be mitigated by using limited-CID coding scheme, e.g., 8b10b code that limits maximum run-length of CID to 5bits. In prototype measurement, PRBS 2^7-1 pattern was used which has maximum run length of 7bit. Prototype chip successfully recovered full-rate and half-rate clock from each 1.25Gbps and 2.5Gbps PRBS patterns.

Table 1 sums up the measurement result.

Table 1. Measurement result summary

Technology	0.18μm CMOS
Data-rate	1.25Gbps/2.5Gbps (dual bit-rate)
Chip area	160μm x 250μm for core 310μm x 250μm for reference PLL
Max. run-length	More than 7bits
Jitter generation	100ps p2p for 1.25Gbps/2.5Gbps
Power supply	1.8V
Power consumption	60mW for core 50mW for Output buffer

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