2005년도 SOC 학술대회

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- : IEEE SSCS/EDS Joint Chapter of Seoul Section
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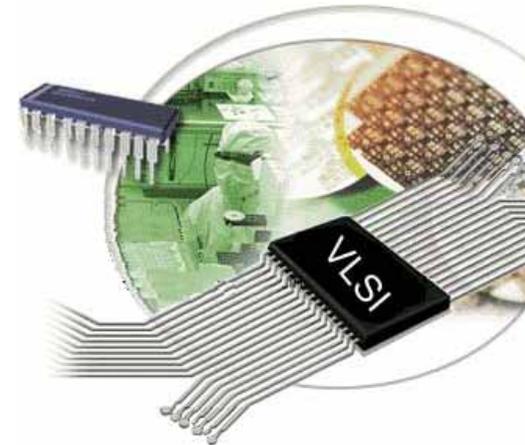
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사단 법인 **대한전자공학회**
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S19	Analog Design Techniques

16:10 ~ 17:30   C031   :   (   )

High Voltage Switch

,   ,   ,   ,   ,   (   )

AC- DC

,   ,   ,   (   )

Bi- CDMOS   Regulator IC

,   ,   ,   (   )

A High Current Driving Charge Pump with Current Regulation Method
Soon- Kyun Shin, Bai- Sun Kong, Chil- Gee Lee, Young- Hyun Jun,
Jae- Whui Kim (Sungkyunkwan Univ)

S20	High Speed Circuit

16:10 ~ 17:30   B031   :   (   )

PLL

,   ,   ,   (   )

**A Low- Voltage and Wide- Range Phase- Locked Loop for
Standard Mobile Imaging Architecture**

,   ,   (   )

1.25Gbps Burst- Mode Receiver Front- End for PON
Ki- hyuk Lee, Woo- Young Choi (Yonsei Univ)

915Mhz   ISO/18000- 6 RFID   PLL

,   ,   (Anyang Univ)

S21	RF Circuit

16:10 ~ 17:30   C033   :   (   )

**A 0.35μm BiCMOS Low Power Direct Conversion Transmitter
with fractional- N frequency synthesizer using a fast AFC
technique for CDMA wireless applications**
Myung- Woon Hwang, Jeong- Cheol Lee, Sungho Beck, Seungyup Yoo,
Kyoohyun Lim, Hyosun Jung, ChangHee Lee, Kyung- lok Kim,
Gyu- Hyeong Cho, Sangwoo Han (KAIST)

**On- chip design of an Auto Focus (AF) driver for mobile
camera applications**

,   ,   ,   ,   ,   (LG   )

UWB   CMOS

Jungwan Park, Sungsoo Choi, Yong Moon (Soongsil Univ)

**A CMOS LC- tank VCO and phase shifting network for direct
conversion receiver of IEEE 802.11a**
Mi- Young Lee, Yong- Hun Kim, Chan- Young Jeong, Changsik Yoo,
Jin- Su Park (Hanyang Univ)

1.25Gbps Burst-Mode Receiver Front-End for PON

Ki-hyuk Lee and Woo-Young Choi

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Abstract – *We presents a design of a compact 1.25Gbps burst-mode optical receiver front-end for passive optical network applications. With fast and accurate threshold detection, fast settling time (25ns) has been achieved at a low supply voltage (1.8V). The receiver achieves the sensitivity of -25dBm and dynamic range of 22dB. The circuit is designed with 0.18μm CMOS technology, occupies 0.4×0.5mm^2 and consumes 80mW.*

Keywords: Burst-mode optical receiver, passive optical network, dynamic range, transimpedance amplifier, and limiting amplifier

1   Introduction

Increasing demand for the high speed access network spurred the development of gigabit-class passive optical networks (PONs) [1-4]. In PON systems, an optical line terminal (OLT) is connected to the multiple optical network units (ONUs) through optical fiber and a splitter as shown in Fig.1. The downstream data from OLT to ONU are transmitted in continuous mode and the upstream data from ONU to OLT are in TDMA burst mode. Because of the different fiber length and power loss, each upstream packet has a large power difference. Therefore the receiver in the OLT must have large dynamic range and short response time to the upstream packets having different power levels.

This paper presents a design of a compact 1.25Gbps burst-mode optical receiver front-end designed in 0.18μm CMOS technology at 1.8V supply with a small chip area and low power consumption.
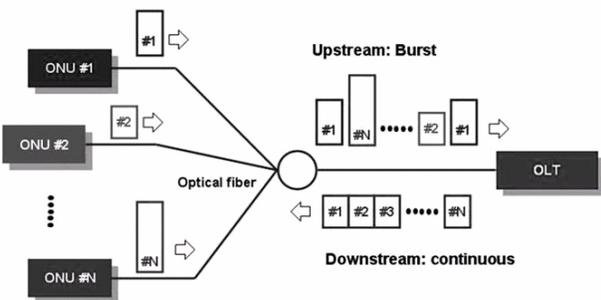
2   Burst-Mode Receiver Front-End

A block diagram of the burst-mode receiver front-end is shown in a Fig.2. It consists of a transimpedance amplifier (TIA) with automatic gain control (AGC), an automatic threshold control (ATC) circuit and a limiting amplifier.
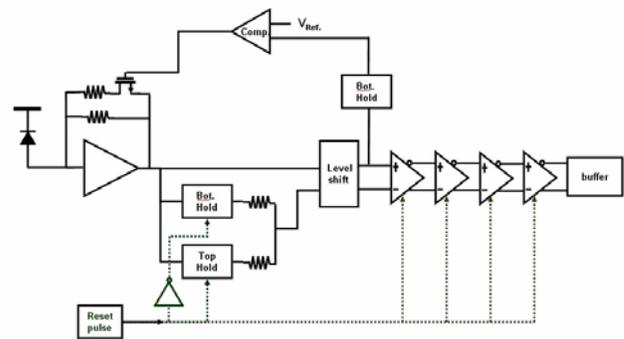

Fig 2. Block diagram of the burst-mode optical receiver

The TIA converts photo-currents from a photodiode into voltage signals. For high sensitivity and wide dynamic range, TIA is made with a single inverter and a large feedback resistor [5]. To relieve the signal distortion in TIA at large current input and achieve a wide dynamic range, we added a smaller resistor and a switch in parallel with the feedback resistor. If the input current reaches a threshold level, the feedback resistance switches to a smaller value. Thus, it suppresses the signal distortion at large current inputs.
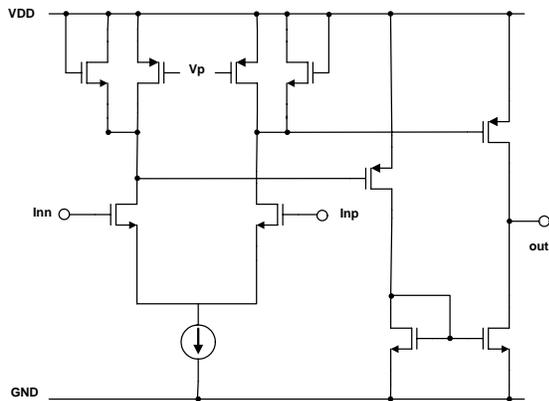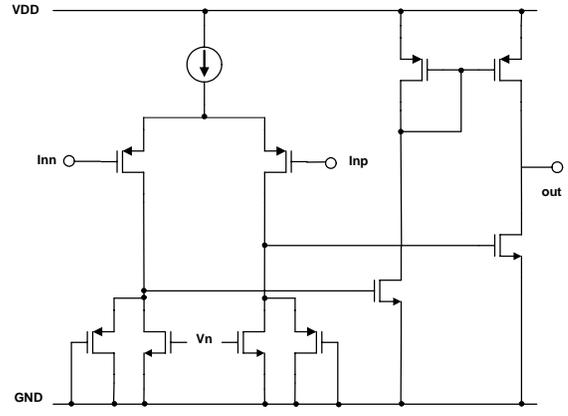

Fig 1. PON systems
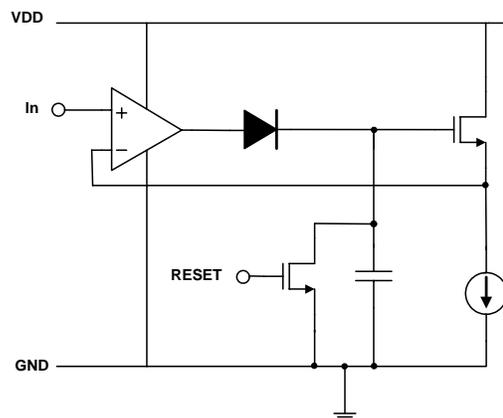
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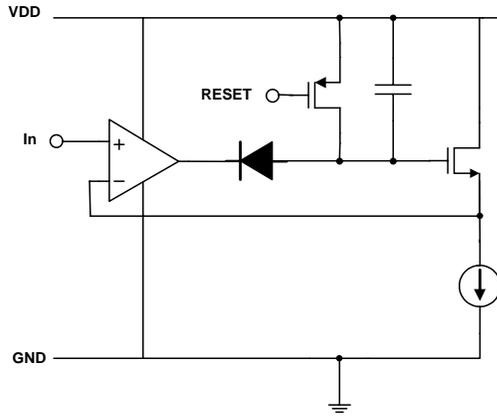
(b)

Fig 3. (a) top hold and (b) bottom hold circuits

(b)

Fig 4. (a) PMOS pair input (b) NMOS pair input differential to single amplifier

In the burst-mode transmission, the threshold voltage or reference voltage must be generated for single to differential conversion and amplification for each packet [2]. We used a top-hold (TH) circuit, a bottom-hold (BH) circuit and a voltage divider with series resistors. The threshold is generated by dividing the voltage between a top level and a bottom level of the TIA output signal. The TH and BH circuits are shown in Fig 3. The input signal is amplified by the main amplifier and rectified by a diode and stored on a capacitor. The hold level is fed back to the negative input of the main amplifier through source follower. The source follower is added to avoid the loading effect of the resistive divider. The MOSFET parallel with hold capacitor discharges the detected voltage level during the guard time with RESET signal. Because the error occurred in the threshold detection results in a long settling time for the small input current, the accurate level detection is needed. In the TH and BH circuits, the gain of input amplifier determines the detection accuracy. Thus, two-stage differential to single amplifiers with PMOS input pair for the TH circuit and NMOS input pair for the BH circuit in Fig 3 are used for large gain.

Because of the limited level detection range of the TH and BH circuits as shown in Fig. 5, the TIA output signal range is tuned by sizing the NMOS and PMOS of the inverter TIA asymmetrically.
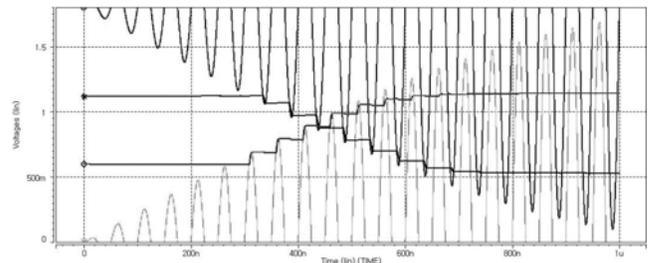

Fig 5. Top and bottom hold circuit detection range

The limiting amplifier receives the voltage signal from the TIA and amplifies it to logic level. To cancel the offset accumulated during the threshold detection and amplification, the feedforward type offset cancellation circuit is added to each gain stage [1, 3]. Four gain cells of Fig 5 are cascaded to obtain the enough gain for the small input currents. The output buffer is designed to have 350mV output swing using current mode logic (CML).
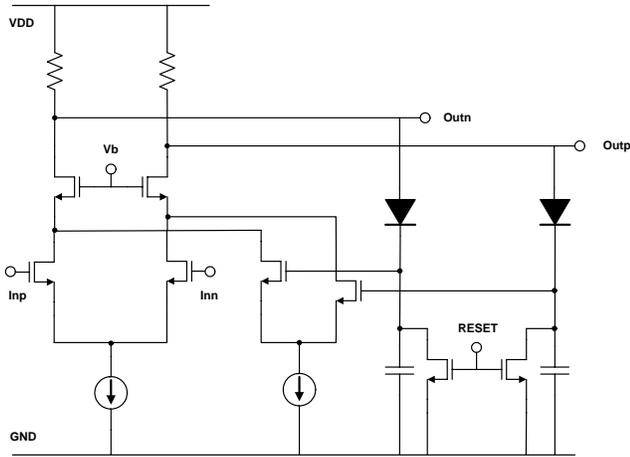

(a)

436

Fig 6. Limiting amplifier with offset cancellation

3   Simulation Result

The whole front-end circuits are designed and simulated in mixed-mode 0.18μm CMOS technology at a 1.8V supply with HSPICE. Assuming the 1pF input capacitance of photodiode, the TIA achieves the transimpedance gain of 2kΩ with bandwidth of 800MHz to optimize the input noise and gain bandwidth. The input referred current noise of the TIA is calculated to be about 200nA. Assuming the responsivity of photodetector is 0.8A/W, the input sensitivity is estimated to be about -25dBm to achieve SNR of 14 for BER<10^{-12}. The maximum overload is -3dBm.
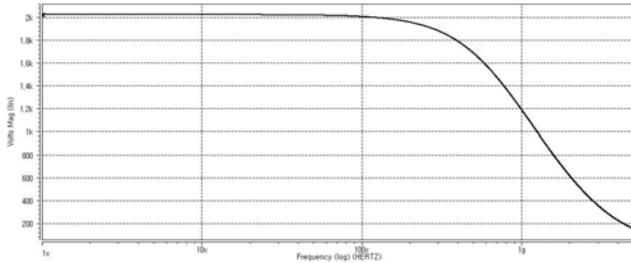

Fig 7. TIA ac response

Fig 8 shows the simulated output waveform for the packet data of different amplitude. The input current of the first data packet is about 4μA corresponding to -25dBm optical input and that of the second one is 570μA corresponding to -3dBm. The detailed output waveforms for the two data packets are shown in Fig 8. (b) and (c). Two limited output signals show the same output voltage of 350mV. In 25ns, the output waveforms settle down to the constant level and it takes shorter time for the larger input currents.
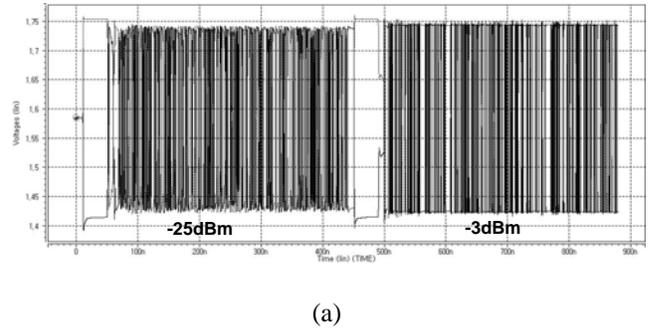
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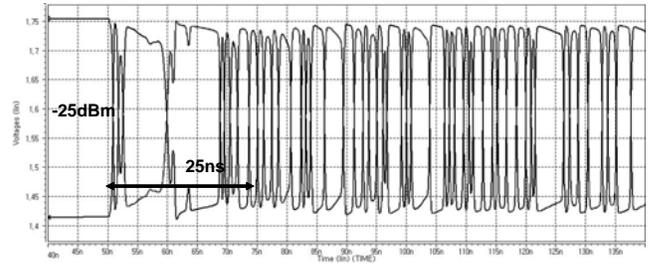
(b)
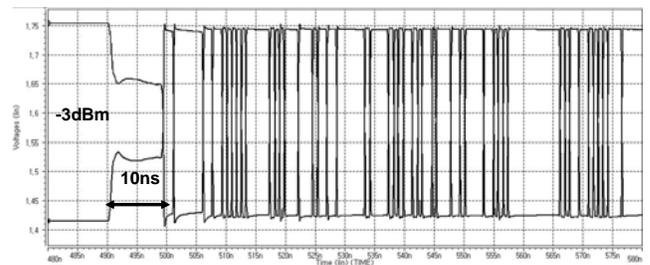
(c)

Fig 8. (a) Simulated output waveform for the (b) -25dBm and (c) -3dBm optical input packets

The power dissipation of the front-end circuit is about 80mW including output buffer. The chip layout is shown in Fig 9. The circuit area is about 0.4×0.5mm^2.

4   Conclusions

.We designed a compact 1.25Gbps burst-mode receiver front-end circuit for PON in 0.18um CMOS technology at 1.8V supply, which satisfies the EPON standards. The circuit shows the minimum sensitivity of -25dBm, the maximum overload of -3dBm and settling time of 25ns. With small area and low power dissipation, the designed circuit can provide a cost effective solution for burst-mode receiver applications.
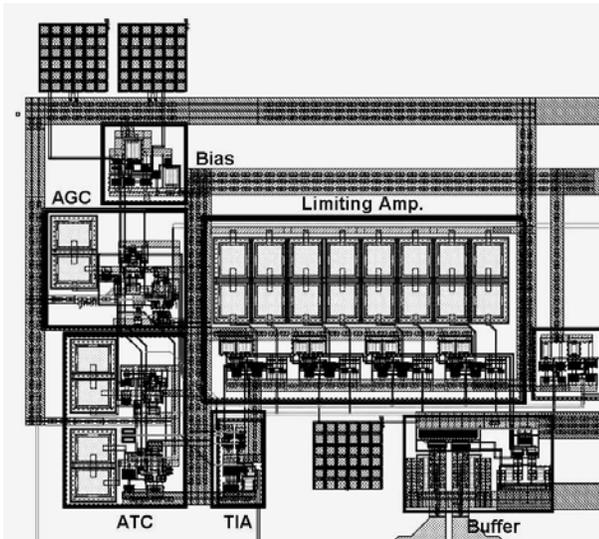
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Fig 9. Layout of the burst-mode front-end circuit

Process	Anam 0.18μm CMOS
Power consumption @ VDD=1.8V	< 80mW (I/O included)
Chip size	0.4 × 0.5 mm²
Sensitivity	-25dBm
Overload	-3dBm
Speed	1.25Gbps
Settling time	~ 25ns

Table 1. Performance summary

Acknowledgment

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