3Gb/s CMOS Adaptive Equalizer for Backplane Serial Links

Jae-Wook Lee and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University
patima@tera.yonsei.ac.kr

Abstract – *A new line equalizer is proposed for the application of backplane serial link. The equalizer is made of digitally controlled feed-forward equalizer (DCFFE), bottom detector, limiting amplifier and control block. The control block is capable of detecting signal shapes and decides the high frequency boosting level of DCFFE. Successful equalization is demonstrated for signals transmitted over 2m long PCB trace (about 10dB loss). The circuit is designed with CMOS 0.18㎛ fabrication process and verified with SPICE simulation.*

Keywords: Adaptive equalizer, analog equalizer, high speed I/O, transceivers, pre-emphasis.

1 Introduction

The need to route the increasing amounts of data traffic has made the backplane a bottleneck in networking infrastructures. Recent efforts to increse data throughput on legacy multigigabit systems face a number of challenges. It is no longer sufficient to solely increse the speed of the ICs to achieve higher data rates. This is due to the emergence of other constraints, specifically signal impairments arising from the transmission media, such as frequency-dependent loss and crosstalk.

In high-rate NRZ data communication over cables or PCB trace, skin-effect resistance causes attenuation of high frequency signal components. However, low frequency signal components are not attenuated, resulting in intersymbol interference(ISI) that limits transmission data rate and distance[1]. A thin strip line with width W has a frequency dependent resistance per unit length as [1]:

$$R(f) = \frac{1}{2W}\left(\frac{\pi \mu f}{\sigma}\right)^{1/2} \qquad (1)$$

where σ is metal conductivity (5.8×10^7 ohms/m for copper). The resistance is proportion to the square root of the frequency and inverse of the linear dimension of the conductor.

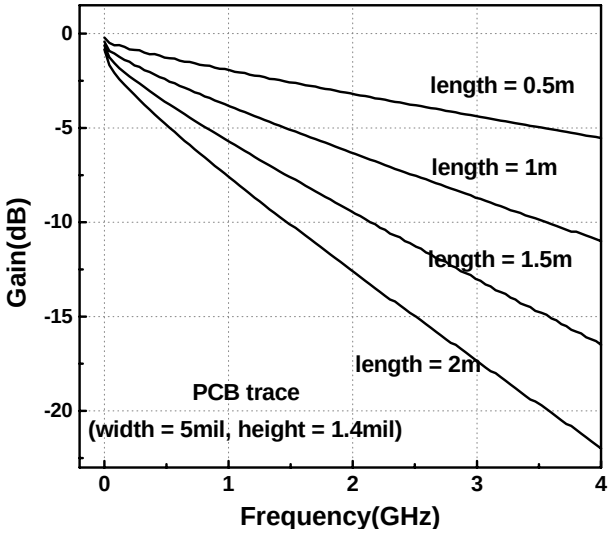

Figure 1. Attenuation curves for 50-ohm strip guided PCB traces.

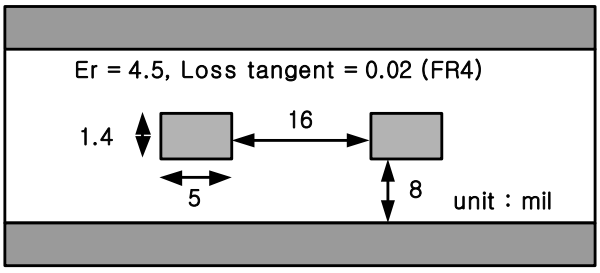

Figure 2. Strip line structure and parameter

Figure 1 shows the calculated attenuation as a function of frequency for a strip guided PCB trace with a differential impedance of Z_0 = 100ohms. The calculation was done for a strip line structure shown in figure 2 with HSPICE W-model. As can be seen in figure 1, attenuation up to 60% of the original signal magnitude per meter can be observed at 1GHz. And the loss of copper traces on FR4 boards is approaching about 10dB at 1.5GHz for 2m length line.

To overcome channel impairments, either pre-emphasis circuit in the transmitter[1,3], equalization in the receiver[2], or a combination of both[4,5] is used. The merit of including receiver equalization is that the equalizer parameters can be adjusted by measuring the quality of the incoming signal to compensate for the process and temperature variation of the signal propagation medium[6].

In this paper, we present a receiver circuit having an equalizer. The equalizer parameters can be adjusted by measuring the envelope and slew rate of equalizer output signal. The equalizer parameters are adjustable to tolerate high frequency signal loss up to 10dB.

2 Equalizer Structure

In order to compensate ISI caused by bandwidth limited channel, an equalizer is designed as a filter whose trasfer function should be set, over an appropriate frequnecy range, equal to the inverse of the connecting cable transfer function. As shown in [7], one can model the cable transfer function as

$$F(s) = \exp(-La\sqrt{s}) \qquad (2)$$

where L is the cable length, and a is a cable-characteristic constant. Therefore, the required equalizer transfer function is given as

$$H(s) = 1 + \alpha G(s) \qquad (3)$$

where, G(s) is the transfer function from a high frequency boost stage and α is adaptively determined gain.

Figure 3 shows our equalizer block diagram. The circuit consists of :

- Digitally controlled feedforward equalizer (DCFFE), which gives variable high frequency emphasis to the input data signal.
- Slicer(Limiter), designed to have controllability of output swing level.
- Bottom detector, which gives control voltage proportion to the DCFFE output signal bottom level.
- Digital control block, which measures the input and output power of slicer and controls the DCFFE boosting gain.

The adaptation loop reaches the steady state when the energy of the DCFFE output signal becomes bigger than that of the slicer.

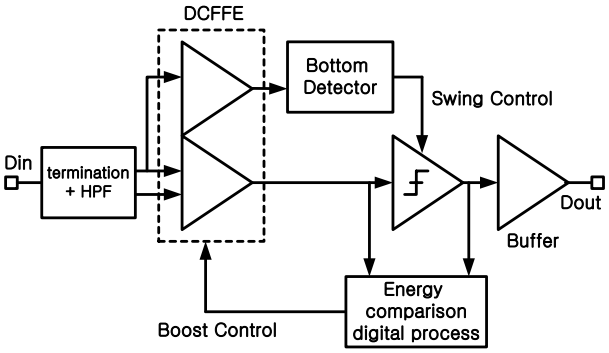

Figure 3. Equalizer Block Diagram

2.1 Digitally Controlled Feed Forward Equalizer

The schematic of the DCFFE, shown in Figure 4, consists of two amplifiers whose gain is tuned with control voltage.

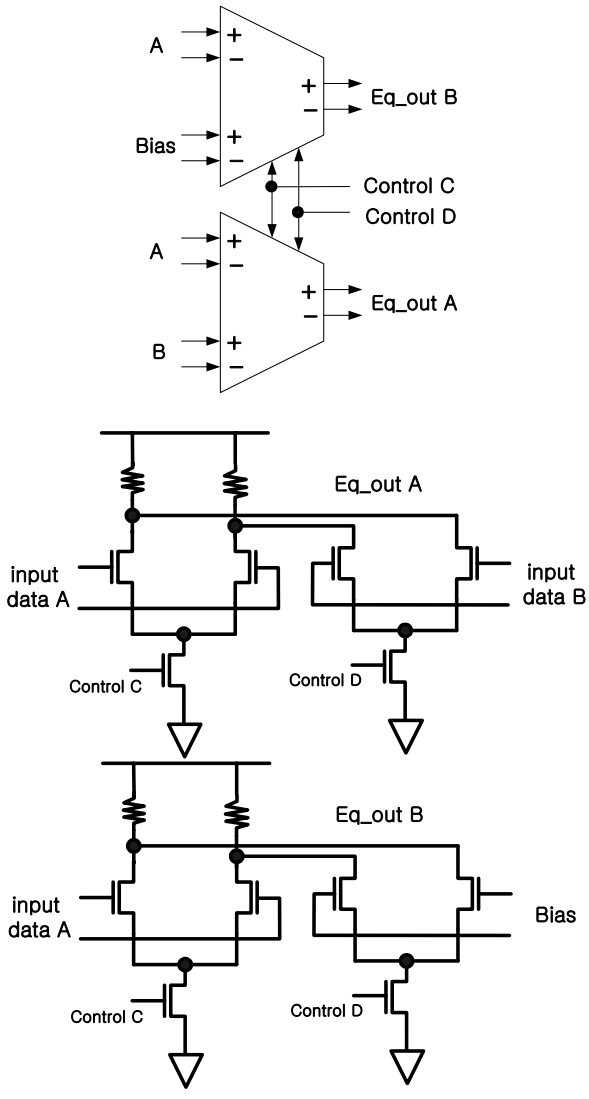

Figure 4. Schematic of DCFFE

The input data A is received signal obtained at termnation and the input data B is obtained at high pass filter(HPF) shown in Figure 5. The frequency response of HPF is shown in Figure 6.

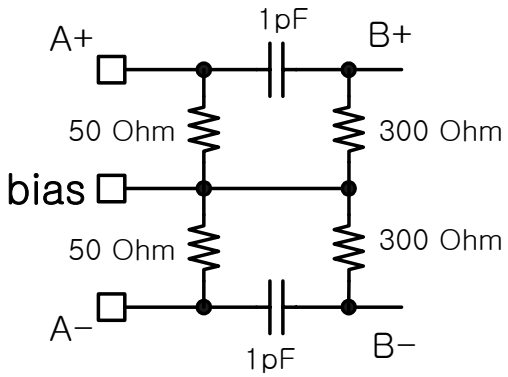

Figure 5. Termination and high pass filter

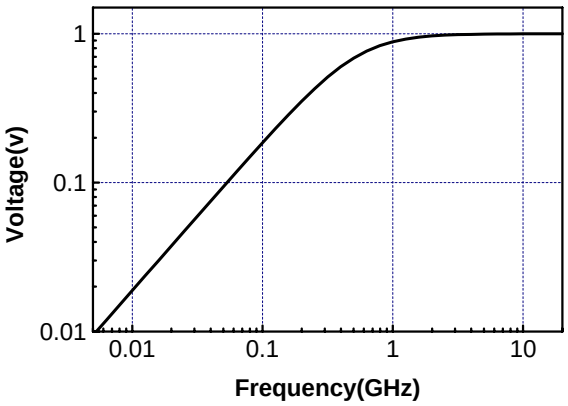

Figure 6. Frequency response of HPF

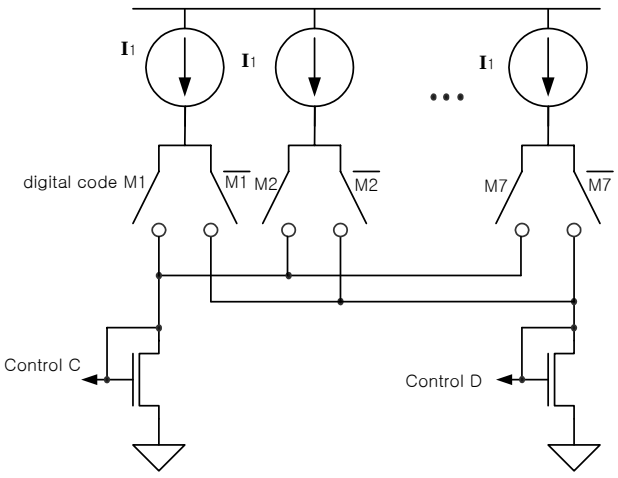

Figure 7. Schematic of digitally controlled bias generator

Eq_out A is weighted sum of two input signals. Control C and D determine the weighting of each signal. And Eq_out B is flat amplified output of input data A. DCFFE has 8 level high frequency boosting gain decided by digital signal. Figure 7 shows digital-to-control-voltage covert circuit. Obtained control C and D guarantee constant tail current sum of DCFFE . Therefore, DCFFE has constant offset voltage .

Figure 8 shows DCFFE ac responses for eight different values. The DCFFE gain is varied in direction of the arrow and increased with high frequency boosting gain. Figure 9 shows simulated waveform of DCFFE. When data transition is occurred, the sufficient boosting gain make overshot. If received signal maintains former condition, Eq_out B has same value of Eq_out A.

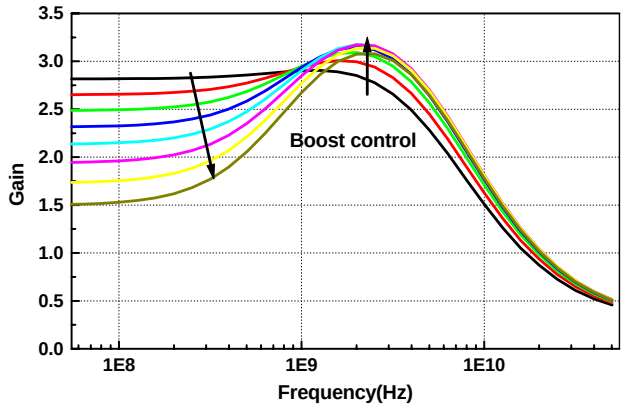

Figure 8. Magnitude bode plot of DCFFE

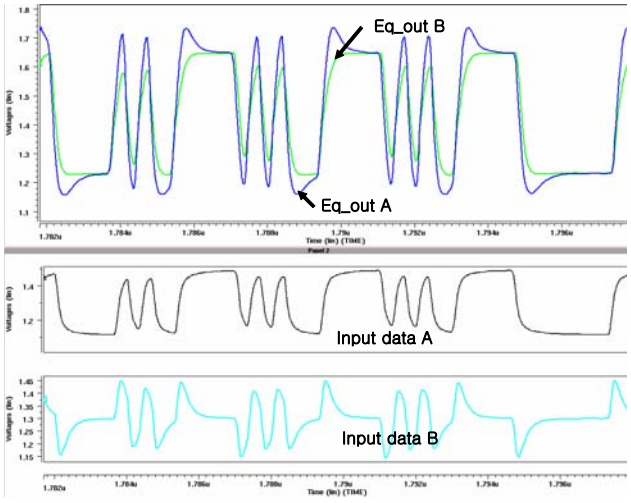

Figure 9. Input and Output Waveform of DCFFE

2.2 Bottom Detector

Figure 10 shows schematic of bottom detector that measures lowest signal value. When signal has reached its lowest value, the output voltage of the OTA will become equal to its negative saturation voltage[8]. The waveform of bottom detector is shown in Figure 11.

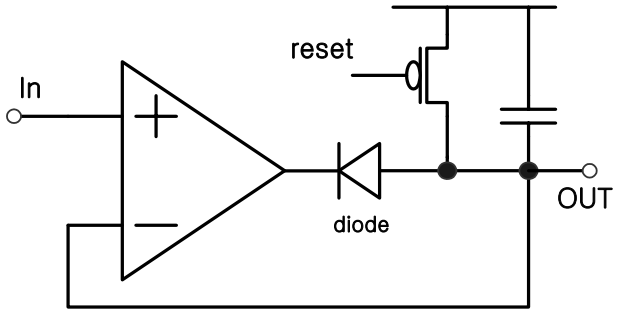

Figure 10. Schematic of Bottom Detector

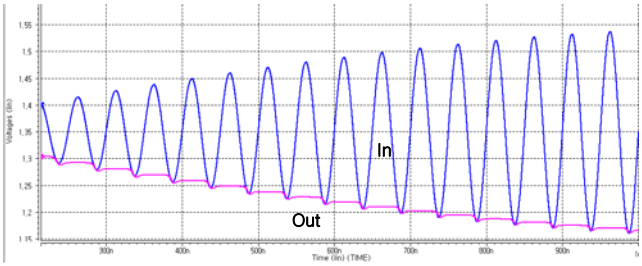

Figure 11. Waveform of Bottom Detector

Conventional equalizer typically employs a single adaptation loop that adjusts the peaking according to the difference between high frequency contents of data before and after slicing[9]. However, for proper equalization, the equalizer stages must remain linear whereas the slicer must experience complete switching. The above difficulty can be alleviated by swing control adjusting loop where the input and output swings of slicer are compared by low-pass filtering and rectification[10]. Without much consideration and analysis of loop dynamic, contradictions between the two loops can be occurred. And two loops provide a much longer settling time for the boost control loop unfortunately.

The approach introduced in this work is shown in Figure 3, where swing control is acquired by feed forward loop with bottom detector. With this mechanism, simple architecture for power measurement could be available; there is not any HPF.

2.3 Swing Controllable Slicer

The slicer, shown in Figure 12, is implemented by three cascaded buffers. The limiting is critical because the DCFFE output exhibits large overshoots even when ISI is minimized. As shown in figure 13, the third buffer produces controllable swing output with swing control voltage[11].

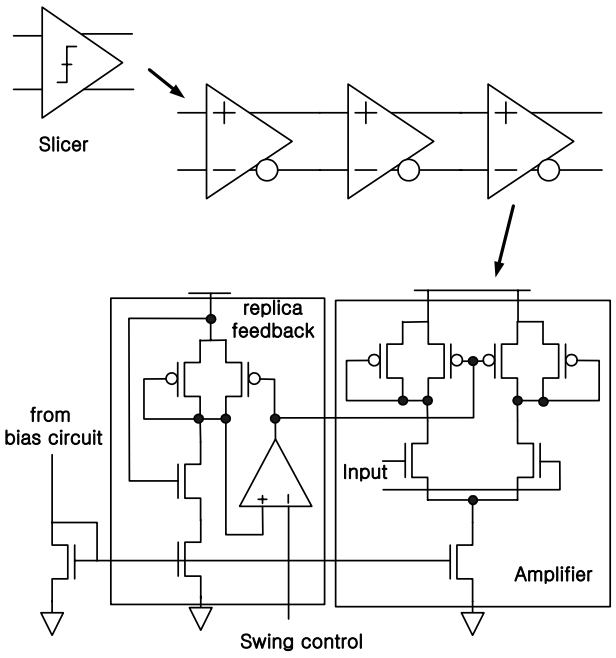

Figure 12. Schematic of Slicer

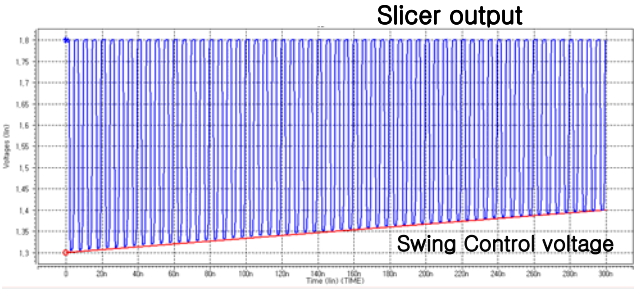

Figure 13. Waveform of Slicer

2.4 Control Block

The other trouble of conventional method is pattern dependence especially for the burst data pattern. There is a trade-off between settling time and loop stability. We used the digital locking method. Figure 14 shows control block. And figure 15 shows flow chart of control block. If optimal boost gain is obtained, the power measurement process will be stopped. Coefficient registers were implemented as an up counter.

Sense amplifier detects square circuit output at an interval of 500nsec. If DCFFE output power is larger than slicer output, this means boosting gain is adequate, and the boost gain will be held. The digital method has merits of power and equalizer locking output characteristics. For worst locking process, the equalizer needs 8 cycles (4usec).

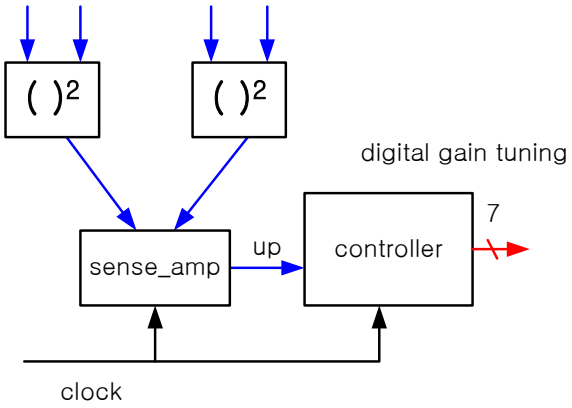

Figure 14. Power Comparison Circuit and Controller

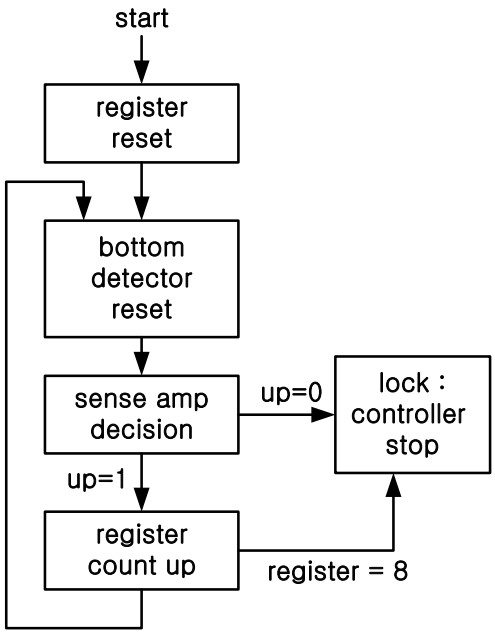

Figure 15. Flow Chart of Controller

3 Simulation Result and Conclusions

The equalizer circuit was designed with 0.18 ㎛ CMOS technology with 1.8V supply. Figure 16 and 17 show HSPICE simulation results; the eye diagram and waveform for 3-Gbps 2^7-1 PRBS at the output of PCB trace and after passing the equalizer. The PCB trace length is 0.2-meter for figure 16 and 2-meter for the figure 17. It is clear that signals are well recovered with the equalizer. The eye patterns show clear eye opening.

The circuit layout is shown in figure 18 where the circuit's area is 0.3 ㎟. Simulated power dissipation is about 20mW.

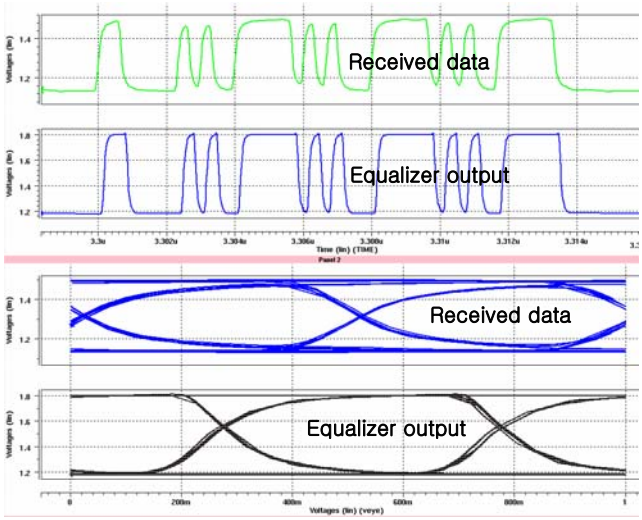

Figure 16. Eye diagram of line output after 0.2m PCB trace and equalizer output

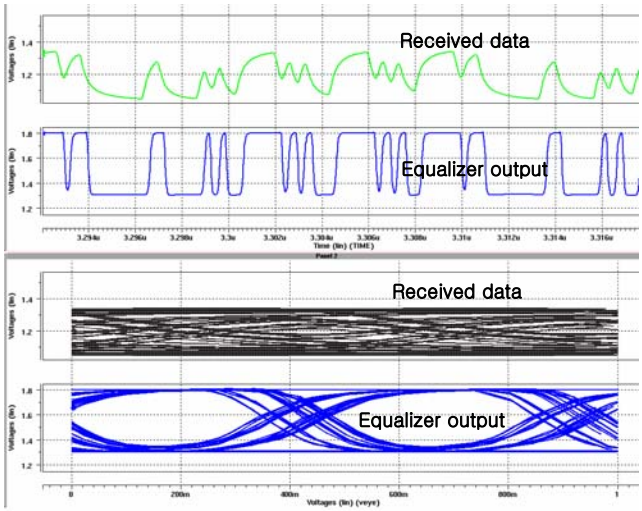

Figure 17. Eye diagram of line output after 2m PCB trace and equalizer output

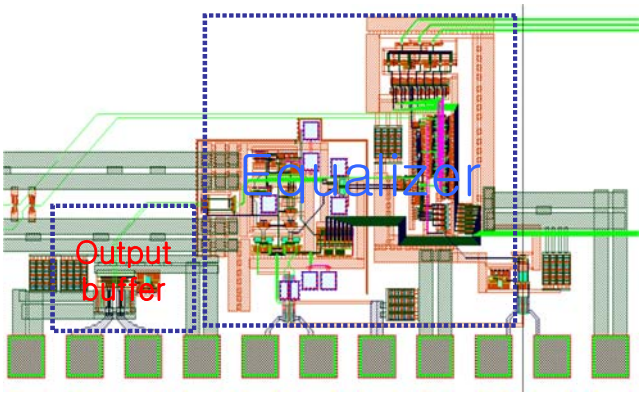

Figure 18 . Equalizer Layout

Acknowledgment

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