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SoC Design Technical Society
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11:10~12:30 **Session 20** (Room 205)

Channel, Security, and Cryptography

Session Chair : Dojun Rhee (Samsung Electronics)
Chanho Lee (Soongsil University)

11:10~11:30 *Efficient Hardware Architecture of SEED S-box for Smart Cards
Joon-Ho Hwang, SoC R&D Center, Samsung Electronics

11:30~11:50 HIGH PERFORMANCE VITERBI DECODER WITH A SCALABLE STRUCTURE
Tae-Jin Kim, Chanho Lee, Soon-Il Yeo*, Tae-Moon Roh*, School of Electronic Engineering, Soongsil University, *Basic Research Lab., ETRI

11:50~12:10 HW/SW Co-Design of ARM-Based CCMP-AES for Wireless LAN Security
Ho Yung Jang, Jun Rim Choi, School of Electrical Engineering and Computer Science, Kyungpook National University

12:10~12:30 About 2 Symbol Error Correction Method for Digital AV consumer products
Hyeong-Keon An, Department of Information and Communications Engineering, Tongmyong University of Information Technology

12:30~13:30 **Lunch**

13:30~15:30 **Session 21** (Room 201)

High Speed Signal Interface

Session Chair : Sung Min Park (Ewha Womans University)
Hong-June Park (POSTECH)

13:30~13:50 Decision Feedback Equalizer for Time-invariant Multi-drop Bus
Yu Jae-Suk, Yoo Kwisung, Gunhee Han, Department of Electrical and Electronic engineering, Yonsei university

13:50~14:10 *1 Gb/s gated-oscillator burst mode CDR with half-rate clock recovery
Pyung-Su Han, Woo-Young Choi, High speed information transmission Lab., Yonsei University

14:10~14:30 A 1.25Gb/s clock recovery circuit using half-rate 4X-oversampling PFD
Hee-sop Song, Hyung-wook Jang, Sung-sop Lee, Jin-ku Kang, Department of Electrical Engineering, Inha University

14:30~14:50 A Dual-loop CMOS PLL with the Max-to-min Frequency Ratio Larger than Five Guaranteed under PVT Corners
Jung-Bum Shin, Sang-Hune Park, Seung-Jun Bae, Hong-June Park, Department of Electronic and Electrical Engineering, POSTECH

14:50~15:10 A DLL-Based Multi-Clock Generator Having Fast-Relocking and Duty-Cycle Correction Scheme
Tae Jin Hwang, Gyu Sung Yeon, Chi Hoon Jun, Yong Moon, and Jae-Kyung Wee, School of Electronic Engineering, Soongsil University

15:10~15:30 A 2.5-Gb/s optical receiver chipset for SONET/SDH applications
Jin Kyu Kwon, Sang Seok Lee, Sang Bock Cho, and Sung Min Park, School of Electrical Engineering, University of Ulsan

13:30~15:30 **Session 22** (Room 208B)

SoC Design Methodology II

Session Chair : Jun-Dong Cho (Sungkyunkwan University)
Kyoung-Son Jhang (Chungnam National University)

13:30~13:50 Clock Mesh Planning Automation System
Soo-Hyun Kim, Myung-Soo Jang, Sea-Hwan Choi, CAE Center, Gun-Ok Jung*, Sung-Bae Park*, CAE Center, Samsung Electronics, *Processor Architecture Lab., Samsung Electronics

1 Gb/s gated-oscillator burst mode CDR with half-rate clock recovery

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Abstract *A new burst mode clock and data recovery circuit is realized that improves the previously-known gated-oscillator technique with half rate clock recovery. The circuit was fabricated with 0.25um CMOS technology, and its functions were confirmed up to 1 Gbps.*

Keywords: Burst mode, PON, clock and data recovery, gated oscillator,

1 Introduction

In Passive Optical Network (PON) systems [1], Optical Line Termination(OLT) in the central station does not know exactly when data packets arrive from various Optical Network Units (ONUs) located at the subscriber side as shown in Fig. 1. Consequently, OLT receiver has to align the receiver clock to each burst data packet.

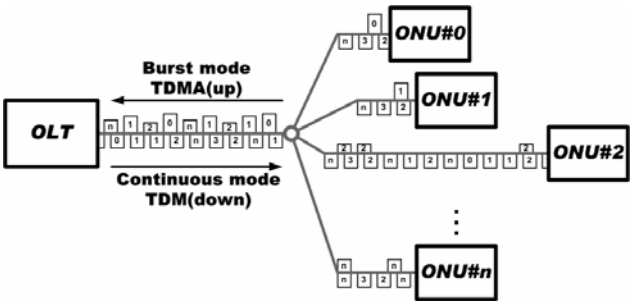


Figure 1. PON system

The conventional PLL-based clock recovery circuit cannot be used for burst mode application since it requires a long sequence of overhead bits to reach the lock condition. In addition, the clock frequency can drift away during the silent times, which require another phase-locking process.

The above problem can be solved with the gated-oscillator clock recovery technique[2], in which “gate stage” is added in the signal path of ring oscillators, making it possible to instantly align the clock phase with data. This technique is simple and requires low power but has limited high-speed operation.

In this paper, we propose a new circuit configuration that has half-rate clock recovery capability thus improving the speed performance of gated-oscillator clock recovery circuits.

2 Gated-oscillator CDR

Fig. 2 shows a gated ring oscillator. An AND gate acts as the gate and can turn on and off the oscillation. If Enable is low, the oscillation stops and if Enable is high, the oscillation starts again. In addition, the oscillation always begins with the signal falling from high to low. Consequently, output clock phase can be set to a desired value by the Enable signal.

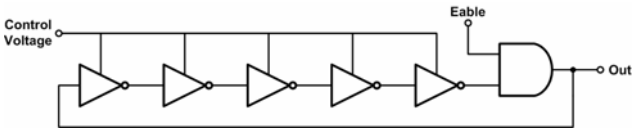


Figure 2. Gated oscillator

In gated-oscillator CDR, input data are used as Enable signals for two gated oscillators as shown in Fig. 3 and output clock is generated whose phase is always aligned with the input data.

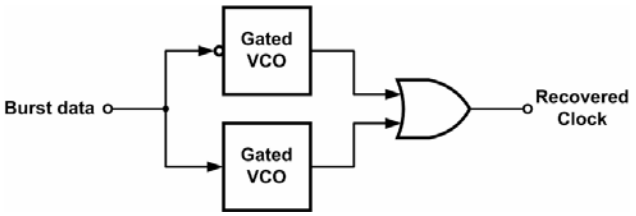


Figure 3. Gated oscillator based CDR

The gated-oscillator clock recovery technique described above can be adopted only for the full rate clock recovery, which means that the frequency of the recovered clock equals the data rate. If the data rate is increased then the clock frequency should be increased as well setting a speed limit especially with CMOS technology.

An alternative way to overcome the device speed limitation is to use multi-phase clock technique, in which more than two identical operations are performed within one clock cycle as in DDR (Double Data Rate) memory using both rising and falling edges to read and write the data, doubling the bandwidth. Recently, many reseachers have used this idea for continuous-mode clock recovery applications [3,4] but no attempt has been made for gated-oscillator burst mode applications. We propose a new circuit structure in which the output clock phase can be selectively set to either 0 or pi, making gated-oscillator CDR with half-rate clock recover possible.

3 Gated oscillator details and problems with half rate clock recovery

Another problem arises when you come to build half rate clock recovery with the gated oscillator. Shown as “ideal clock” in Figure 4, recovered half rate clock has to be shifted from the data transition edges exactly pi/2 for optimum sampling, but gated oscillator always aligns the clock edge to data edges. Therefore you need delayed version of recovered clock, and it will be accounted later.

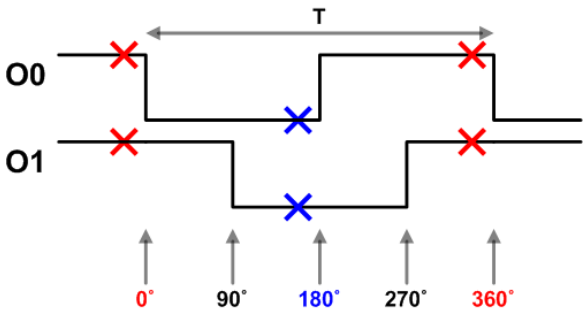


Figure 4. Phase definition and finding R0 and R1

4 Gated-oscillator with half-rate clock

Figure 5 shows our new gated-oscillator. Owing to the additional gate stage it takes only 1/4 of the clock period to settle down when Enable goes low and oscillation stops. In addition, by controlling values of R1 and R2, the output clock phase can be controlled. For example, setting both R0 and R1 to low, the oscillator always starts to oscillate with O0 going to high. The combination of R0 and R1 required for the desired phase values is shown in Table 1. O0d and O1d is simply pi/2 delayed version of O0 and O1 and they are used to retime the data bits in half rate CDR.

5 Proposed half rate CDR

With the new version of gated oscillators, we designed a half rate clock recovery circuit shown in Figure 6. It has two gated oscillators, and they are switched by input data. This circuit differs from the conventional gated-oscillator CDR in the following points.

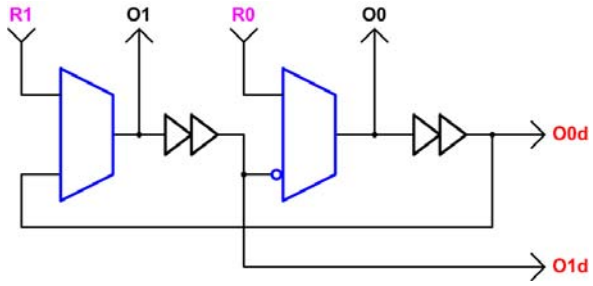


Figure 5. Modified gated oscillator

Table 1. Starting phase and corresponding R0 and R1

Phase	R0	R1
0°	1	1
90°	0	1
180°	0	0
270°	1	0

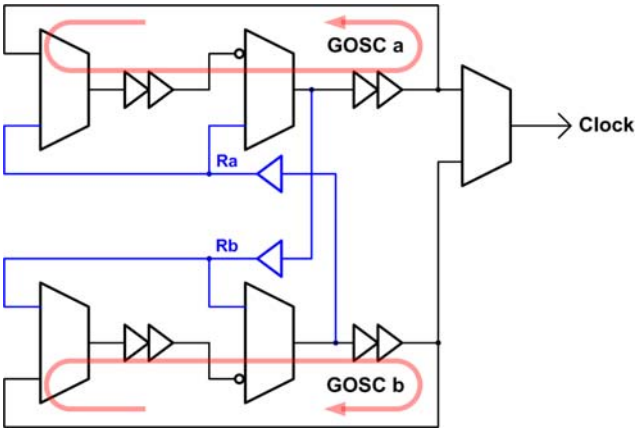


Figure 6. Proposed half-rate CDR

First, our new gated oscillators require the reset phase setting value R0 and R1. Since both rising and falling edges are required, it has to alternate the reset phase value supplied by the the oscillators. Second, the half portions of the recovered clock are combined using a MUX, not an OR gate, because even when the oscillator is not oscillating, the alternating R values come out to the output and may corrupt the combined clock. Data signals are also used as the MUX selecting signals so that the output path can be switched to the clock-generating gated oscillator resulting in complete half rate clock signals aligned with the data.

6 Experimental results

The proposed half rate clock recovery circuit was designed with CMOS 0.25um parameter and verified by hspice simulation. Designed circuit was fabricated and directly attached on the test board. Prototype chip includes 8-bit wide deserializer as well as half rate clock recovery, as shown in Figure 7, therefore we can observe 1/8 rate recovered clock instead of half rate clock. Figure 8 shows the micro-photograph of the chip.

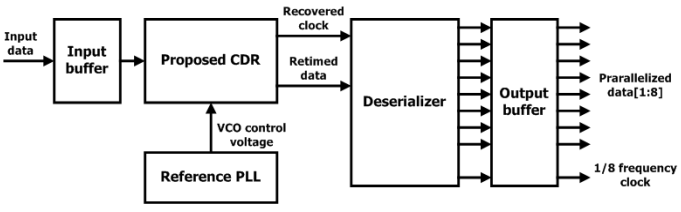


Figure 7. Block diagram of the prototype chip

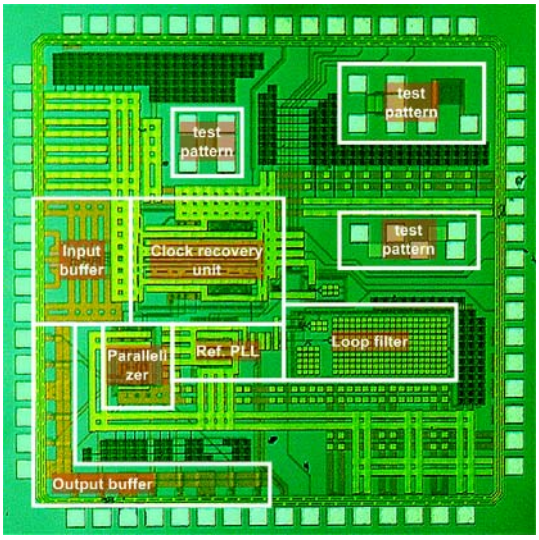


Figure 8. Micro-photograph of prototype chip

It was found that the fabricated chip can operate at up to 1Gbps. Figure 9 shows recovered clock from the PRBS11 data, and the measured clock jitter was 4.6ps[rms].

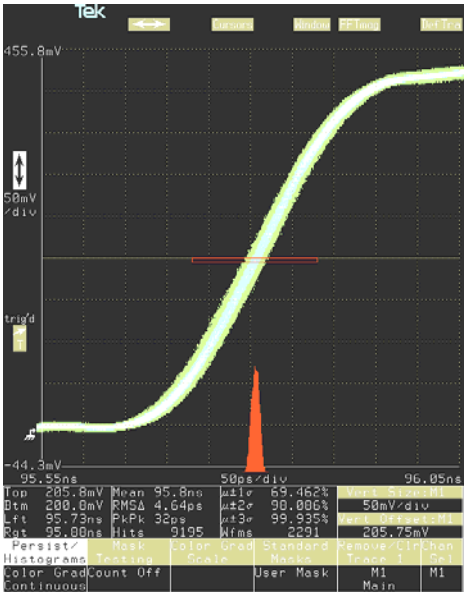
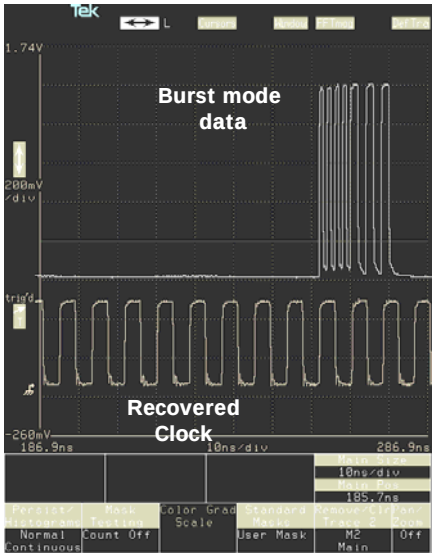


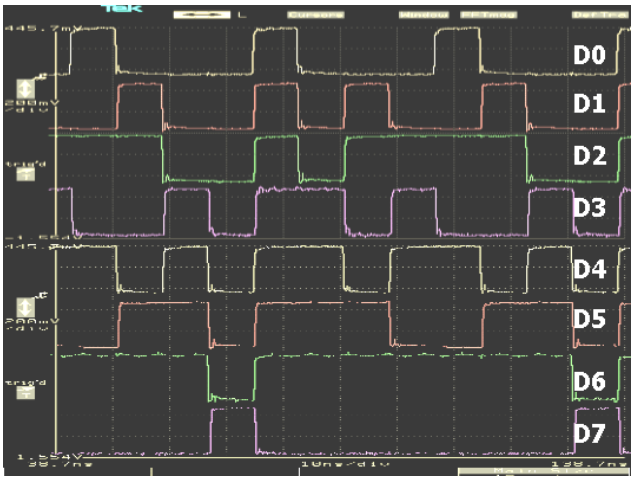
Figure 9. Recovered clock from PRBS11 and jitter measurement

Burst mode as well as continuous mode operation was verified by injecting the packet-like programmed bit patterns and into the test chip, and the recovered data and clock are shown in Figure 10. Table 2 shows the summary of chip performance.



(a) Burst mode packet and recovered clock

(b) Retimed and deserialized data



(c) Retimed and deserialized data in continuous mode data

Figure 10. Half rate clock recovery operations

Table 2. Starting phase and corresponding R0 and R1

Process	CMOS 0.25um
Power supply	2.5V
Operating frequency	1Gbps for PRBS15
Recovered clock jitter	4.6ps[rms] for PRBS11
Power consumption	100mW core, 375mW including deserializer and I/O

Acknowledgements

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References

[1] “G.984.2 Gigabit-capable passive optical networks(GPON): Physical media dependent(PMD) layer specification”, ITU-T, 2003

[2] M. banu and A. E. Dunlop, “Clock Recovery Circuit with Instantaneous Locking”, Electronic letters, Vol. 28, No. 23, pp. 2127 – 2130, 1992

[3] Chih-Kong Ken Yang and Mark A. Horowitz, “A 0.8-um CMOS 2.5Gb/s Oversampling Receiver and Transmitter for Serial Links”, JSSC, Vol. 31, No. 12, pp. 2015-2023, December 1996

[4] Gijung Ahn, Deog-Kyoon Jeong, and Gyudong Kim, “A 2-Gbaud 0.7-V Swing Voltage-Mode driver and On-Chip Terminator for High-Speed NRZ Data Transmission, JSSC, Vol. 53, No. 6, pp. 915-918, June 2000