A 2-Gbps CMOS Adaptive Line Equalizer

Jae-Wook Lee, Bhum-Cheol Lee*, and Woo-Young Choi
Dept. of Electrical and Electronic Eng., Yonsei University,
134, Shinchon-Dong, Sudaemon-Ku, Seoul 120-749, Korea
TEL: (02) 2123 - 7709, E-mail: patima@tera.yonsei.ac.kr
*Switching Technology Team, Electrics and Telecommunications Research Institutes,
161, Gajeon-Dong, Yusong-Ku, Daejon 305-350, Korea

ABSTRACT

A 2-Gbps line equalizer circuit is realized with 0.25 ㎛ CMOS technology. The equalizer is made of input stage buffer, limiter and square difference circuits. The limiter has replica-feedback limiting amplifiers, which do not require common mode feedback. Successful equalization is demonstrated for signals transmitted over 1.5m long PCB trace.

Ⅰ. Introduction

In high-rate NRZ data communication over cables or PCB traces, skin-effect resistance causes attenuation of high-frequency signal components. However, low frequency signal components are not attenuated, resulting in inter symbol interference (ISI) that limits transmission data rate and distance.

This ISI can be greatly reduced if the receiver includes a line equalizer. Digital [1-3] and analog [4-7] line equalizers have been reported in literature. In digital equalization, the output of the analog front end has to be fed into a high-resolution A/D converter (ADC), which usually consumes a great deal of power and chip area [1]. By using an analog pre-equalizer just before the ADC, a less accurate ADC can be used [2]. But this results in more complicated structure for Decision Feedback Equalization (DFE) and, consequently, its applicability for high data transmission rate is limited

On the other hand, analog equalization has none of the above-mentioned problems, although it requires more careful circuit design. Gm-C filters and OPAMP-based filters have been applied for analog equalization [4]. While Gm-C filtering is easier to implement in high frequency signal processing, OPAMP-based filtering is more power efficient.

In this paper, a new OPAMP-based analog equalizer having adaptive DFE circuit is realized for equalizing 2-Gbps signals transmitted over PCB traces.

2. Background

A thin strip line with width W has a frequency-dependent resistance per unit length as [8]:

$$R(f) = \frac{1}{2W}\left(\frac{\pi \mu f}{\sigma}\right)^{1/2} \qquad (1)$$

where σ is metal conductivity (5.8×10^7 ohms/m for copper). The resistance is proportion to the square root of the frequency and inverse of the linear dimension of the conductor.

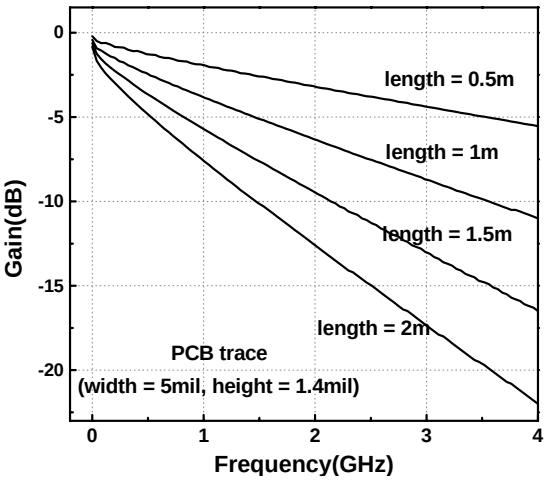


Figure 1. Attenuation curves for 50-ohm strip guided PCB traces.

Figure 1 shows the calculated attenuation as a function of frequency for a strip guided PCB trace with a differential impedance of Z_0 = 100ohms. The calculation was done for a strip line structure shown in figure 2 with HSPICE W-model.

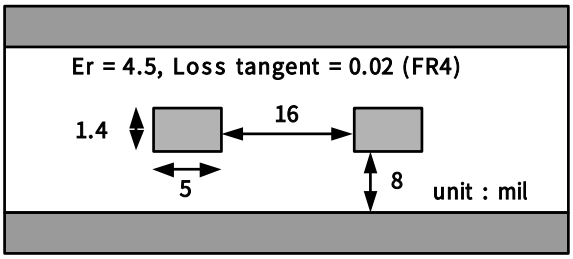


Figure 2. Strip line structure and parameter

As can be seen in the figure 1, attenuation up to 60% of the original signal magnitude per meter can be observed at 1GHz. A line equalizer can overcome this.

3. Equalizer structure

In order to compensate ISI caused by the bandwidth limited channel, the equalizer should perform the inverse of the channel characteristic transfer function. The required equalizer transfer function is given as

$$H(s) = 1 + \alpha G(s), \qquad (2)$$

where, G(s) is the transfer function from a high frequency boost stage and α is adaptively determined gain. Figure 3 shows the block diagram for our equalizer. The input stage and high pass filter (HPF) construct transfer function given in (2). The gain of Variable Gain Amplifier (VGA) is determined by DFE mechanism with limiter and square difference circuits.

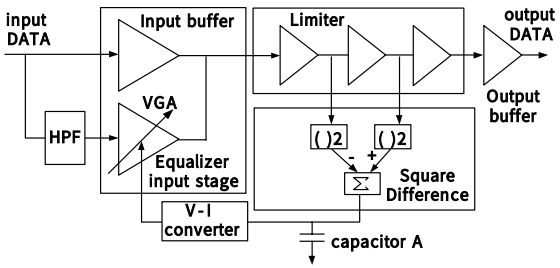


Figure 3. Equalizer block diagram.

Figure 4 shows HPF structure and its frequency response. As shown in figure 5, the sum of currents from the input buffer and VGA is delivered to the limiter.

Figure 6 shows the limiter structure, which has 3-stage amplifiers with the same fan-out. First

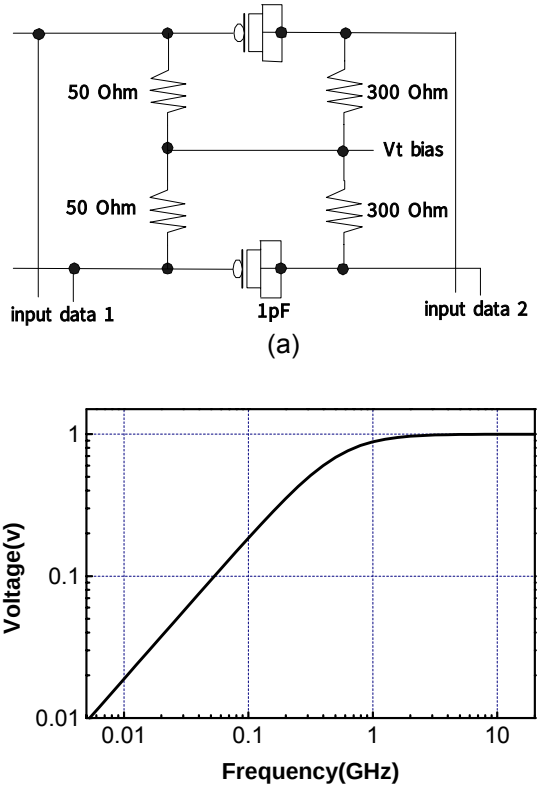


Figure 4. High-pass filter: (a) Structure, (b) Frequency response.

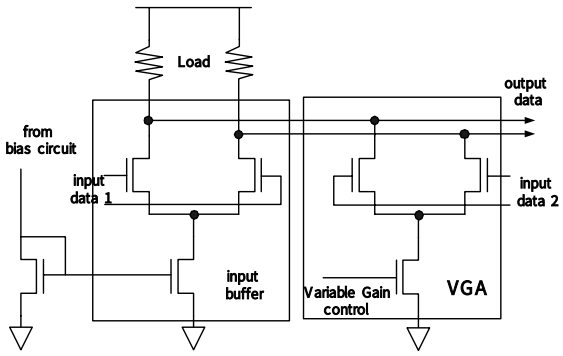


Figure 5. Equalizer input stage schematic

and second stage amplifiers drive square difference (SD) circuits. And the third stage drives output buffer. The amounts of output swings for first and second stages are guaranteed the same by the replica-feedback [9].

Figure 7 is the schematic for Square Difference (SD) circuit, which detects slew rate difference between input A and B, and adjusts the voltage level of capacitor A by pumping currents. Because input A and B have equal swing levels, only slew rate difference causes current pumping until they are matched.

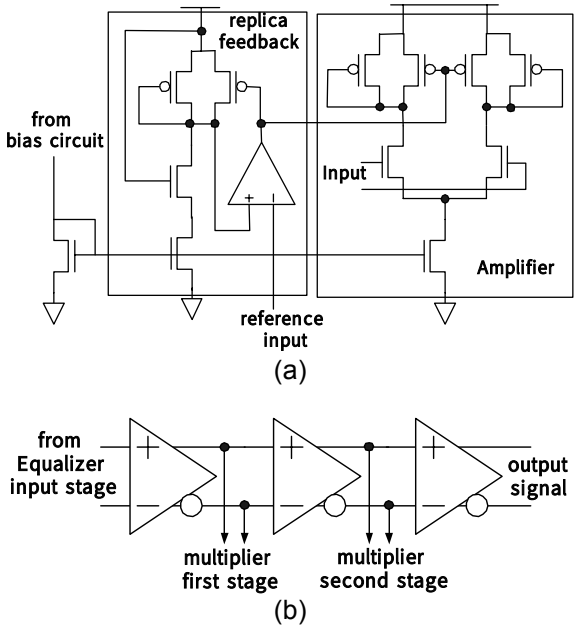


Figure 6. Limiter circuit: (a) Replica-feedback amplifier schematic, (b) Limiter schematic

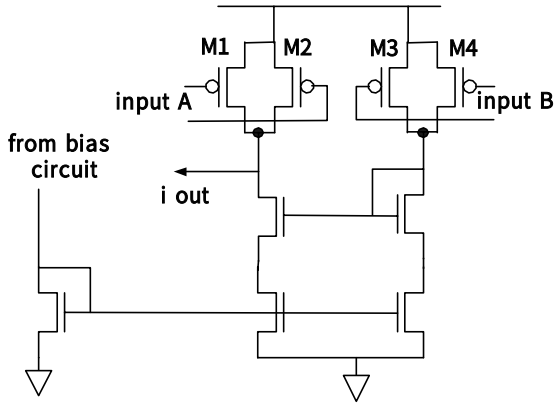


Figure 7. Square difference schematic

The voltage at the capacitor A is converted into a current, which controls VGA bias and, thus, its gain.

4. Simulation and Measurement results

Our equalizer circuit was fabricated with 0.25 μm CMOS technology. The circuit was tested in a chip-on-board assembly with 2.5-V power supply.

Figure 8 shows transient variations of the control voltage of the VGA from unstable to stable states for different PCB trace lengths for 2-Gbps signal.

Figure 9 and 10 show the eye diagrams for a 2-Gbps 2^7-1 PRBS at the output of PCB trace and after passing the equalizer. The PCB trace length is 0.6-meter for figure 9 and 1.5-meter for the figure 10. It is clear that the signals are recovered and rectified with the equalizer. The eye pattern is clearly large enough for detection.

The die photo of circuit is shown in figure 11 where the circuit's area is 0.08 ㎟. The circuit's power dissipation is 45mW.

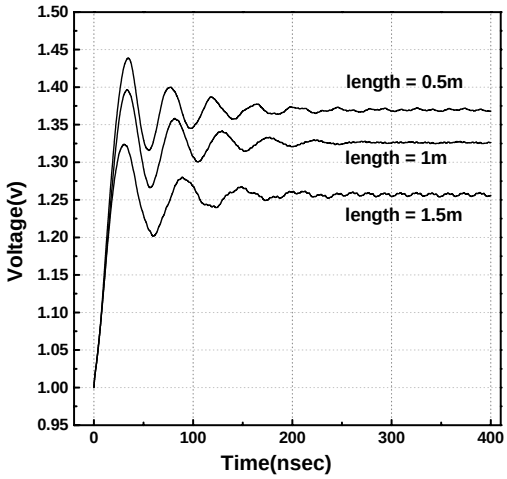
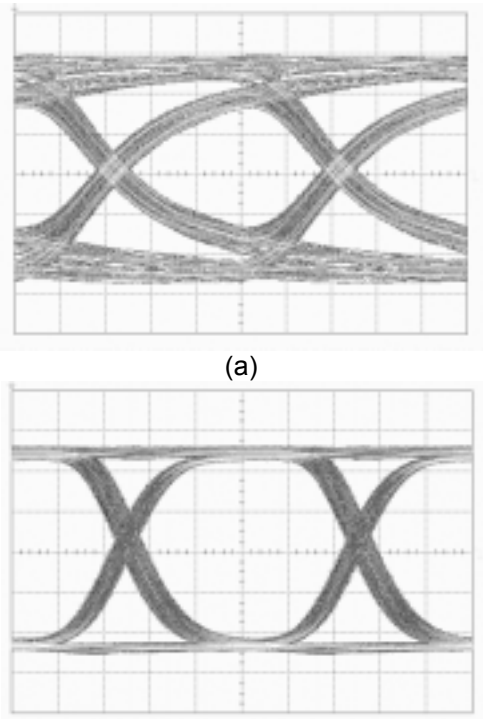


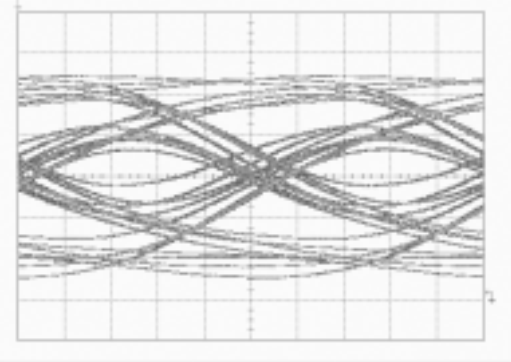
Figure 8. VGA control signal.



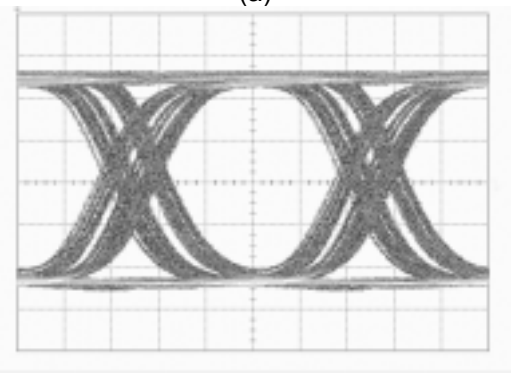
(a)

(b)

Figure 9. Eye diagram; (a) line output after 0.6m PCB trace, (b) equalizer output after 0.6m PCB trace. Vertical scale is 100mV/div; horizontal scale is 100ps/div.



(a)



(b)

Figure 10. Eye diagram; (a) line output after 1.5m PCB trace, (b) equalizer output after 1.5m PCB trace. Vertical scale is 100mV/div; horizontal scale is 100ps/div.

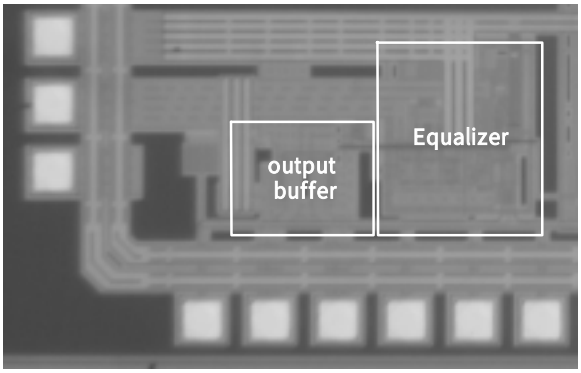


Figure 11. Die photo

References

[1] Tai-Cheng Lee and Behzad Razavi, " A 125-MHz CMOS Mixed-Signal Equalizer for Gigabit Ethernet on Copper Wire," *IEEE Custom Integrated Circuits Conference*, 2001, pp. 131-134.

[2] Kamran Azadet et al. "A Gigabit Transceiver Chip Set for UTP CAT-6 Cables in Digital CMOS Technology," *IEEE International Solid-State Circuits Conference*, 2000, pp. 300-307.

[3] N. Patrick Kelly et al. "A Mixed-Signal DFE/FFE Receiver for 100Base-Tx Applications," *IEEE International Solid-State Circuits Conference*, 2000, pp. 310-311.

[4] Pezhman Amini and Omid Shoaei, "A Low-Power Gigabit Ethernet Analog Equalizer," *IEEE International symposium on Circuits and Systems*, 2001, vol. 1, pp. 176-179

[5] Joseph N. Babanezhad, "A 3.3V Analog Adaptive Line-Equalizer for Fast Ethernet Data Communication," *IEEE Custom Integrated Circuits Conference*, 1998, pp. 343-346.

[6] Mohammad H. Shakiba, "A 2.5Gb/s Adaptive Cable Equalizer," *IEEE International Solid-State Circuits Conference*, 1999, pp. 396-397.

[7] Yoshiharu Kudoh et al., "A 0.13um CMOS 5-Gb/s 10-meter 28AWG cable transceiver with no-feedback-loop continuous-time post-equalizer," *Symposium on VLSI Circuits Digest of Technical Papers*, 2002, pp. 64-67.

[8] W.J. Dally and John Poulton, "Transmitter Equalization for 4-Gbps Signaling" IEEE Micro, vol. 17, Jan-Feb. 1997. pp. 48-56.

[9] J. Maneatis, "Low-jitter process-independent DLL and PLL based on self-biased techniques," *IEEE J. Solid-State Circuits*, vol.31, pp.1723-1732, Nov. 1996