Design of Monolithic 3GHz-Range PLL Using 0.5um GaAs MESFET Process

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Abstract

A 1.8 ~ 3.2GHz fully differential phase-locked loop (PLL) is realized for ATM clock generation applications. The PLL includes a new differential voltage-controlled oscillator (VCO) with the wide tuning range of 1.74 ~ 3.40GHz and a new differential charge pump with improved hold characteristics. The PLL is implemented with 0.5μm GaAs MESFET process. The experimental results show that the PLL has the lock-range of 1.8 ~ 3.2GHz and its output RMS jitter is at most 5.0ps (0.015UI) at 3.2GHz.

I. Introduction

In multi-link systems such as ATM, it is cost-effective to integrate several links into one high-speed serial link reducing the system complexity. This requires high-speed PLLs which provide the system clock for data serialization and de-serialization. There have been intensive research efforts to increase the PLL operating frequency and the operating range, and reduce output jitter [1-4]. Since the maximum operating frequency and the operating range of the PLL are determined by VCO and the jitter characteristics are influenced by VCO and the charge pump, most research efforts for high-speed PLL are focused on VCO and the charge pump. Our goal is realizing a high-speed PLL with a wide lock-range and low jitter characteristics for ATM applications. In order to achieve this goal, we come up with new circuit ideas for VCO and the charge pump.

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The remainder of this paper is organized as follows. Section II describes a new type of wide-tuning range VCO and demonstrates its characteristics by HSPICE simulation results and experimental results. Section III explains a newly proposed charge pump circuit having improved output hold characteristics. The experimental results of the PLL which has the proposed VCO and the charge pump are discussed in Section IV, and Section V gives the conclusions.

II. Voltage-Controlled Oscillator

A ring oscillator-type VCO is widely used for PLLs for system clock generation applications since it requires a very small chip area and it can produce high frequency signals with large magnitudes suitable for digital systems.

Figure 1 shows the block diagram of a new VCO structure [5][6] realized in this paper. It has two identical loops, each of which consists of one AMUX and several inverters. Two loops are combined by AMUXs. Assuming that the AMUX output V_{z1} and V_{z2} are linearly controlled by V_C and the propagation delays of AMUXs and inverters are t_d, the following relationships can be derived:

$$V_{z1} = \left[(1-V_C)V_y + V_C V_x\right]\cdot e^{-j\theta} \quad \text{(1-a)}$$

$$V_{z2} = \left[(1-V_C)V_x - V_C V_y\right]\cdot e^{-j\theta} \quad \text{(1-b)}$$

$$V_x = -A^2 e^{-j2\theta} V_{z1} \quad \text{(2-a)}$$

$$V_y = A^2 e^{-j2\theta} V_{z2} \quad \text{(2-b)}$$

In the above equations, A is the small signal gain of the inverter at the frequency of f_{osc}, and θ is the output phase

delay produced by the inverter and AMUX. From Eq. (1) and (2), the relationship between V_{z1} and V_{z2} is obtained as

$$V_{z1} = \frac{(1-V_C)A^2e^{-j3\theta}}{1+V_CA^2e^{-j3\theta}} \cdot V_{z2} \quad (3\text{-a})$$

$$V_{z2} = -\frac{(1-V_C)A^2e^{-j3\theta}}{1+V_CA^2e^{-j3\theta}} \cdot V_{z1}. \quad (3\text{-b})$$

By summing Eq. (3-a) and (3-b), the following equations are obtained.

$$\left[\frac{(1-V_C)A^2e^{-j3\theta}}{1+V_CA^2e^{-j3\theta}}\right]^2 = -1 \quad (4\text{-a})$$

$$\frac{(1-V_C)A^2e^{-j3\theta}}{1+V_CA^2e^{-j3\theta}} = \pm j \quad (4\text{-b})$$

Since the left side of Eq. (4-b) represents the phase delay between V_{z1} and V_{z2}, "+j" in the right side is meaningless. Therefore, $e^{-j3\theta}$ can be expressed as

$$e^{-j3\theta} = \frac{-j}{A^2[(1-V_C)+jV_C]}. \quad (5)$$

In addition, θ can be expressed by T_{osc} and t_d as

$$\theta = \frac{2\pi t_d}{T_{osc}}. \quad (6)$$

By combining Eq. (5) and (6), f_{osc} can be expressed by as

$$f_{osc} = \frac{\frac{\pi}{2} + \tan^{-1}\left(\frac{V_C}{1-V_C}\right)}{2\pi} \cdot \frac{1}{3t_d} \quad (7)$$

From Eq. (7), it can be seen that the new VCO has the tuning range of $1/(12t_d) \sim 1/(6t_d)$, which is wider than the conventional VCO structure.

The advantage of the new VCO is that the AMUX input phase difference is fixed at π/2 in the whole tuning range. As shown in Figure 1, two inputs of AMUX1 and AMUX2 are V_x and V_y, and $-V_y$ and V_x, respectively. In case of AMUX1, the phase difference between V_y and V_x is exactly π/2, because V_y is a delayed signal of V_x by $3t_d$, and V_x is an oscillating signal which has a period of $12t_d$. In case of AMUX2, the phase difference between V_x and $-V_y$ is also exactly π/2, because the phase difference between $-V_y$ and V_y is π.

In order to estimate the tuning sensitivity of the proposed VCO, f_{osc} at various V_C is measured from the fabricated VCO. As can be seen in Figure 2, VCO tuning range is 1.74 ~ 3.40GHz and it can be accurately fitted by Eq. (7) by using t_d=50ps.

III. Charge Pump

A differential charge pump is generally used for high-speed PLL applications because it switches only the current paths while leaving the current sources and sinks always turned on.

Figure 3 shows the schematic diagram for our new charge pump [7]. In order to increase the output resistance of all the current sources and sinks, they are implemented with the cascode structure using one GaAs MESFET and one resistor. Six enhancement mode GaAs MESFET diodes are placed in each current path to prevent the charges in the loop filter capacitors from flowing to the current sinks during the hold state. In order to block the leakage currents from I_{UP1} and I_{UP2} to C_P and C_N, the current sink control blocks, F1 and F2, are implemented which respectively make I_{DN1} and I_{DN2} to be equal to or larger than I_{UP1} and I_{UP2}. This scheme differs from the current sink control method used in [8] in that I_{DN1} and I_{DN2} do not have to be exactly matched to I_{UP1} and I_{UP2}. The only requirement in our scheme is $I_{DN1} \geq I_{UP1}$ and $I_{DN2} \geq I_{UP2}$, a much easier condition to satisfy.

IV. Experimental Results

A PLL that has newly proposed VCO and the charge pump was implemented with 0.5μm GaAs MESFET

process. Figure 4 shows the layout of the chip which include three PLLs with slight modifications for the measurement purpose. The chip size is 3500μm × 3500μm and the power dissipation of the PLL core is about 380mW with +3.3V/-2.0V power supplies. The PLL uses a generic PFD implemented with nine SCFL 2-input OR gates and two SCFL 3-input OR gates, frequency dividers (divide by 20) implemented with SCFL D-type flip-flop, and on-chip second order loop filters. The loop filter parameters (1800Ω, 40pF, 4pF) were chosen to make damping factor (ζ) of the closed-loop transfer function to be 0.707, which corresponds to loop bandwidth of 6.45MHz.

The fabricated PLL was fully functional with the lock-range of 1.8 ~ 3.2GHz with the input reference signal ranging from 90 to 160 MHz. Figure 5 shows the measured RMS jitters for the entire lock ranges. The jitter ranges from 0.009UI at about the center oscillation frequency to 0.015UI at the highest oscillation frequency. Figure 6 shows the measured jitter histograms of the VCO output when the PLL was locked at its minimum, center, and maximum frequency. The RMS jitters for the VCO output are 6.2ps (0.011UI) at f_{VCO}=1.8GHz, 3.9ps (0.010UI) at f_{VCO}=2.6GHz, and 5.0ps (0.015UI) at f_{VCO}=3.20GHz.

V. Conclusions

A 1.8 ~ 3.2GHz fully differential on-chip PLL with low jitter characteristics was successfully realized with 0.5μm GaAs MESFET. The experimental results show that the PLL has the lock-range of 1.8 ~ 3.2GHz and the maximum VCO RMS jitter of 5.0ps (0.015UI) at 3.2GHz.

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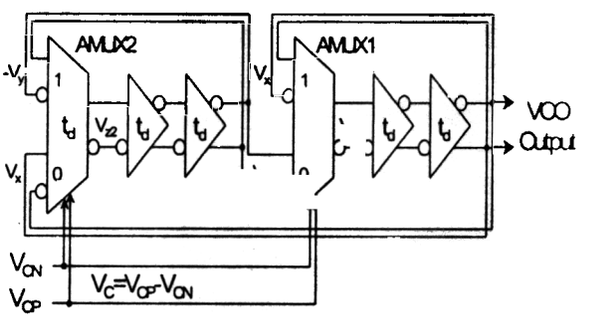


Figure 1 Block diagram of the proposed VCO

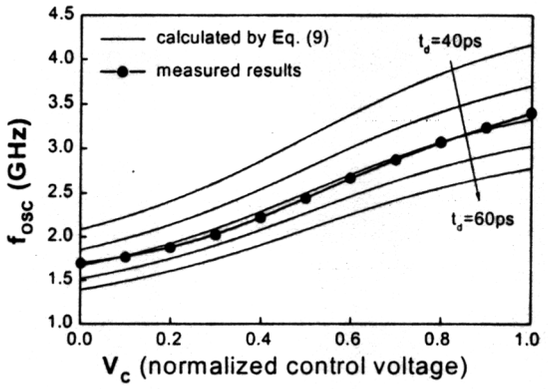
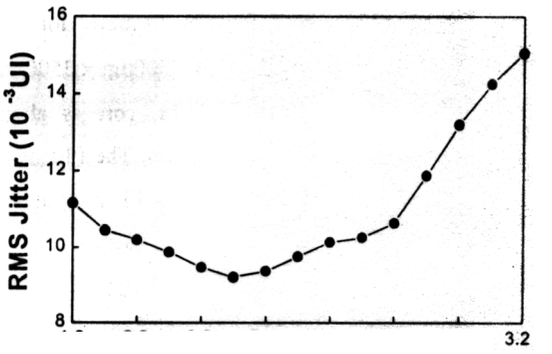


Figure 2 Measured and calculated VCO tuning sensitivity



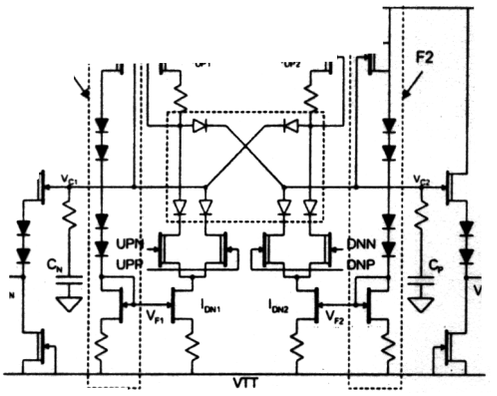


Figure 3 Schematic diagram of the proposed charge pump

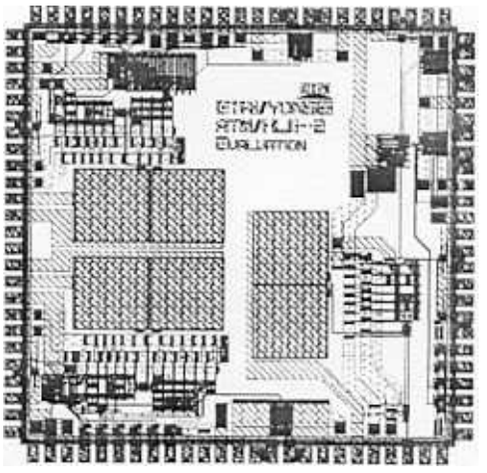


Figure 4 Layout of PLL.
(3 PLL circuits are included)

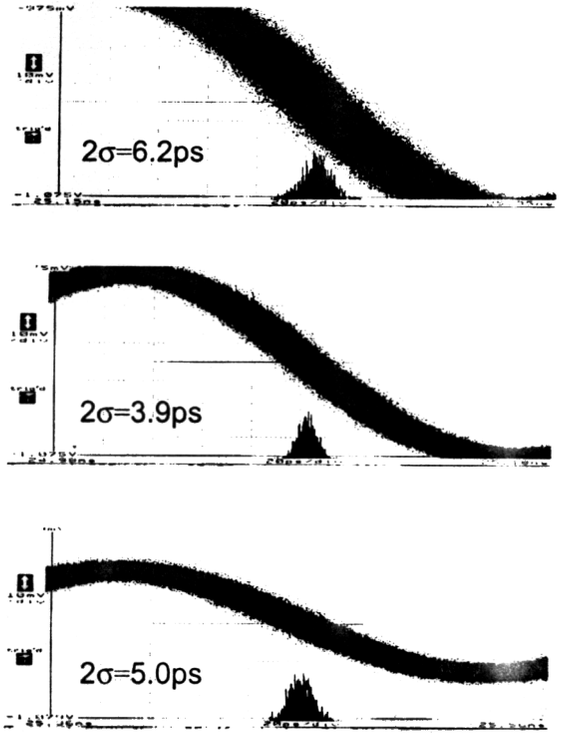


Figure 6 Measured jitter histograms of VCO outp

(a) f_{vco}=1.8GHz

(b) f_{vco}=2.6GHz

(c) f_{vco}=3.2GHz