Analysis of a Novel Elevated Source Drain MOSFET with Reduced Gate-Induced Drain-Leakage Current

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Abstract — A new self-aligned ESD (Elevated Source Drain) MOSFET structure which can effectively reduce the GIDL (Gate-Induced Drain Leakage) current is proposed and analyzed. Proposed ESD structure is characterized by sidewall spacer width (W_S) and recessed-channel depth (X_R) which are determined by dry-etching process. Elevation of the Source/Drain extension region is realized so that the low-activation effect caused by low-energy ion implantation can be avoided. The GIDL current in the proposed ESD structure is reduced as the region with the peak electric field is shifted toward the drain side.

I. INTRODUCTION

As the MOSFET's have been scaled down to 0.15-μm regime, the formation of ultrashallow junctions have become increasingly important to suppress the short-channel effects. In order to make ultrashallow junctions with the conventional ion implantation technology, very low-energy ion implantation and rapid thermal annealing is indispensable. However, the low implantation energy causes higher sheet resistance due to the low-activation effect [1]. As a result, increase in the implantation dose is required in order to reduce the sheet resistance of the SDE (Source Drain Extension) region. But in conventional LDD (Lightly Doped Drain) MOSFETs, the increase of the SDE implantation dose results in the increase of the GIDL (Gate-Induced Drain-Leakage) current [2]. GIDL is one of the major leakage components that determine the off-state leakage characteristics and it can also act as a scaling limiting factor in deep-submicron devices [3-4]. Consequently, for the conventional LDD structures, there exists a significant tradeoff relationship between the driving current and the GIDL current. In this work, a novel ESD MOSFET structure which can effectively reduce the GIDL current without sacrificing the driving current is proposed and analyzed.

II. PROPOSED STRUCTURE

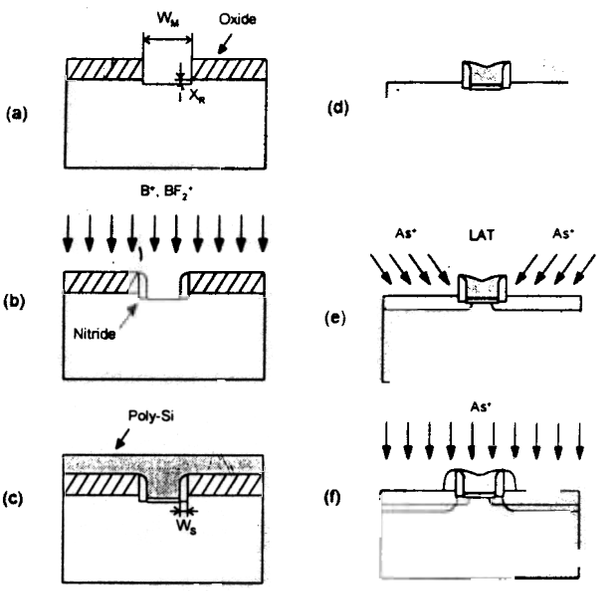

Fig. 1. Fabrication steps for the proposed ESD MOSFET.
(a) mask oxidation and dry etching
(b) nitride sidewall formation and channel implantation
(c) poly-Si deposition
(d) poly-Si etching and mask oxide removal
(e) LAT(Large-Angle-Tilted) SDE implantation.
(f) n^+ source/drain implantation.

The process steps for the proposed ESD MOSFET are shown in Fig. 1. After the mask oxidation on p-type (100) Si wafer, the channel region is opened by dry-etching [5]. Silicon surface is etched to the depth of X_R. Nitride is deposited and etched to form inverted sidewall spacers which have width of W_S. These structural parameters have powerful influence on the device characteristics such as short-channel effects and driving capabilities because they determine the shape of the SDE regions. In this work, W_S and X_R are selected 20nm and 30nm respectively to effectively suppress the short-channel effects. B^+ ($4\times10^{12}cm^{-2}$, 45keV) and BF_2^+ ($8\times10^{12}cm^{-2}$, 90keV) implantations are

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