A New Self-Aligned Asymmetric Structure (SAAS) for 0.1μm MOSFET Technology

Chang-Soon Choi, Kyung-Whan Kim and Woo-Young Choi

Department of Electrical and Computer Engineering, Yonsei University, Seoul, 120-749, KOREA
E-mail: *mosoon@semicon4.yonsei.ac.kr,* ***Tel:*** *+82-2-361-2874*

Suggested Area : Silicon Devices and Technology

Abstract **— A new Self-Aligned Asymmetric Structure (SAAS) which has asymmetric halo at the highly doped source extension is proposed and optimized for sub-0.1μm MOSFET technology. The fabrication process for the asymmetric structure requires no additional masks. The hydrodynamic device simulation coupled with process simulation shows that the highly doped asymmetric halo enhances the velocity overshoot at the source side and suppresses the short channel effects. The degradation of device performance caused by increased resistance in the highly doped halo is reduced by the asymmetric drain structure with low parasitic resistance.**

I. Introduction

The demands for higher performance and density of integrated circuits have led to the scaling of MOSFET's down to the 0.1μm dimension. As MOSFET shrinks to sub-0.1μm regime, velocity overshoot is expected to be one of the important physical phenomena because it is directly related to the improvement of device performance [1]. However, the adverse effect caused by substantially increased parasitic resistance in LDD region degrades driving capability. To enhance the device performance, higher doping concentration in LDD region is necessary, but this imposes negative effects on the reliability problems such as hot carrier effects and punchthrough phenomena.

To improve the device performance without sacrificing hot-carrier reliability, several asymmetric MOSFET structures have been reported [2-5]. Asymmetric LDD structures have been proposed [2-3] for reducing parasitic resistance and maintaining hot carrier reliability. However, as the devices are scaled down, these structures aggravate the short channel effects because they have LDD extension only on the drain side. Lateral Asymmetric Channel structures have been proposed [4-5] in order to take full advantage of velocity overshoot effect and suppress the short channel effects with asymmetric halo doping at source region. To fully suppress the short channel effects and enhance the velocity overshoot, higher halo doping is required. However, it causes serious degradation of device performance due to increased parasitic source resistance [6]. In addition, the fabrication processes of previously reported asymmetric structures has a poor feasibility in sub-0.1μm regime because they require additional masks and precise alignment.

In this work, we propose a new Self-Aligned Asymmetric Structure (SAAS) to solve these problems. And we compare the new structure with previously reported asymmetric structures on the device performance, reliability and short channel effects using TSUPREM-4 and MEDICI [7-8].

II. Proposed Structure & Process

Fig. 1 schematically illustrates the fabrication process sequence for SAAS. After 38Å thick gate oxide is grown on (100) p-type wafer, poly-Si is deposited. Poly-Si is doped with $POCl_3$ and the pad oxide is deposited on the poly-Si. Next, the pad oxide on the gate-source area is etched away using dry etching process. Nitride film is deposited and etched to form a sidewall as shown in Fig. 1(C). In the sidewall formation, the thickness of nitride film determines the poly gate length. This sidewall masking technique was employed in 0.1μm MOSFET and reported to have better uniformity of line width compared with e-beam lithography [9]. After the exposed poly-Si is anisotropically etched, highly doped source extension is formed by As^+($1\times10^{15}cm^{-2}$, 10keV) implantation. And asymmetric halo implantation with BF_2^+ ($2\times10^{13}cm^{-2}$, 65keV, 25°) is performed to make lateral asymmetric channel profile. In order to prevent damages during etching and implantation steps, nitride is deposited for capping the source region and etched by dry etching or CMP until the pad oxide reveals as shown in Fig. 1(E). After the pad oxide is etched by HF, the exposed poly-Si is etched by dry etching. Lightly doped drain extension is formed by As^+(5×10^{13} cm^{-2}, 10keV) implantation. The remaining nitride is removed by H_3PO_4. After the 1000Å side-

(0-7803-6304-3/00/$10.00 ©2000 IEEE)