A Novel Charge Pump PLL with Reduced Jitter Characteristics

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Abstract

A new charge pump structure is proposed that can improve jitter characteristics of a Phase-Locked Loop (PLL) by blocking the control voltage leakages. The new structure also has low power consumption because it uses a self-biased method that switches the current flow only on demand. A PLL with the proposed charge pump is designed with 0.6㎛ CMOS process technology and evaluated by post-layout simulation.

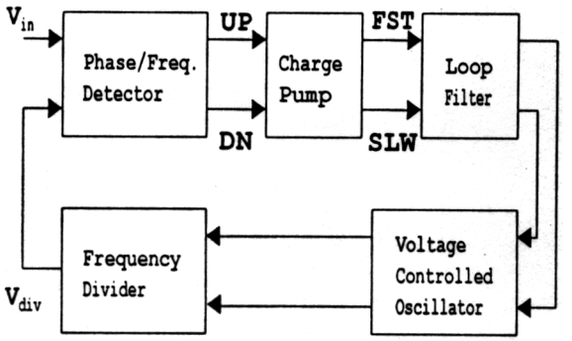

Fig 1. Block diagram of PLL

PLL optimization for high frequency operation has been studied by many researchers(1-3). The PLL structure can be divided into five parts as shown in Fig 1. The phase/frequency detector (PFD) detects the phase difference between external input signal V_{in} and frequency divider's output signal V_{div}, and produces UP and DN signals that, through the charge pump and the loop filter, control Voltage Controlled Oscillator (VCO). When PLL is locked, two outputs of PFD should be the same and the charge pump output should be constant. In practice, however, this does not happen as the charge pump circuit usually has asymmetric features that cause VCO control voltage changes and PLL output frequency noises. A new charge pump structure is proposed that minimizes this problem.

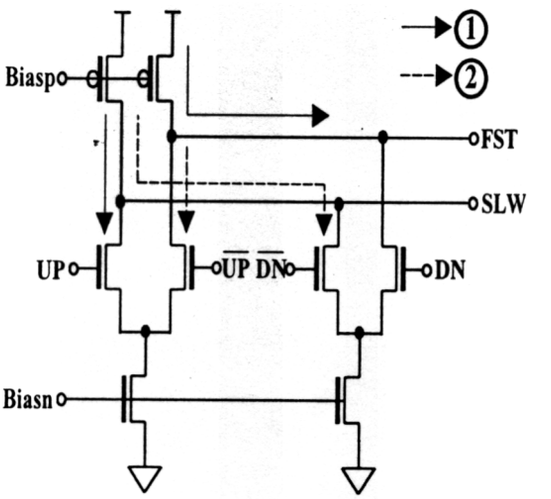

Fig 2. Conventional charge pump

Figure 2 shows a conventional structure for

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the charge pump. When UP signal is logic '1' and DN signal logic '0', FST node is charged and SLW node is discharged. When PLL is locked, UP and DN signals are both logic '0', except during PFD's reset time in which case they are logic '1'. When UP and DN are logic '0', current path ② is established, and when they are logic '1', current path ① is established. Consequently, even when PLL is locked, path ① and ② consume power. In this case, the current driving ability of PMOS is lower than NMOS if the control voltage is higher than the bias voltage (1.65V). Such changes in the control voltages cause noises in VCO output. As the difference between the charge pump's output voltages and the bias voltage increases, the voltage change increases.

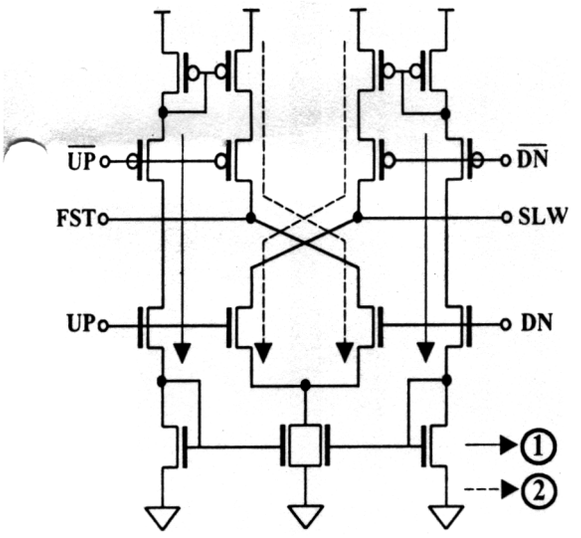

Fig 3. Proposed charge pump

A new charge pump structure that minimizes such a problem is shown in Fig 3. The suggested charge pump uses a self-biased method and functions as a differential charge pump. It has current mirrors which establish current path ② from path ①. When PLL is locked, UP and DN signals are logic '0', and PMOS and NMOS are both turned off. The control voltage is constant because FST and SLW node's current paths are blocked. As a result the PLL output noise is reduced.

Two PLL circuits including structures shown in Fig. 2 and Fig. 3 are designed with 0.6 ㎛ CMOS process parameters.

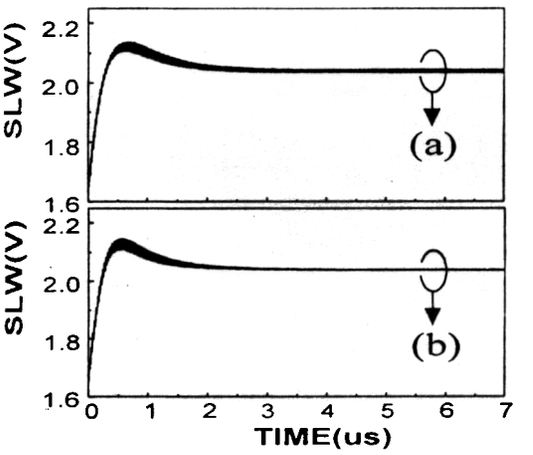

Fig 4. The control voltage of the PLL
(a) Conventional (b) Proposed

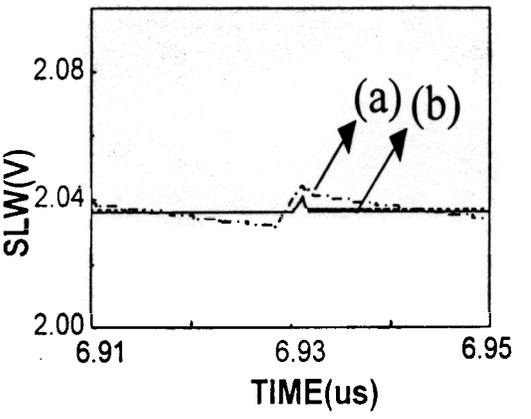

Fig 5. Magnification of Fig 4.

Conventional configurations are used for PFD and VCO. The VCO center frequency is 650MHz. The simulation results for 28ns input period is shown in Fig. 4 and 5. Figure 4 (a) and (b) are SLW node voltages for a PLL with conventional and proposed charge pump

structures, respectively. As can be seen, the proposed charge pump has much reduced SLW node voltage changes. Figure 5 shows the magnified waveforms.

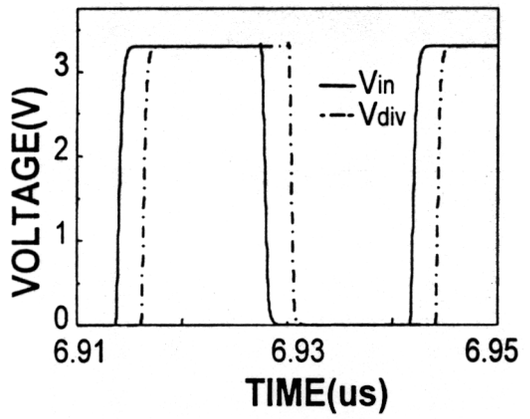

Fig 6. Input/output waveforms of conventional charge pump PLL

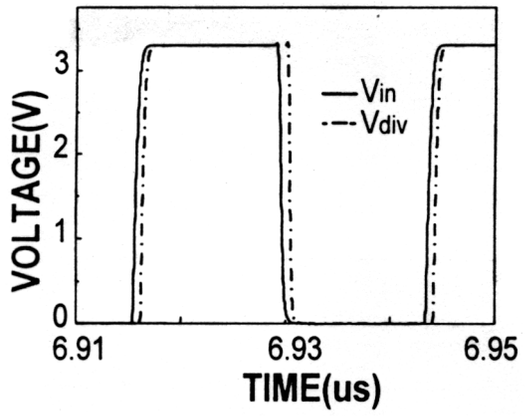

Fig 7. Input/output waveforms of proposed charge pump PLL

Figure 6 shows Input/output waveforms of conventional charge pump PLL with 28ns input period and Figure 7 shows that of proposed charge pump PLL. Comparing Fig. 6 with Fig. 7, proposed charge pump also reduces phase offset of PLL.

Conclusion

A new charge pump PLL was proposed and designed. The design was done with 0.6㎛ CMOS process parameters for +3.3V power supply. Post-layout simulation shows that the proposed circuit has reduced leakage currents for VCO control voltages and, consequently the VCO output frequency is more stable.

Reference

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