A Novel 10GHz-Range Voltage-Controlled Differential Ring Oscillator

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Abstract: In this paper, a novel 10GHz-range voltage-controlled differential ring oscillator is proposed. It consists of a 2-stage differential ring oscillator and a differential amplifier which differentially amplifies two signals from common-source of each stage. A signal from the common-source of differential inverter depends on both two inputs, and therefore, when the 2-stage differential ring oscillator oscillates with f_{osc}, the frequency of the signals at common-source of each stages is exactly $2f_{osc}$. By using this, a 10GHz-range oscillator was designed with 0.5μm GaAs MESFET and its performance was evaluated by SPICE simulation. From the simulation results, it was shown that 10GHz-range output signals could be obtained by the proposed VCO which would be very difficult obtained with conventional ring oscillators.

I. INTRODUCTION

The demand for high speed communication systems has increased the need for high-frequency phase-locked loops(PLLs). PLLs are generally used to implement frequency synthesizers or clock/data recovery circuits included in most high-speed data processing systems[1]. Especially, as the operating frequency of the system increases, fully differential PLLs (Fig. 1) are preferred because of their high stability on noises such as temperature, process parameters, and power supply variations. As shown in Fig. 1, a PLL consists of five major blocks; phase/frequency detector(PFD), charge pump, loop filter, voltage-controlled oscillator(VCO), and frequency divider. Of these, VCO is the critical building block which determines the output frequency of PLL. Therefore, there have been many efforts to increase the output frequency of VCO, and presently, several GHz-range VCO's have been implemented[1-3].

With this trend, a novel 10GHz-range voltage-controlled differential ring oscillator is proposed in this paper, as a part of implementation of 10GHz-range PLL. Proposed VCO is designed with 0.5μm GaAs MESFET, and its performance is evaluated by SPICE simulation.

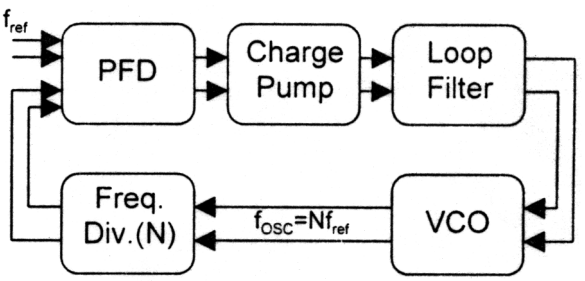


Fig. Fully differential PLLs.

II. CONVENTIONAL RING OSCILLATOR

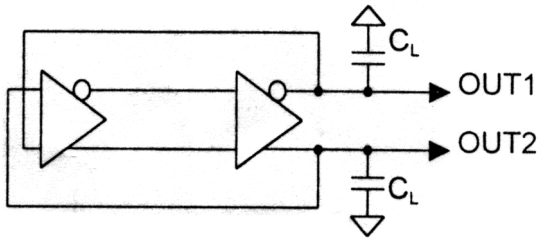
A voltage-controlled oscillator(VCO) outputs a signal whose oscillating frequencies are determined by the input control voltages. Although there are many types of VCOs, a differential ring type is adopted for our VCO because it can be integrated with the overall system in one chip. Schematic diagrams of conventional differential ring oscillators are shown in Fig. 2. When a differential inverter is used as a delay cell, either even(Fig. 2(a)) or odd(Fig. 2(b)) stages of ring oscillator can be implemented.

The oscillation frequency(f_{osc}) of a conventional N-stage ring oscillator is determined by Eq. (1),

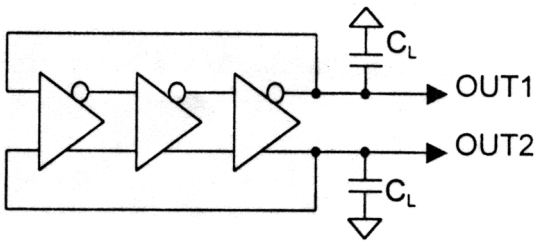
$$f_{OSC} = (2NT_D)^{-1} \qquad (1)$$

where, N is the number of stages and T_D is the propagation delay time for the delay cell. From Eq. (1), it is clear that N and T_D must be minimized in order to

maximize the oscillation frequency of a ring oscillator. However, N is limited to be more than 2 by the oscillation conditions and T_D is limited by the process technology. In xample, in order to obtain an oscillation frequency of 10GHz from 2-stage ring oscillator, T_D of a delay cell must be at least 25ps, which is very difficult to implement with a conventional structure even though a state-of-the-art process technology such as 0.5㎛ GaAs MESFET process is used. Moreover, since the conventional ring oscillator outputs a signal directly from the main feedback loop, an additional load capacitance(C_L) is induced in the loop and this makes the oscillation frequency to be reduced and varied with the load. Therefore, a novel structure of ring oscillator must be needed to solve these problems.



(a) Even number of stages.



(b) Odd number of stages.

Fig. 2 Conventional differential ring oscillators.

III. PROPOSED VCO

Fig. 3 shows the proposed GaAs MESFET differential inverter. It consists of a differential amplifier and two source followers. This differs from a conventional differential inverter in that the proposed circuit has an additional output port(OUT3) at the common-source of the differential amplifier. When two periodic signals (V_{Bias}+Asin(wt), V_{Bias}-Asin(wt)) are differentially applied the input ports(IN1, IN2), the output signal V(OUT3) can be expressed as Eq. (2), by assuming that the output resistance of the current source(J3, R3) is infinite and FET J1 and J2 operate in the saturation region.

$$V(OUT3) = V_{Bias} - V_{th} - \sqrt{\frac{I_O}{2K} - A^2 \sin^2(\omega t)} \quad (2)$$

where, V_{th} and K is the threshold voltage and the transconductance factor of J1 and J2, respectively, and I_O is the output current of the current source. From Eq. (2), it can be seen that the waveform of V(OUT3) is repeated at every half of the input period. So, if a N-stage ring oscillator composed of the differential inverters oscillates with the frequency of f_{osc}, the frequency of OUT3 signals of each differential inverters becomes $2f_{osc}$, just twice of that of the main feedback loop.

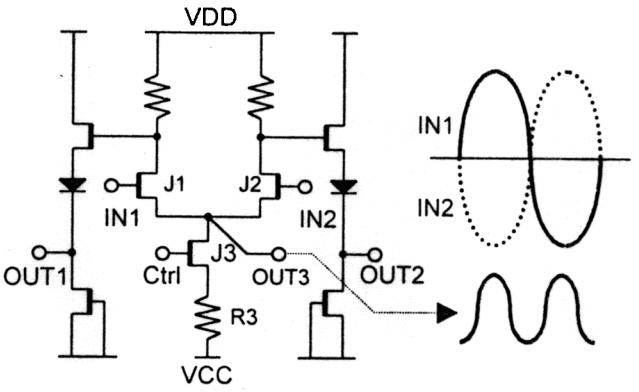


Fig. 3 Proposed differential inverter and its large-signal characteristics.

However, those signals cannot be directly used as outputs because they contain a component which depends on the common variations of the input signals. In other words, if the bias level of two differential input signals or two branch currents(I_{ds}'s of J1 and J2) are commonly changed by noises such as temperature, process parameters, or power supply variations, the voltage level of common-source node of differential inverter is also changed to keep the output current of current source constant. Also, because the magnitude of OUT3 signals are small compared with that of main feedback loop, some processes must be included to remove the noise-dependent components in OUT3 signals and to amplify the magnitude of OUT3 signals. This can be done by differentially amplifying two OUT3 signals whose phase difference is 180° as shown in Fig. 4.

Fig. 4 shows the proposed 2-stage differential ring

oscillator. As shown in figure, the phase differences of each input and output pairs are 90° so that the phase difference of input pairs of the first delay cell and output pairs of the second delay cell is to be 180°. So, the phase difference of $OUT3_1$ and $OUT3_2$ becomes 180°, and therefore, two differential outputs which have the frequency of $2f_{osc}$ and are highly stable on the above noises can be obtained by differentially amplifying them.

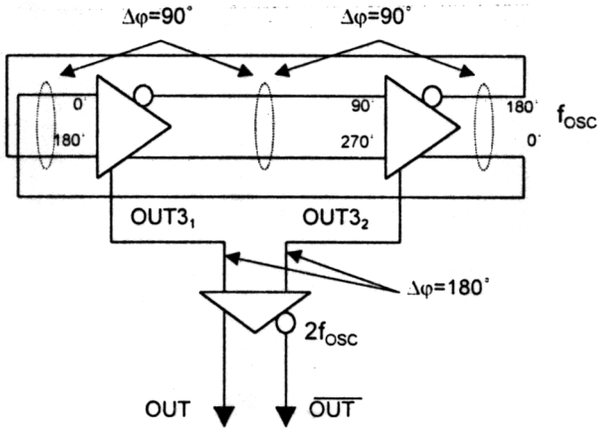


Fig. 4 Proposed 2-stage differential ring oscillator.

IV. SIMULATION RESULTS

The proposed VCO was designed with 0.5㎛ GaAs MESFET and its performance was evaluated by SPICE simulation. To guarantee the reliability of simulation results, some estimated parasitic capacitors are included at each node of the circuit.

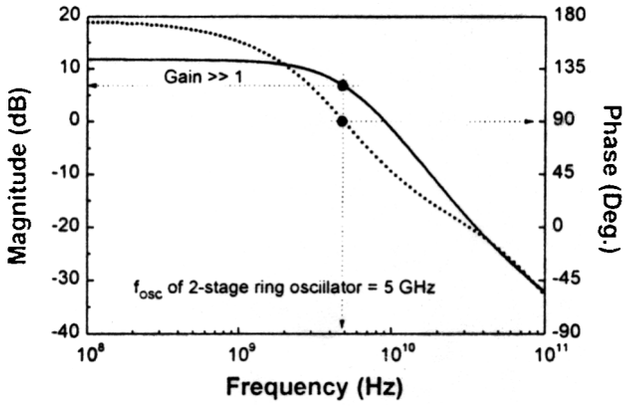


Fig. 5 AC characteristics of proposed differential inverter.

Fig. 5 shows the AC characteristics of the differential inverter used as a delay cell in proposed VCO. In order that 2-stage differential ring oscillator is in the oscillation state, the phase difference between two inputs and two outputs of differential inverter is to be 90° and at this, its small-signal gain must be more than 1. From Fig. 5, it can be seen that this differential inverter can be used as a delay cell of 2-stage ring oscillator, and its oscillation frequency will be about 5GHz.

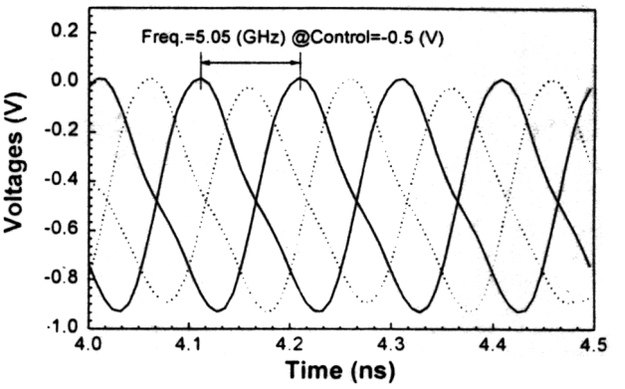


Fig. 6 Output waveforms of main feedback loop.

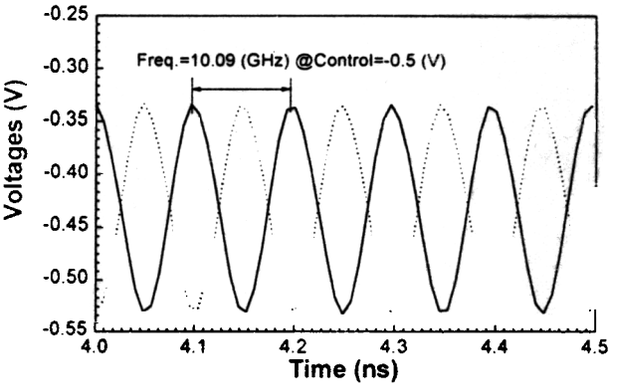


Fig. 7 Output waveforms of $OUT3_1$ and $OUT3_2$.

Fig. 6 shows the output waveforms of the main feedback loop. In this figure, solid lines and dotted lines represent two outputs of the first and second stages, respectively. As shown in this figure, the oscillation frequency of the main feedback loop is 5.05GHz. And, Fig. 7 shows the output waveforms of the common-source node of each differential inverters($OUT3_1$ and $OUT3_2$).

From the figure, it can be seen that the frequency of $OUT3_1$ and $OUT3_2$ is 10.09GHz which is just twice of that of main feedback loop signals(5.05GHz) and the phase difference between them is 180°. However, The magnitude of OUT3's is about $0.2V_{p-p}$ which is small compared to the minimum ECL output level. And as mentioned above, since they contain common noise components, it is needed to differentially amplify them. Final output waveforms of proposed VCO are shown in Fig. 8. In this figure, the waveforms at minimum, center, and maximum frequencies are shown together. As shown in this figure, the magnitude of VCO output is in the range of $0.47\sim0.53V_{p-p}$ and their common-mode voltages vary from -1.36V to -1.27V. This variation of the output bias level will be reduced by increasing CMRR of differential amplifier.

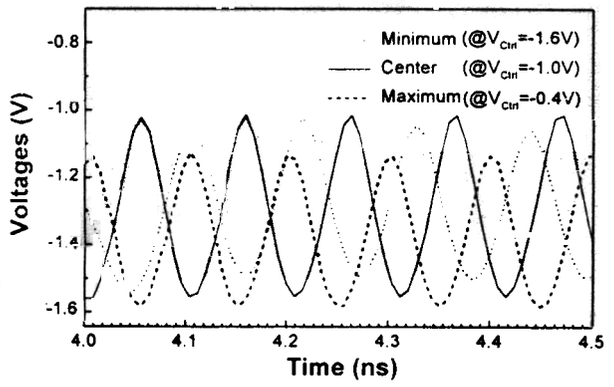


Fig. 8 Output waveforms of proposed VCO.

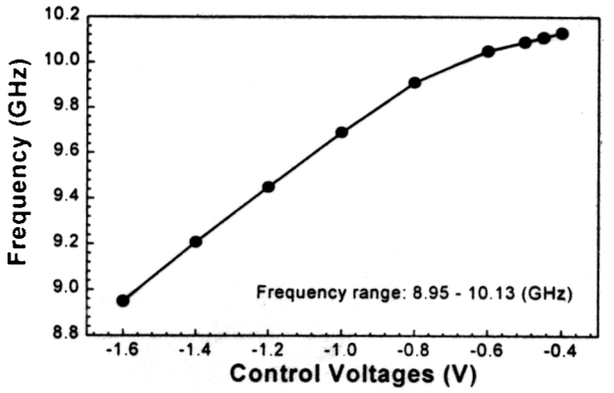


Fig. 9 Tuning sensitivity of proposed VCO.

Fig. 9 shows the tuning sensitivity of proposed VCO. As shown in this figure, the output frequency of proposed VCO varies from 8.95GHz to 10.13GHz when the control voltage varies from -1.6V to -0.4V. The tuning sensitivity of proposed VCO is about 980MHz/V. It is expected that the proposed differential ring VCO can be successfully applied to 10GHz-range PLL.

V. CONCLUSION

In this paper, a novel 10GHz-range voltage-controlled differential ring oscillator was proposed and its performance was evaluated with SPICE simulations. Proposed VCO consists of a 2-stage differential ring oscillator which oscillates with the oscillation frequency of f_{osc} and a differential amplifier which differentially amplifies two common-source signals of each stages having the oscillation frequency of $2f_{osc}$. Therefore, proposed VCO can output very high frequency signals as twice as the conventional one. With SPICE simulation, it was shown that the output frequency of proposed VCO is about 10GHz. This result shows that the proposed VCO can obtain 10GHz-range outputs, which would be difficult with the conventional schemes. More detail specifications of proposed VCO is in table 1.

Table 1. Specifications of proposed VCO.

Maximum output frequency	10.13GHz
Output frequency range	8.95 ~ 10.13GHz
Control voltage range	-1.6 ~ -0.4V
Output level	-0.32±0.25V
Technology	0.5㎛ GaAs MESFET
Power supply	+3.3V/-2.0V
Power dissipation	about 250mW

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