Design of Charge-Pumped Loop Filter for GHz-Range Phase-Locked Loops with GaAs MESFET

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Abstract: In this paper, a charge-pumped loop filter for GHz-range phase-locked loops(PLLs) was designed using 1.2 ㎛ GaAs MESFET. The characteristics of charge-pumped loop filter and the stability of PLL system including this circuit were analyzed. Some measures to evaluate the performance of the charge-pumped loop filter were defined, and based on these definitions, the performance of the proposed circuit was verified by SPICE simulation.

1. Introduction

The demand for high-speed communication systems have increased the need for high-frequency PLL. The PLL, one of the critical parts of communication system has three major blocks; a voltage-controlled oscillator(VCO), a phase/frequency detector(PFD)[1] which compares the phase and frequency of input reference signal with that of an output signal of VCO, and a loop filter(LPF) which is generally comprised of RC low-pass filter and converts the output of PFD into the control voltage of VCO.

In ideal cases, when the PLL is locked with an input reference signal having a constant frequency, the control voltage of VCO should be unchanged so that the frequency of the output signal of VCO is equal to that of the input signal. In real cases, however, there is an output decaying of PFD due to discharging of capacitors and this results in a periodic frequency ripple of the output of VCO. Furthermore, when the PLL is locked at a frequency which is different to the free-running frequency of VCO, there always exists a static phase error[2]. To solve this, a circuit so called charge pump had been introduced [2]. A charge pump is located between PFD and loop filter, and can be modeled as an electric switch which cuts off the conduction path between PFD and loop filter electrically when the PLL is locked. In this paper, the charge pump and loop filter are named as a charge-pumped loop filter because these two circuits must be considered together.

Although a charge-pumped loop filter is generally included in most present PLLs, some measures to evaluate the performance of it have not been proposed.

In this paper, four measures were defined to do this, and a charge-pumped loop filter integrated circuit for GHz-range PLL is designed with 1.2 ㎛ GaAs MESFET. Finally, the performance of proposed circuit is verified by SPICE simulation.

2. Charge-Pumped Loop Filter

2.1 Architecture and Its Behavior

A charge-pump PLL system is shown in Fig. 1. The charge-pumped loop filter is connected between PFD and VCO, and generates two differential mode control voltages for VCO according to the outputs of PFD.

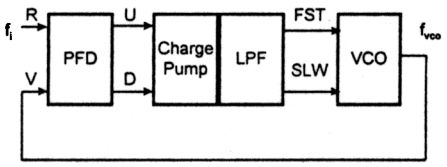

Fig.1 A block diagram of charge-pump PLL

This circuit can be conceptually modeled as shown in Fig. 2[2]. It consists of two independent current sources, two ideal electric switches controlled by two outputs of PFD, U and D, respectively, and a simple RC loop filter. PFD can produce three different output states; U is HIGH and D is LOW when the rising/falling edge of an input reference signal is prior to that of the output of VCO, U is LOW and D is HIGH when the rising/falling edge of the output of VCO is prior to that of an input reference signal, and U and D are both LOW when both two rising/falling edges are coincident[3]. According to the output state of PFD, output voltage of charge-pumped loop filter increases, decreases or unchanges.

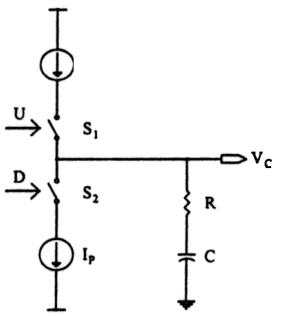

Fig.2 A conceptual model of charge-pumped loop filter

Although there are several possible implementations, we selected a second order active loop filter as shown in

Fig. 3[2]. In this circuit, C_1 is used to alleviate the slew rate limitation of op-amp and C_2 acts just like C in Fig. 2.

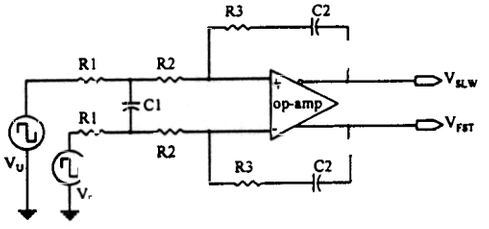

Fig.3 A second-order charge-pumped loop filter

If the op-amp is an ideal one, two inputs of op-amp are always same so that no current path exists for C_2 when both inputs of charge-pumped loop filter, U and D are LOW. The transfer function of this circuit, H(s), is

$$H(s) \equiv \frac{V_{FST}(s)-V_{COM}(s)}{V_U(s)-V_D(s)} = \frac{V_{SLW}(s)-V_{COM}(s)}{V_D(s)-V_U(s)}$$

$$= \frac{1}{2}\frac{1}{R_1+R_2}\cdot\frac{1+sC_2R_3}{sC_2}\cdot\frac{1}{1+2sC_1(R_1\|R_2)} \quad (1)$$

where $V_{COM}(s)$ is the common-mode voltage of two outputs, $V_{FST}(s)$ and $V_{SLW}(s)$. Using Eq. (1), the step response of the charge-pumped loop filter can be easily derived as

$$v_{FST}(t) = \frac{V_P}{2(R_1+R_2)C_2}t + \Delta V_j \cdot \left[1-e^{-\frac{1}{2C_1(R_1\|R_2)}t}\right] \quad (2)$$

where V_P is the magnitude of input pulse and ΔV_j is

$$\Delta V_j = V_P\frac{C_2R_3-2C_1(R_1\|R_2)}{2C_2(R_1+R_2)} \quad (3)$$

If the input pulse width is τ, the increment of output voltage after the input pulse is applied, ΔV_C, is

$$\Delta V_C = \frac{V_P}{2(R_1+R_2)C_2}\tau \quad (4)$$

Fig. 4 shows the output waveform of charge-pumped loop filter when a pulse input is applied.

2.2 Stability

Relationships between resistors and capacitors in Fig.3 can be determined by the stability conditions derived from the closed-loop transfer function of PLL[2]. Although some researches on the stability of a charge-pumped loop filter using second-order passive filter had been done in Ref. [2] and [3], there has been no accurate interpretation about the stability of charge-pumped loop filter using second-order active filter. However, by redefining some parameters, the stability problem of second-order active filter can be approximately equalized with that of passive filter.

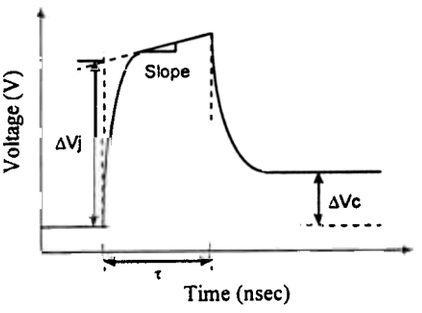

Fig.4 An output waveform of the charge-pumped loop filter

The equivalent impedance of the second-order active filter shown in Fig.3, Z(s), is

$$Z(s) = \left(\frac{b-1}{b}\right)\cdot\frac{s\tau_2+1}{sC_2\left(\frac{s\tau_2}{b}+1\right)} \quad (5)$$

where b and τ_2 are defined as

$$b \equiv \frac{C_2R_3}{2C_1(R_1\|R_2)}, \quad \tau_2 \equiv C_2R_3 \quad (6)$$

And the closed-loop transfer function of the charge-pump PLL system, H(s), is

$$H(s) = \frac{K\left(\frac{b-1}{b}\right)\left(s+\frac{1}{\tau_2}\right)}{\frac{s^3\tau_2}{b}+s^2+K\left(\frac{b-1}{b}\right)s+\frac{K(b-1)}{b\tau_2}} \quad (7)$$

where the loop gain K is

$$K = K_VV_P\frac{C_2R_3-2C_1(R_1\|R_2)}{2C_2(R_1+R_2)} \quad (8)$$

where K_V is the VCO gain and its unit is [MHz/V].

Since the parameters b, τ_2, and K are redefined, the stability limit of second-order loop filter can be obtained by the method in Ref. [2]. This limitation determines the relationships between R_1, R_2, R_3, C_1, and C_2. From this limitation, the numerical values can be determined as; R_1=400, R_2=400, R_3=150, C_1=1pF, C_2=0.2nF

2.3 Specifications

Several basic specifications are shown in table 1. They are the requirements in our 1 ~ 3 GHz-range PLL system.

Table 1. Several basic specifications

Contents	Specifications
Input pulse level	-0.705V/-0.26V
Output range	-0.4825V ± 0.5V
Power supply	+3.3V/-2.0V
Maximum operating frequency	more than 300MHz
Power dissipation	less than 500mW

Although a charge-pumped loop filter is generally used in present PLLs, some measures to evaluate the performance of charge-pumped loop filter have not been proposed. In this paper, four measures are defined to do this and they are as follows:

Maximum output current: The output current of charge pump flows into or out of capacitor C_2. This can be increased by reducing the numerical values of R_1,R_2, and R_3, while maintaining its ratio. Larger output current means that the charging or discharging of C_2 can be made faster, i.e. the desired increment or decrement of output voltage of charge-pumped loop filter can be obtained by narrower input pulse width. However, when the output current of charge pump increases, the common-mode voltage of output port, V_{COM} decreases due to the non-zero output resistance of op-amp. In this paper, the maximum output current is defined as the current which maintains the relative error of V_{COM} within 0.5%.

Minimum input pulse width: This means the minimum input pulse width which can generate the output waveform as predicted in Eq. (3) and (4). This definition may be meaningless because the charge-pumped loop filter takes the output of PFD as its input, and when the PLL is locked, the input pulse width is to be 0. However, this is a good measure to evaluate how accurately it can operate. In this paper, the minimum input pulse width is defined as less than 3.3ns which corresponds to the maximum operating frequency, 300MHz.

Symmetry: The symmetry of two outputs of charge-pumped loop filter, V_{FST} and V_{SLW} is a very important property which affects on the performance of PLLs. This can be defined as two types; one is the symmetry between the increment or decrement of one output and that of the other, and the other is the symmetry between the increment and decrement of both two outputs.

Hold time: An ideal charge-pumped loop filter has an infinite hold time. This means that the output voltage is unchanged when the PLL is locked. However, the output of a real circuit is exponentially decayed toward its initial value because the dc gain of op-amp included in that circuit has a finite value. So, to take a maximum advantage from the use of charge-pumped loop filter, the dc gain of the op-amp must be high and the resulting hold time must be long.

2.4 Op-amp Design

As shown in Fig.3, an op-amp for our application must be a differential amplifier which has two differential input and two differential outputs. Its common-mode gain must be small to increase the resistance against the variation of temperature, process parameters, and power supply noises. Also, its differential-mode gain must be high to increase the hold time of the charge-pumped loop filter. By considering this consideration, an op-amp was designed using 1.2 μm GaAs MESFET, which takes the form of three stage cascade structure to obtain high dc gain, and each stage takes the form of a differential amplifier which includes a feedback loop to enhance the CMRR characteristics and a source follower to shift the output level for the next stage. Fig. 5 shows the designed amplifier stage. In this circuit, J3, J4, J6, and J7 form the feedback loop which suppresses the variation of the voltage at node nc by adjusting the gate voltage of J5 and enhances the CMRR. The overall schematic is omitted due to the space limitation. Frequency compensation was performed by capacitive feedback loops between first and third stage and between second and third stage[4].

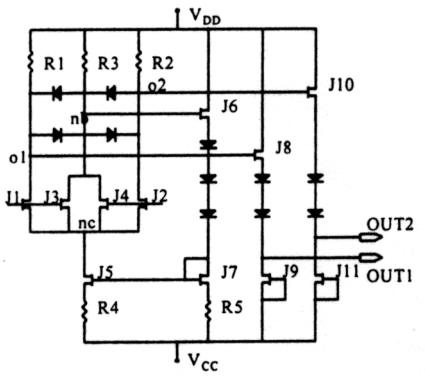

Fig.5 Schematic diagram of a differential amplifier

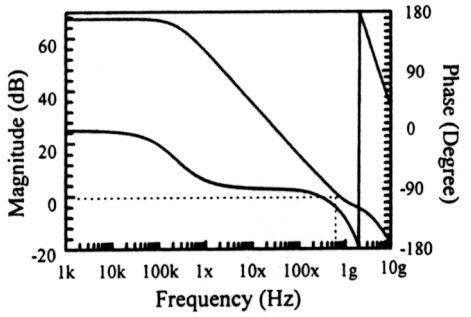

Fig.6 Bode plot of op-amp

Fig. 6 shows the results of simulation to estimate the

performance of designed op-amp. From this figure, it can be seen that dc gain of designed op-amp is 67.4dB, unity-gain frequency is 706MHz, and phase margin is 58°.

3. Simulation Results

The maximum output current of the charge-pumped loop filter was determined by simulation after the capacitors C_2 is removed. When the numerical values of R_1, R_2, and R_3 decrease with same scale factor which is determined by stability limitation mentioned in Sec.2.2, the output current increases. From this simulation, the maximum output current was determined to 0.4954mA at $R_1=R_2=$ 400 Ω, and R_3=150 Ω.

Fig. 7 shows the results of simulation to determine the minimum input pulse width. From this figure, it is verified that our circuit can operate without a significant problem with 1ns input pulse width, and this means that our circuit can operate up to 500MHz and, thus, can be applied to GHz-range PLL systems.

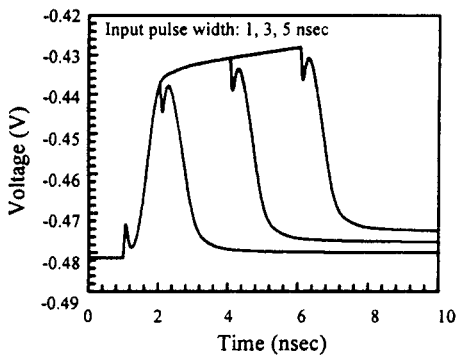

Fig.7 Simulation results to determine the minimum input pulse width

Fig. 8 shows the results of simulation to evaluate the symmetry between two differential mode outputs, FST and SLW, and between increment and decrement of each outputs, following the same amount of U and D pulses. From this figure, the relative error of the output common mode voltage to the initial voltage after 120 U pulses with 4ns period and 50% duty ratio are applied, can be calculated as 0.34%, showing very good symmetry between FST and SLW. Furthermore, since the relative error of one output voltage after same number of U and D pulses to the initial voltage is too small to be calculated, increment of FST or SLW due to U or D input is exactly same as decrement of FST or SLW due to D or U input.

Fig. 9 shows the results of simulation to evaluate the hold times of output voltages. From this figure, the relative errors of two outputs, FST and SLW, to each initial voltage after 50 μs can be calculated as 0.59 and 0.71%, respectively, showing very long hold time.

4. Conclusion

In this paper, a charge-pumped loop filter for GHz-range PLL system was designed using 1.2 μm GaAs MESFET and its performance and characteristics are verified by SPICE simulation. From the above verification, it is expected that our charge-pumped loop filter can be successively applied to GHz-range PLL system.

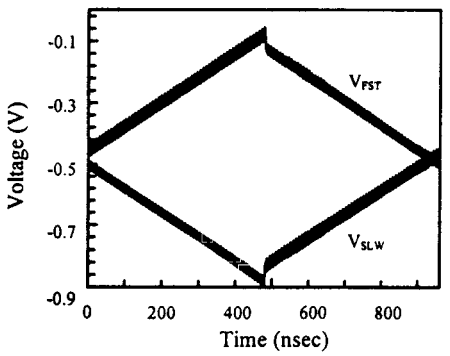

Fig.8 Simulation results to evaluate the symmetry of two outputs.

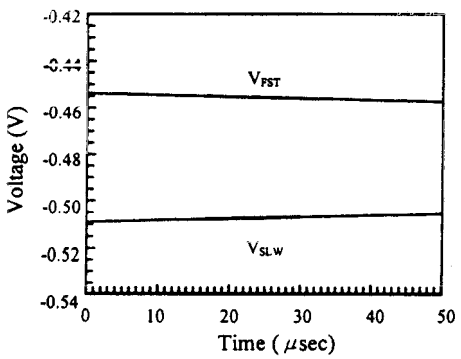

Fig.9 Simulation results to determine hold time

References

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