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Design of A Viterbi Decoder with Sequence-Processing Capability

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Abstract : In this paper, we proposed a Viterbi decoder for practical implementation of Forward Error Correction(FEC). The design was mainly focused on real-time processing by using the memory organization and its control method with constraint length 7, coding rate 1/2. Management of memory contents in a Viterbi decoder is a major design problem for both hardware and software realization. In this design, we solved that problem with sequence processing.

1. Introduction

In many digital communication systems, error correction circuitry is widely used in order to reduce the bit error rate of transmitted data [2,5]. Convolutional coding with Viterbi decoding is a powerful method for forward error correction [1-5]. In present commercial applications, Viterbi decoders with R(coding rate)=1/2 and K(constraint length)=7 are widely used.

A very simple variation of the Viterbi algorithm permits the use of soft-decision demodulated data in which signal values are quantized into multiple levels and digitized [2,5]. The advantage of soft decision demodulation is that the signal values not only indicate whether they represent one or zero, but also indicate the magnitude of the corruption of the signal by noise at the instant of quantization. A significant processing gain can be achieved by using soft decision data, typically about 2 dB for 3-bit data.

We designed a Viterbi decoder that has R=1/2, K=7 and 3-bit soft decision. Our design has a trace-back architecture and achieves tracing, updating and storing of the real-time sequences within a single clock cycle.

2. Viterbi Algorithm

The Viterbi algorithm performs the maximum likelihood decoding [1-5]. The advantage of Viterbi decoding is that the complexity of the decoder is not a function of the number of symbols in the codeword sequence [2]. The algorithm determines a measure of similarity between received signals, at time t_i, and all the trellis paths entering each state at time t_i. Then, it removes trellis paths that can not be a candidate for the maximum likelihood choice. When two paths enter the same state, the one having the smallest metric is chosen. This path is called the survivor path. The selection of survivor path is performed for all the states. The decoder continues in this way and makes decisions by eliminating the least likely paths [2-5]. The early rejection of the unlikely paths reduces the decoding complexity [2].

Viterbi decoder has three major parts. The first part calculates branch metrics. The branch metric is the likelihood metric of received codes, and is calculated based on the comparison between the trellis and received convolutional codes [2-5]. The second part is "Add-Compare-Select(ACS)" part. In ACS, path metrics are updated by adding branch metrics associated with each possible state transition [6]. The number of states N_s of a convolutional encoder which generates n encoded bits is a function of the constraint length K and input bits b [1,2].

$$N_s = 2^{b(K-1)} \quad (1)$$
$$R = b/n \quad (2)$$

The third part performs path selection and memery manangenent. The smaller path metric is the path metric for the state and the resulting decision is stored in the survivor sequence memory management unit where the most likely path is determined [6]. Fig. 1 shows the block diagram of the whole Viterbi decoder.

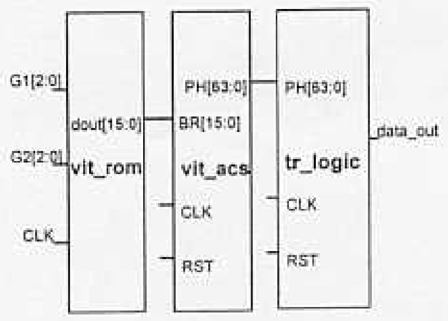

Fig. 1 Block diagram of the Viterbi decoder

3. The Sequence Processing

The sequence processing means that data come out without suspension. When the data are sent to destination, the time it takes for the decoder to correct the errors in data degrades system performance. To solve this problem, our decoder is designed with sequence-processing capability. This makes it possible to implement the decoder with real-time processing [6].

Forney has shown that if τ, defined as memory path, is on the order of five times the encoder memory or more, decoding decision is maximum likelihood [8]. Thus, the value traced back with enough depth in any state converges into a fixed position. This property can be implemented by four RAMs.

Table 1 shows the sequence processing using four RAMs. At t0, 64 state values are written into RAM0. At t1, they are also written into RAM1. At t2, they are written into RAM2, and the state values written in RAM1 are read. At t3, they are written into RAM3 and the state values written in RAM0 are read. The state values read in RAM0 are decoded in tr_back module and decoded data are written in TB_RAM0. At the same time, the state values written in RAM2 are read to find convergence value in RAM1. At t4, they are written into RAM0, and the state values written in RAM1 are read. Then, they are decoded in tr_back module and decoded data are written into TB_RAM1. Simultaneously, the state values written in RAM3 are read to find convergence value in RAM2 and the decoded data written in TB_RAM0 are read. After this, decoded data come out of the Viterbi decoder continuously, and the process is similar to what was performed at t4. Fig. 2 shows the block diagram of the hardware implementation of trace-back logic which performs the sequence processing. Fig. 3 shows the tr_back module which actually performs the trace-back operation.

	t0	t1	t2	t3	t4
RAMA addr_1	Write 0→127			Read 127→0	Write 0→127
RAMB addr_2		Write 0→127	Read 127→0		Read 127→0
RAMC addr_1			Write 0→127	Read 127→0	
RAMD addr_2				Write 0→127	Read 127→0
TB_ RAM0 addr_2				Write 0→127	Read 127→0
TB_ RAM1 addr_1					Write 0→127

Table 1. Management of memory for the Sequence Processing

4. Simulation and Layout Results

To confirm the operation of Viterbi decoder designed for real-time processing, we performed simulation with VHDL(Very high speed integrated circuit Hardware Description Language) [7]. We also performed the gate level simulation. Viterbi decoder designed in this paper was simulated and synthesized. As test bench, we put '1', '1', '0', '0', '1', repeatedly. Fig. 4 shows the gate level simulation results which make it possible to confirm the sequence processing.

Fig. 5 shows layout of our Viterbi decoder. The design was done with a standard 0.6 μm CMOS process and 2-layer metal technology. It is composed of logic circuit with 15,887 gates, four 128×64 RAMs, two 128×1 RAMs, and one 64×16 ROM. It runs on a 3.3 V supply and operates at 20 MHz. The estimated power consumption is 120 mW and the chip size is about 4 mm × 4 mm.

5. Conclusion

We have designed Viterbi decoder which performs the sequence processing. Trace-back logic architecture is based on the management of the memory contents. The operation of our design was confirmed with VHDL simulation, and the actual circuit was synthesized and laid-out.

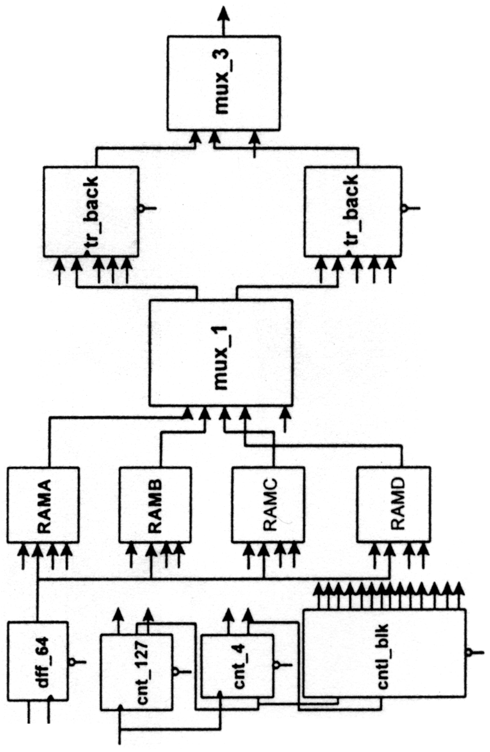

Fig. 2 Block diagram of trace-back logic

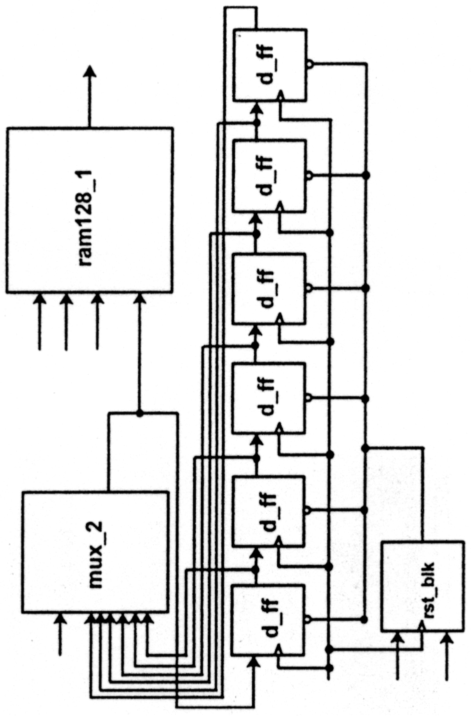

Fig. 3 Block diagram of tr_back

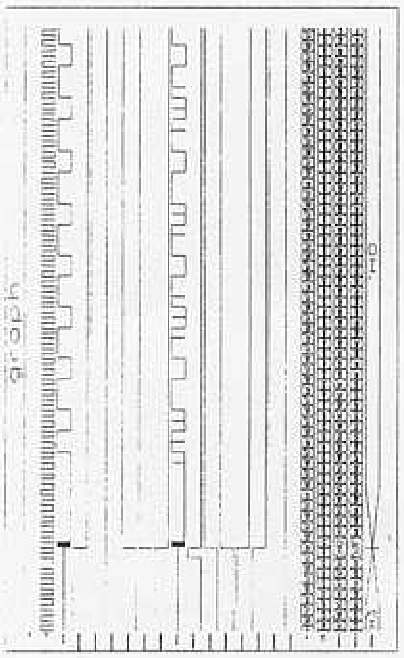
Fig. 4 Gate level simulation results

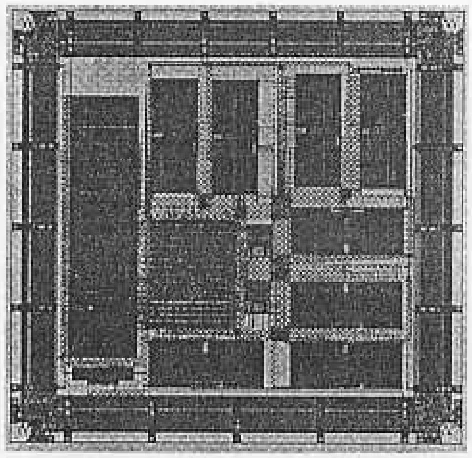
Fig. 5 Layout of designed Viterbi decoder

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