Proceedings of ITC-CSCC '96, July 15-17, 1996, Seoul, Korea

Design of High-Speed Voltage-Controlled Ring Oscillator with Reduced Gain

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Abstract

A monolithic Voltage-Controlled Ring Oscillator (VCRO) which is a key element in phase-locked loop (PLL) is designed with new architecture that has oscillation frequency range of 2.47 to 3.01 GHz and gain of only 540 MHz/V. VCRO gain reduction is desired as the stability of PLL employing VCRO is inversely proportional to VCRO gain. New VCRO is implemented with GaAs MESFET and its simulation results are presented.

Introduction

Ever-increasing speed of present-day communication networks requires faster and faster electronic circuits that make up communication systems. One important element of such systems is Phase-Locked Loop (PLL) that is widely used for data recovery. Consequently, it is very important to design and implement high-speed, high-performance PLL. In this paper, we present a new type of monolithic Voltage-Controlled Ring Oscillator (VCRO), which is an important part of PLL as it determines the maximum obtainable speed of PLL [1]. In general. the higher operating frequency of VCRO is, the larger VCRO gain, defined as the change in oscillation frequency per unit control voltage, becomes due to the structure of ring oscillator that makes up VCRO. In high-speed VCRO, however, too large VCRO gain is undesirable since PLL stability is inversely proportional to VCRO gain [2]. This is especially the case with MESFET-base VCRO as the available control voltage range is only about one volt. So, we came up with a new VCRO structure that has about 2.7 GHz center oscillation frequency with gain of only 540 MHz/V to realize a very high-speed, yet highly stable monolithic PLL with GaAs MESFET for high-speed clock and data recovery applications.

VCRO with Analog Mixer

Our VCRO is based on previously reported VCRO with analog mixer [3] whose schematic is shown in Figure 1. The frequency tuning in this VCRO is achieved with the analog mixer which mixes signals oscillating in the fast loop (two inverters) and slow loop (four inverters). The output of analog mixer, Vz is given as C*Vy + (1-C)*Vx [3], where Vx and Vy are two inputs to the mixer and C is the mixing ratio ranging from 0 to 1 determined by the control voltage. The highest oscillation frequency is obtained when C = 1, or signals propagate only in the fast loop, and the lowest when C = 0, or signals propagate only in the slow loop. Intermediate frequencies are obtained for 0 < C < 1 when signals in the fast loop and the slow loop are mixed by the mixer. If we assume for

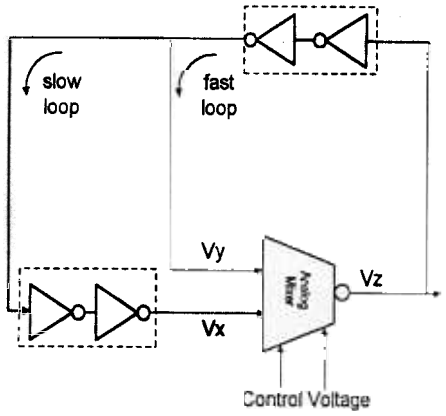

Figure 1. Schematic diagram of conventional VCRO

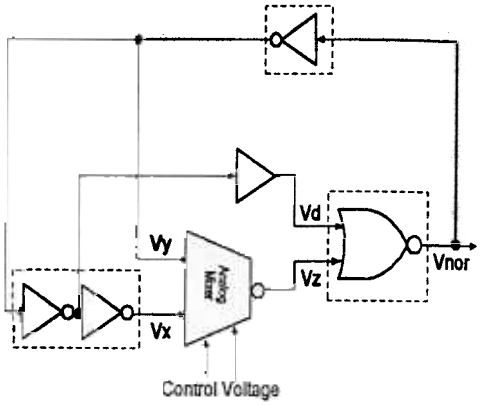

Figure 2. Schematic diagram of new VCRO

simplicity that all the gates including the analog mixer have delay time of D, then the largest oscillation period is 10D and the smallest 6D. The ideal timing diagrams for these two cases as well as for C = 0.5 with the delay time of 8D are shown in Figure 3(a). Note that the widths of both HIGH and LOW pulses change with the control voltage from 6D to 10D.

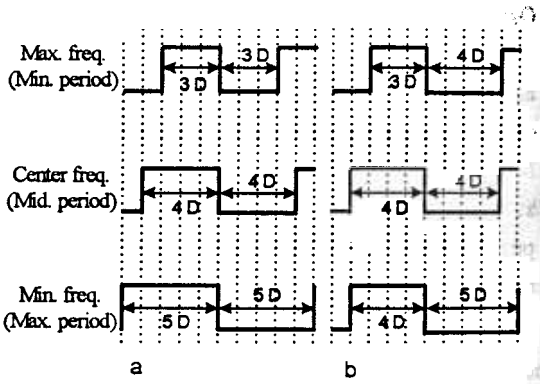

Figure 3. Timing diagram for
(a) conventional VCRO
(b) new VCRO

New VCRO architecture

Our new VCRO is based on a simple idea that VCRO tuning range, thus VCRO gain, can be reduced if the width of either logic HIGH or LOW, but not both, is controled by the control voltage as illustrated in Figure 3(b). The resulting oscillation period is then maximum 9D and the minimum 7D, and this reduction in range of oscillation period is directly translated to the VCRO gain reduction. Such waveforms as shown in Figure 3(b) can be implemented by addition of an NOR gate to the VCRO with analog mixer as shown in Figure 2 [4]. In order to understand the role of added NOR gate, consider the case when C = 1 which sets Vz = Vy. Assuming again that all the gates have the same delay time of D, transition from HIGH to LOW at Vnor (the output of NOR gate) reaches Vd (input to NOR gate) after 3D and Vz (the other input to NOR gate) after 2D. Vnor switches back to HIGH from LOW after 4D as both inputs to NOR gate have to be LOW in order to make its out HIGH. Likewise, transition from LOW to HIGH at Vnor reaches Vd after 3D and Vz after 2D, But, Vnor switches back to LOW from HIGH after 3D as only one input to NOR gate has to be HIGH to make its out LOW. As a result, the width of HIGH pulse is 3D and that of LOW pulse 4D making the oscillation period 7D. When C = 0 with Vz =

Vx, it can be easily argued that the width of HIGH pulse is 4D and that of LOW pulse 5D, making the oscillating period 9D. That is, transition from HIGH to LOW at Vnor reaches Vd after 3D and Vz after 4D. Vnor switches back to HIGH from LOW after 5D as both inputs to NOR gate have to be LOW in order to make its out HIGH. Likewise, transition from LOW to HIGH at Vnor reaches Vd after 3D and Vz after 4D, But, Vnor switches back to LOW from HIGH after 4D as only one input to NOR gate has to be HIGH to make its out LOW. For $0 < C < 1$, oscillating periods ranging from 9D to 7D can be obtained where only LOW pulse width is changed for $0 < C < 0.5$, and only HIGH pulse width is changed for $0.5 < C < 1$. In short, the addition of NOR gate reduces the tuning range of oscillation period from 4D of conventional VCRO to 2D of new VCRO and this factor of two reduction is directly translated to factor of two reduction in VCRO gain.

Simulation Results

In order to verify the above idea, we performed SPICE simulation with 1 μm MESFET technology. For the simulation, all the gates were implemented with GaAs Source-Coupled FET Logic which has a wider allowable threshold voltage range, a better fan-out capability, a smaller input capacitance as well as a versatility for the application than the other MESFET logics [5]. Both VCRO configurations shown in Figure 1 and 2 were simulated for comparison where the number of oscillation stage was selected so that the center oscillation frequency of about 3 GHz can be achieved. The resulting oscillating waveforms for the cases of $C = 0$, 0.5 and 1 are shown in Figure 4 with solid, dashed and bold dashed lines, respectively.

These waveforms are drawn from an inverting output buffer and, consequently, the polarity is

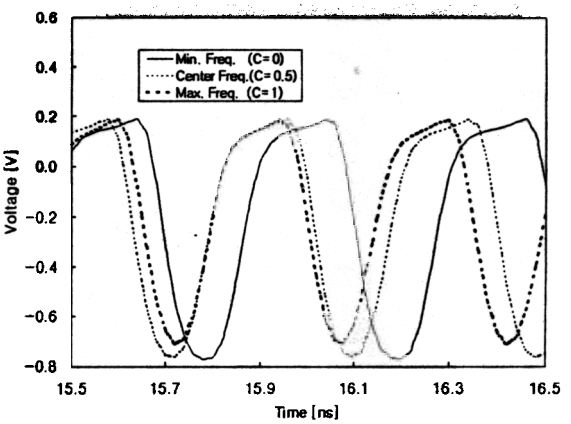

Figure 4. SPICE simulation results for oscillating waveforms

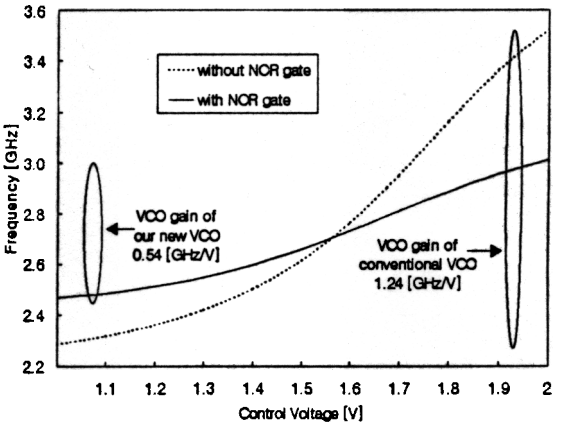

Figure 5. SPICE simulation result for tuning characteristics of conventional and new VCROs.

reversed from the ideal timing diagram shown in Figure 3. Figure 4 clearly shows that asymmetric control of HIGH and LOW pulse widths is achieved. The difference in pulse shape between pulse HIGH and pulse LOW is due to various capacitive components in the MESFET circuit as well as different gate delay times. Figure 5 shows the simulated dependence of oscillation frequency on control voltage for the conventional and our new VCROs. For the simulation, the control voltage was changed in steps of 0.05V. As can be seen from the figure, the

conventional VCRO has gain of 1.24 GHz/V for the range of 2.31 to 3.55 GHz. In comparison, our new VCRO has gain of 540 MHz/V for the range of 2.47 to 3.01 GHz.

Conclusion

A new VCRO architecture based on GaAs MESFET is proposed. It has an advantage that VCRO gain is reduced by factor of two while high oscillation frequency is maintained. Simulation results show that new VCRO has gain of 540 MHz/V, more than factor of two improvement over conventional VCRO with analog mixer. It is believed that this new VCRO can be very useful for realizing highly stable GHz-range PLL based on GaAs MESFET.

References

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