Low-Power PAM-4 Transmitter and Receiver

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Low-Power PAM-4 Transmitter and Receiver

by

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Abstract

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As the data rates in serial data communication rise up to 56 Gb/s, Pulse Amplitude Modulation (PAM-4) plays a critical role for achieving the required data rate. In addition, this modulation technique has been approved as a next generation standard, accordingly, many researches have tried to design and propose a high-speed and low-power PAM-4 transmitter/receiver.

In this dissertation, a newly proposed PAM-4 transmitter and receiver achieve high-speed operation with consuming low-power and occupying small chip area. The PAM-4 transmitter is based on the toggling seriailzer which produces data transition information from the

parallel data. With this structure, not only serializing data but also pre-emphasizing PAM-4 can be realized simply. In addition, a new type of SST driver enables to control pre-emphasis gain according to various channel response. A 40-Gb/s PAM-4 transmitter realized in 28-nm CMOS technology achieves 1.2 pJ/bit and 1.68 pJ/bit without/with pre-emphasis, and it occupies 0.0084 mm^2.

In the PAM-4 receiver focusing on clock and data recovery (CDR), a newly proposed phase detector filters specific transitions in order not to sacrifice the jitter performance of recovered data/clock. In addition, rotating edge sampling clocks periodically enables to decrease power consumption and chip area without the degradation of the performance. Our prototype chip is realized with 28-nm CMOS technology and its performance is successfully demonstrated. The 32-Gb/s PAM-4 CDR consumes 32 mW with 1.2-V supply and the clock signal recovered from PAM-4 input data has 0.0136-UI rms jitter.

Keywords: PAM-4 transmitter, PAM-4 receiver, Serializer, Source-series terminated driver (SST), Bang-bang phase detector, Clock and data recovery (CDR), high-speed serial link, multiphase

1. Introduction

1.1. Pulse Amplitude Modulation in Serial Interface

The recent traffic of data center is increasing dramatically as the spread of smartphones and tablet PC results in the growth of cloud computing services as shown in Fig. 1-1 [1]. Accordingly, Ethernet Standards is also continuously increasing to process large volume of data, and 100GbE (Gigabit Ethernet) equipment is being deployed in the Ethernet communications. In addition, 400GbE and 200GbE standards developed by the IEEE 802.3bs Task Force were approved as next generation [2].

However, servers in the data centers are always on and communicating each other because data never sleeps. As a result, energy consumption in the data centers can be a critical issue. As can be seen in the Fig. 1-2 [3], most of power is consumed to cool the server, which indicates that many electrical devices in the servers are power hungry. In order to decrease the cost of maintenance as well as provide good quality of service to consumers, the data centers should be designed as “high-speed” and “low-power”.

In order to transmit/receive higher data rate, Pulse Amplitude

Modulation (PAM) signaling is being highlighted as a solution to substitute common Non-Return-to-Zero (NRZ) signaling.

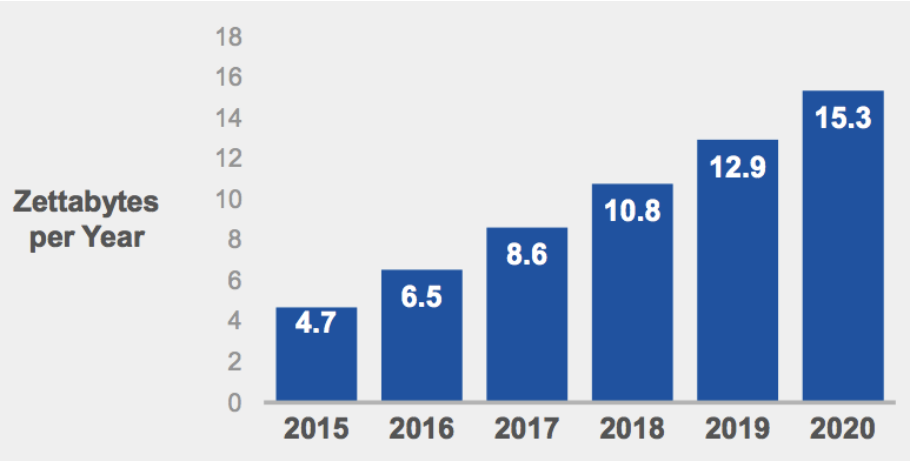


Fig. 1-1. Global data center traffic growth.

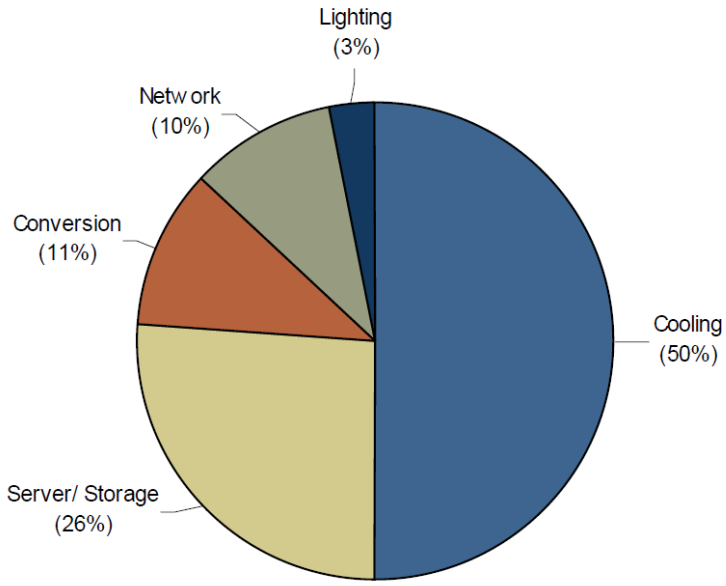


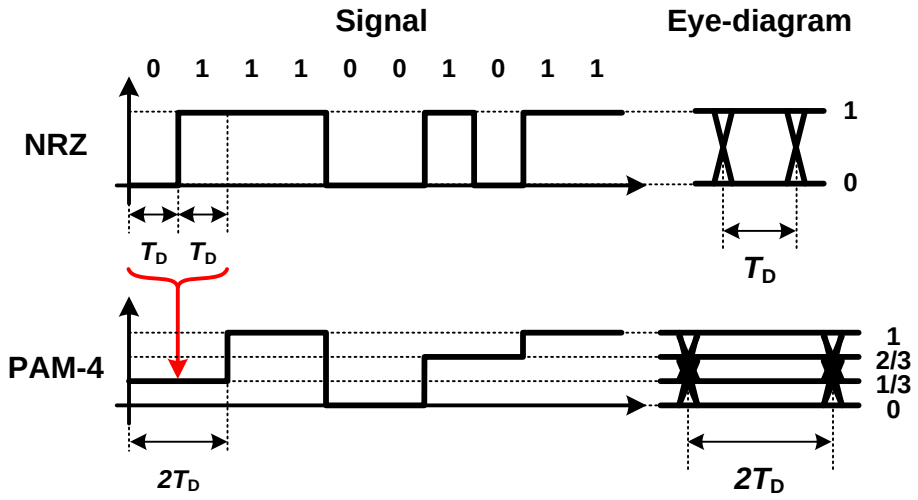
Fig. 1-2. Typical data center energy consumption.

1.2. PAM vs. NRZ

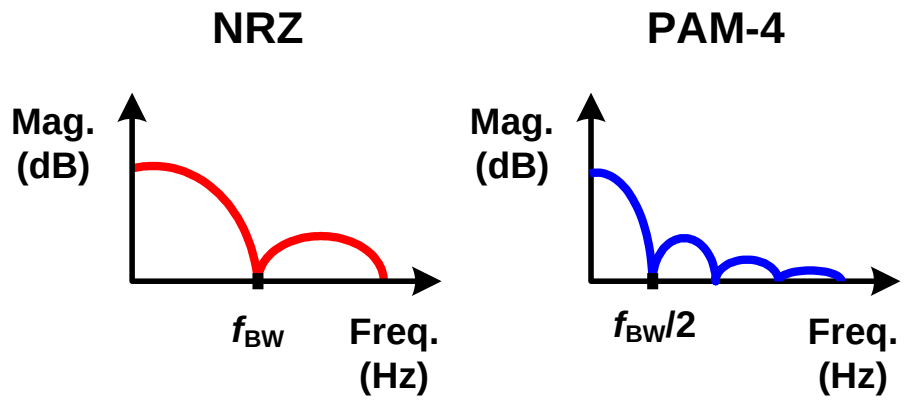
There are a great amount of research and development interests [4]–[8] for PAM-4 signaling as the need for higher-bandwidth serial interfaces is continuously increasing, and the conventional NRZ signaling is facing serious bandwidth and power consumption limitation. Furthermore, it is approved now as a next generation standard such as 400GbE and CEI-56G [2].

While NRZ (also known as PAM-2) is a modulation technique having two voltage levels as 1 and 0, PAM-4 modulates two bits of NRZ signal (00, 01, 10, and 11) into one voltage level among 4 possible voltage levels as one symbol. As an example, '01' two NRZ bits (MSB=0, LSB=1) can be expressed '1/3' in PAM-4 as shown in Fig. 1-3(a). PAM-4 has the advantage of having half of the Nyquist bandwidth and twice throughput compared NRZ signals, and it can be also observed in the frequency domain as shown in Fig. 1-3(b).

However, in PAM-4 signals, additional voltage levels degrade Signal-to-Noise Ratio (SNR) compared with NRZ signals. As shown in the Fig. 1-3(a), PAM-4 signal has one third amplitude compared with NRZ which causes the additional loss of SNR, and it can be expressed as,



(a)



(b)

Fig. 1-3. NRZ vs. PAM-4 in (a) time-domain, and (b) frequency-domain.

. $$SNR_{\text{loss}} = 20 \times \log_{10} \frac{1}{3} \cong -9.5\,\text{dB} \quad (1.1)$$

So that reason, the use of PAM-4 instead of NRZ can be justified in the channel having the loss difference more than -9.5 dB between the loss at NRZ Nyquist frequency, f_N, and PAM-4 Nyquist frequency, $f_N/2$, as shown in Fig. 1-4. Simply, when $|H(f_N)| - |H(\frac{f_N}{2})| = G_{\text{loss}} \leq -9.5\,\text{dB}$, PAM-4 signal can be a better solution compared with NRZ.

Theoretically, PAM-4 should have twice horizontal eye-opening, T_{PAM}, compared with NRZ signal, T_{NRZ}, but it is not doubled practically, and this can be observed in the time-domain. In PAM-4 signaling, three cases of rising transitions, y_1, y_2 and y_3, can be considered as shown in

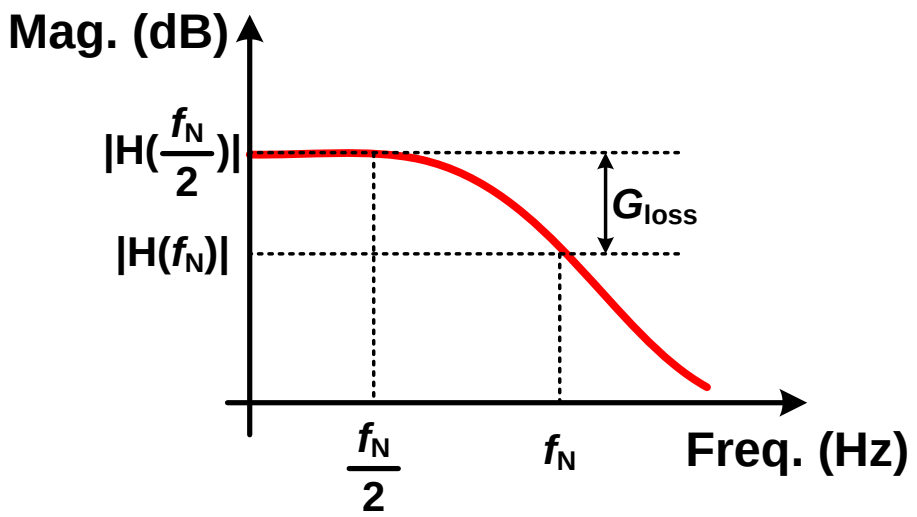


Fig. 1-4. Channel response for justifying the use of PAM-4.

Fig. 1-5 while one transition, y, can be considered in NRZ signaling. For a simple comparison, each rise/fall time, T_R, in PAM-4 and NRZ is set equally. In NRZ signal, the distance between the x-axis intercept of y and y' is 3, and it means that the horizontal eye-opening is $2 \cdot T_{NRZ}=3$. However, in the PAM-4 signal, the smallest horizontal eye-opening is $\frac{7}{3}$, since the x-axis intercept of y_2 and y2' are $(\frac{1}{3}, 0)$ and $(\frac{8}{3}, 0)$ respectively, and $T_{PAM}=\frac{7}{3}$. It means that the PAM-4 1-UI, T_{PAM}, achieves less than twice eye width of NRZ, $2 \cdot T_{NRZ}$. In addition, the combinations of unsymmetrical eye-diagrams in top and bottom and symmetrical eye-diagrams in middle as shown in Fig. 1-6 [9] also degrade the horizontal margin of eye-diagram. Since EW is smaller than $EW_{largest}$. So those reasons, PAM-4 is usually used in the channel having G_{loss} lower than -11-dB, and it can be found in the standard channel as shown in Fig. 1-7 [9].

The level separation mismatch ratio, R_{LM}, is an important specification [10] indicating the vertical linearity of the signal. V_0, V_1, V_2, and V_3 indicate each voltage level, and V_{mid} is the mid-level of the signal as shown in Fig. 1-8(a). V_{mid} is then normalized and offset adjusted so that V_{mid} corresponds to 0, V_0 to −1, V_1 to −ES1, V_2 to ES2, and V_3 to 1, and they can be expressed as,

$$V_{\text{mid}} = \frac{V_0 + V_3}{2} \tag{1.2}$$

$$\text{ES1} = \frac{V_1 - V_{\text{mid}}}{V_0 - V_{\text{mid}}} \tag{1.3}$$

$$\text{ES1} = \frac{V_2 - V_{\text{mid}}}{V_3 - V_{\text{mid}}} \tag{1.4}$$

And, finally, R_{LM} is defined as [10],

$$R_{\text{LM}} = \min\left((3 \cdot ES_1), (3 \cdot ES_2), (2 - 3 \cdot ES_1), (2 - 3 \cdot ES_2)\right) \tag{1.5}$$

If the signal is ideal, R_{LM} would be '1', because the distance of V_1 to V_{mid} and V_2 to V_{mid} are one third of the distance of V_0 to V_{mid} and V_3 to V_{mid} respectively, $ES_1 = \frac{1}{3}$ and $ES_2 = \frac{1}{3}$. However, if the vertical non-linearity of eye-diagram is occurred, R_{LM} would not be '1' as shown in Fig. 1-8(b) as an example, $R_{\text{LM}} = 0$. Generally, PAM-4 eye distortion is measured with the R_{LM}, and standards recommend $R_{\text{LM}} > 0.92$.

PAM-4 signaling can be a better solution in the aspects of overcoming bandwidth limitation. However, it should be handled carefully in order not to sacrifice the SNR and the linearity of the signal.

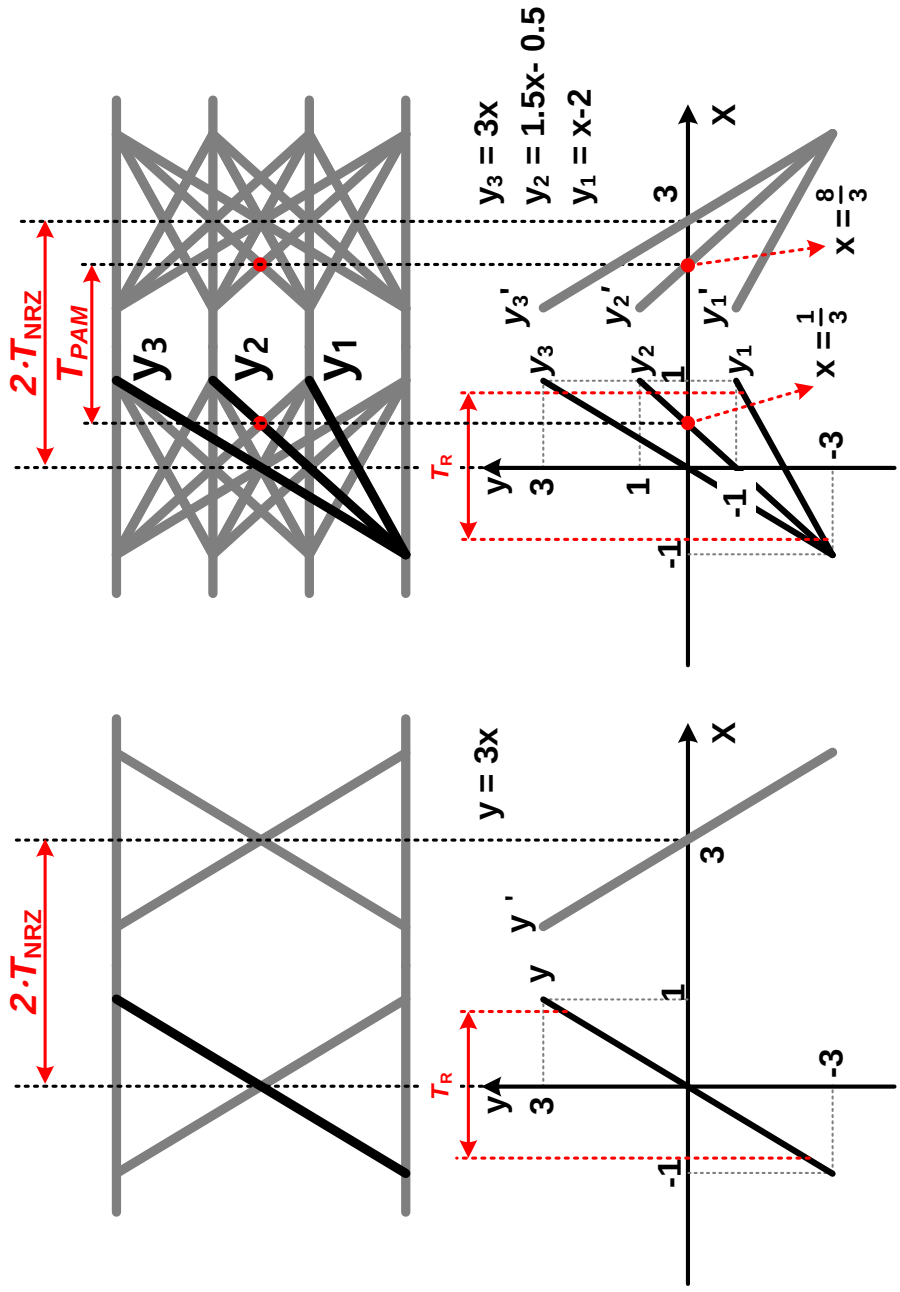


Fig. 1-5. The horizontal eye-diagram comparison between NRZ and PAM-4.

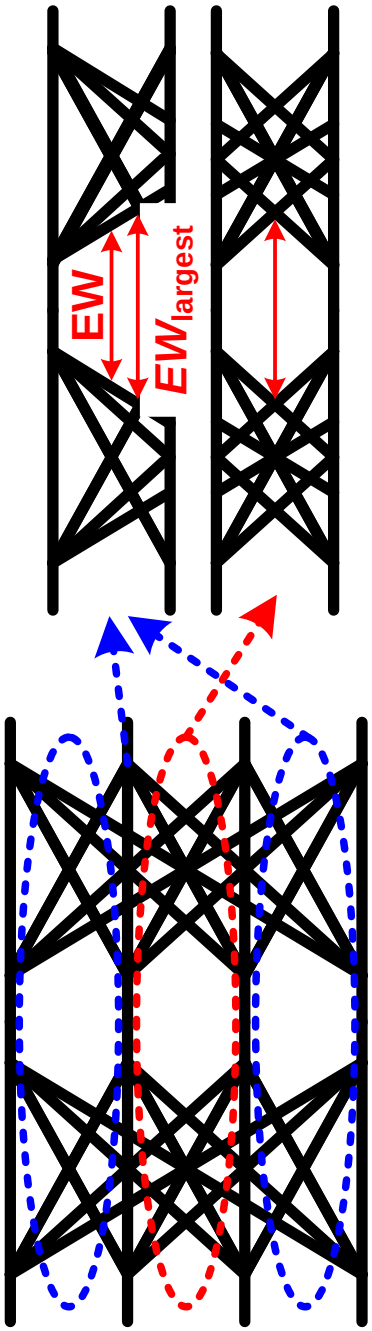


Fig. 1-6. Unsymmetrical eye-diagram in top and bottom side, and symmetrical eye-diagram in mid side.

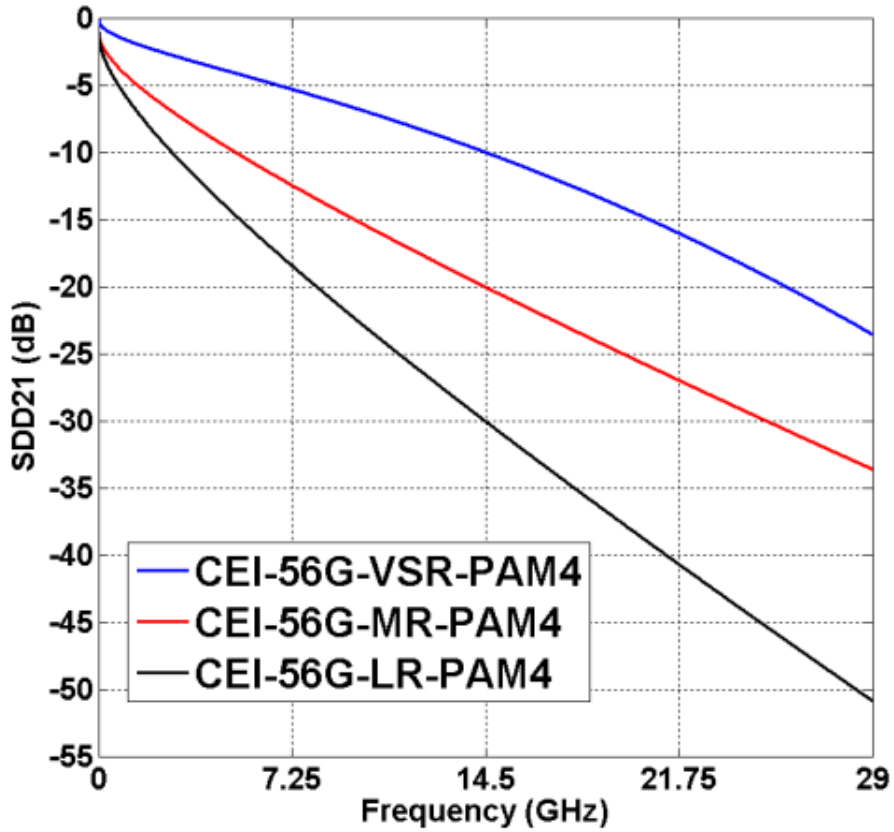
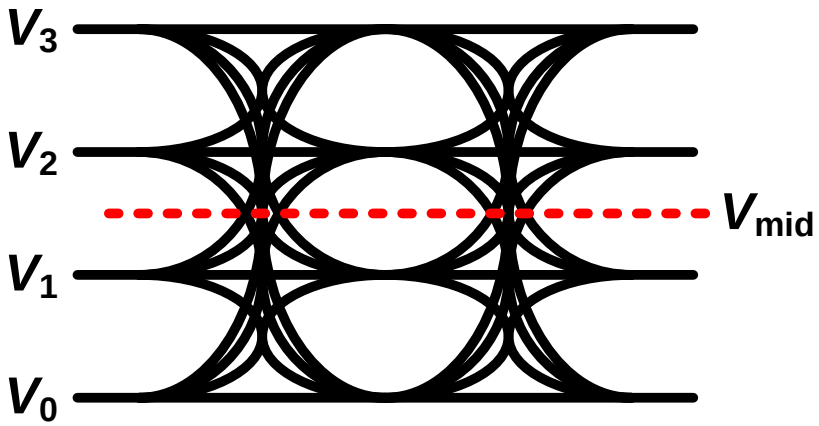
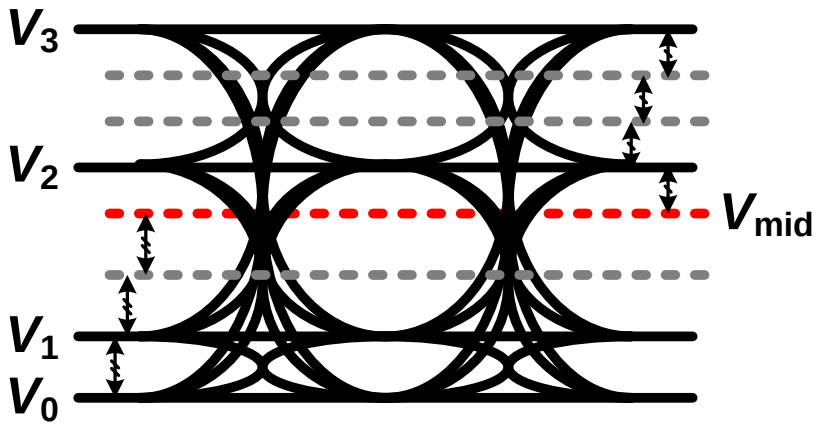


Fig. 1-7. CEI-65G-VSR (Very Short Reach) /MR (Medium Reach) /LR (Long Reach) -PAM4 baseline specifications.



(a)



(b)

Fig. 1-8. (a) Ideal eye-diagram, and (b) distorted eye-diagram.

1.3. Overview of PAM-4 transmitter and receiver

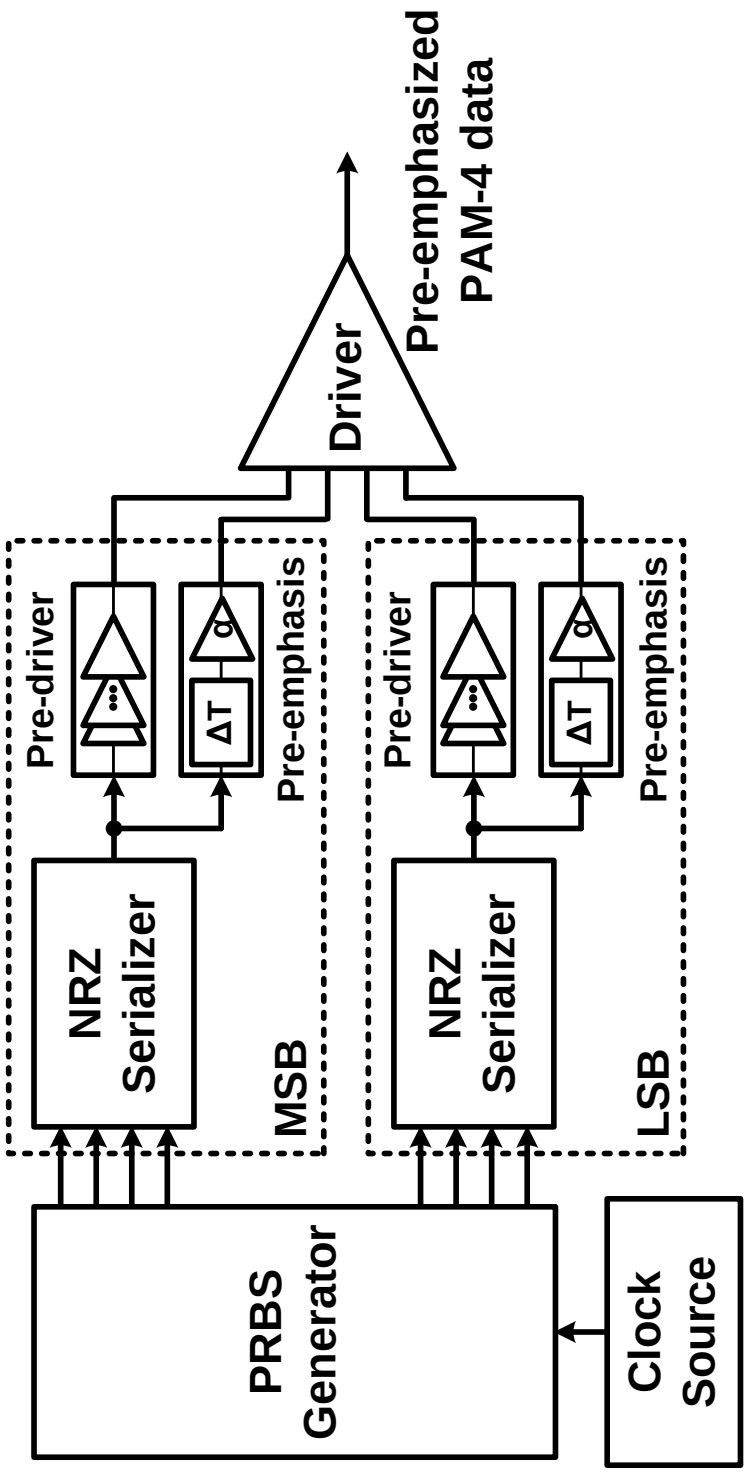
Generally, PAM-4 transmitter and receiver is very similar with the structures of NRZ, but the additional blocks are necessary for handling multi-level signals.

In the case of the transmitter, 2 NRZ serializers generate LSB and MSB respectively as shown in Fig. 1-9(a), and each signal is combined at the driver. In order to satisfy the specifications of standards as shown in Table 1-1, additional DFFs are necessary for delaying MSB, LSB respectively to pre-emphasize PAM-4 signal, which increases power consumption and chip area. The driver combines the signal, MSB, LSB and pre-emphasis while it maintains a higher R_{LM} than 0.92 to satisfy the specifications of the standard, so the driver should be designed carefully in order not to sacrifice the linearity.

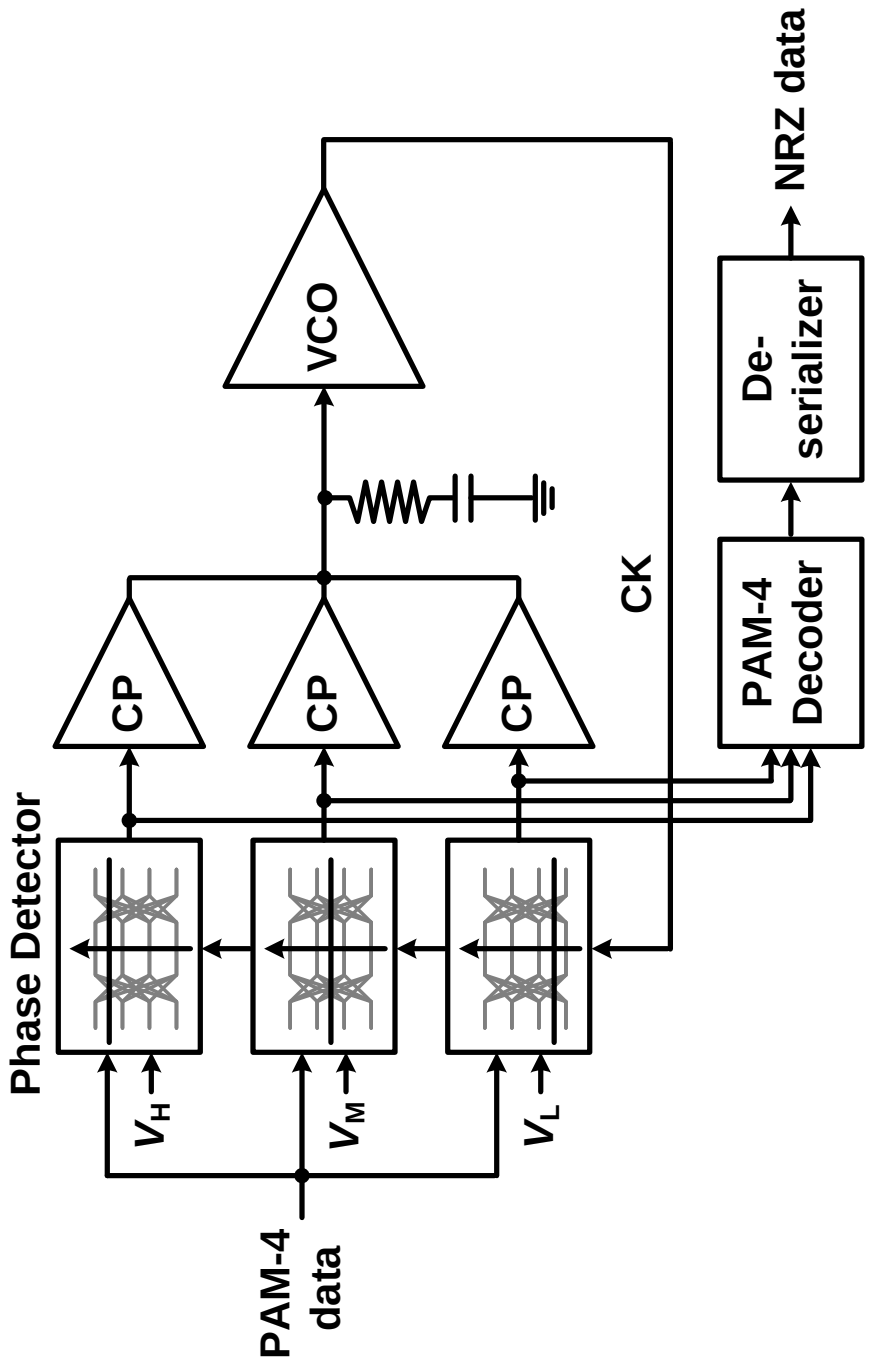
Similarly, in PAM-4 receiver as shown in Fig. 1-9(b), each block should handle not 2-levels but 4-levels, so the three times number of the blocks and a PAM-4 decoder are necessary compared with NRZ receiver. Three phase detectors (PD) having different reference voltage, V_H, V_M, and V_L, detects the edge of the data similar with the PD for NRZ signal. However, as shown in the Fig. 1-5 and 1-6, multi-level transitions result in the degradation of CDR performance, since it can

be shown as the increase of input jitters to CDR. So that reason, CDR in PAM-4 receiver should be designed insensitive to the quality of input within the range of the specifications provided by the standard. If not, the characteristics of CDR will vary greatly according to the quality of multi-level transitions.

As mentioned before, the PAM-4 signaling can be a good solution which needs half of the bandwidth compared with NRZ signal. However, it sacrifices not only horizontal but also vertical eye-margin, so careful design is necessary in realizing PAM-4 transmitter and receiver.


Pre-emphasized
PAM-4 data
Driver
Pre-driver
Pre-emphasis
ΔT
NRZ
Serializer
MSB
LSB
PRBS
Generator
Clock
Source

(a)



(b)

Fig. 1-9. (a) PAM-4 transmitter, and (b) PAM-4 receiver.

TABLE 1-1
SUMMARY OF CEI-56G DIFFERENT REACHES AND DISTANCES.

Parameter	**VSR**	**MR**	**LR**
Reach	Chip-to-module	Chip-to-chip	Chip-to-chip over backplane
Data Rate (Gb/s)	39.2 - 58	36 - 58	36 - 58
Insertion Loss	10 dB @ 14GHz	20 dB @ 14GHz	30 dB @ 14GHz

1.4. Outline of Disseration

This dissertation focuses on designing high-speed and low-power PAM-4 transmitter and receiver. PAM-4 transmitter based on the toggling serializer is proposed, and it enables to produce pre-emphasized signal easily as well as decrease power consumption and chip area. In addition, a newly proposed Series-Source Terminated (SST) driver for pre-emphasized PAM-4 signal can control pre-emphasis gain efficiently without sacrificing the R_{LM}. In PAM-4 receiver, a selective transition phase detector (STD) made by simple logics enables PAM-4 CDR tolerable to input slew-rate which might degrade horizontal loss in PAM-4 eye-diagram. In addition, the rotating edge-sampling clock schemes decrease the power consumption and chip area.

The dissertation consists of five chapters. Chapter 2 shows the basic concept of PAM-4 transmitter based on the toggling serializer. The operation of toggling serializer and the process of producing pre-emphasized PAM-4 are explained. The operation of a newly proposed SST driver is also described. Detail circuit implementation of the PAM-4 transmitter including the driver is also described. Chapter 3 shows PAM-4 receiver focusing on CDR which is designed with STD to be

tolerable to input slew-rate and rotational scheme for edge-sampling clocks. Detail circuits including PAM-4 decoder for deserializing PAM-4 signal are also described. Chapter 4 gives implementation, experimental setup and results of 40-Gb/s PAM-4 transmitter and 32-Gb/s PAM-receiver respectively. Finally, chapter 5 summarizes this dissertation with conclusions and discussions.

2. PAM-4 Transmitter

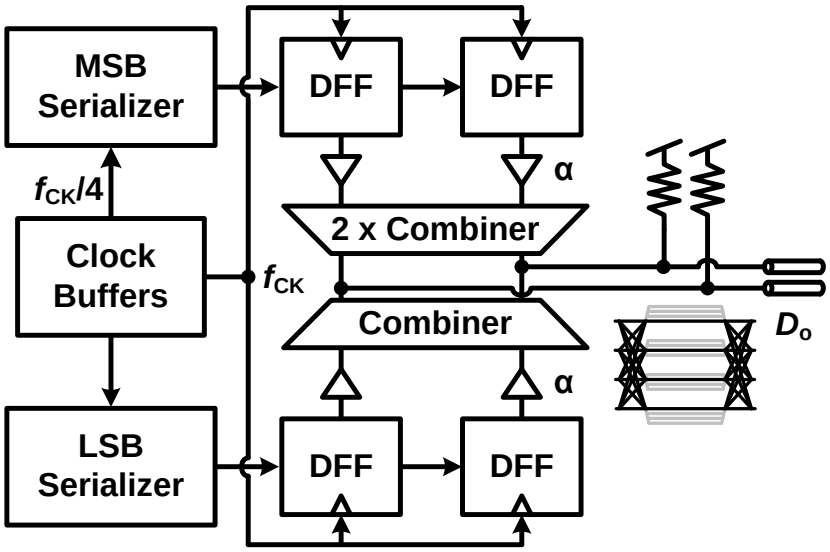
The designing multi-levels causes the complexity of serializer especially in the transmitter having pre-emphasis technique.

Fig. 2-1 shows the conventional PAM-4 transmitter having a pre-emphasis function [11], [12]. It is intuitive technique to make serialized and pre-emphasized signals, however, it requires bunch of clock buffers to drive a high-speed clock and a power hungry DFF which might need additional inductors for avoiding bandwidth limitation. In [11], CML type combiners can control pre-emphasis gain easily, but consumes large amount of power.

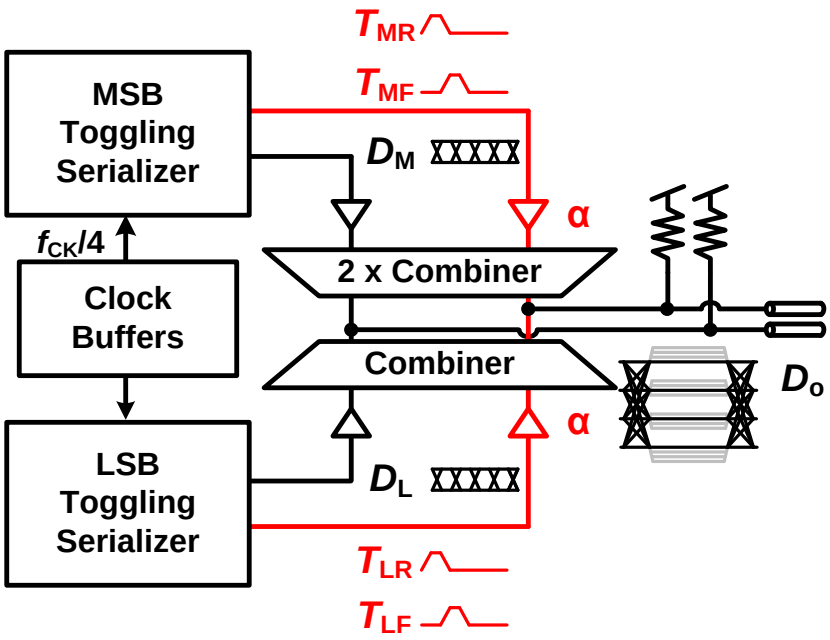
[12] uses a SST driver so that it achieves reduction of power consumption, however, it results in bunch sets of resistors in order to control the gain. Unfortunately, the bunch sets except the set of resistors in use result in additional bandwidth limitation caused by parasitic capacitors and resistors. [6] proposes a new type of PAM-4 transmitter producing pre-emphasized PAM-4 signal from transition information. However, it needs additional encoders to generate transition information from the PRBS generators.

Our transmitter based on the toggling serializer [13] can produce pre-emphasized PAM-4 signal easily without high-speed clock buffers,

DFFs, and additional encoders as shown in Fig. 2-1. In addition, the newly proposed SST driver can produce pre-emphasized PAM-4 signal easily without bunch sets of resistors.



(a)



(b)

Fig. 2-1. (a) Conventional PAM-4 transmitter, and (b) proposed PAM-4 transmitter.

2.1. PAM-4 Transmitter Based on Toggling Serializer

From Fig. 2-2 [13], the operation of toggling serializer [13] can be described simply. In order to extract transition information from the parallel data, A, B, C, and D, should be aligned to each clock phase and converted into RZ data form, A', B', C', and D'. With simple logical operations as shown in Eq. 2-1 and 2-2, the transition information, T_R (rising transition) and T_F (falling transition), can be extracted, and the serialized data, D_P and D_N, can be produced.

$$T_R = \overline{\left(\overline{A'}\cdot B'\right)\cdot\left(\overline{B'}\cdot C'\right)\cdot\left(\overline{C'}\cdot D'\right)\cdot\left(\overline{D'}\cdot A'\right)} \quad (2.1)$$

$$T_F = \overline{\left(\overline{A'\cdot\overline{B'}}\right)\cdot\left(\overline{B'\cdot\overline{C'}}\right)\cdot\left(\overline{C'\cdot\overline{D'}}\right)\cdot\left(\overline{D'\cdot\overline{A'}}\right)} \quad (2.2)$$

Fig. 2-3 shows how to make PAM-4 signals from the toggling serializer. Simply, two NRZ serializers are used to produce serialized and transition signals. The MSB and LSB toggling serializers generate D_M (MSB), D_L (LSB), T_{MR} (MSB rising transition signal), T_{LR} (LSB rising transition signal), T_{MF} (MSB falling transition signal), and T_{LF} (LSB falling transition signal).

As an example, D_M, D_L are logical zero at the first interval in Fig.

2-3, and D_M, D_L become high simultaneously at the second interval. In this case, T_{MR} and T_{LR} becomes high, and other transition signals are logical zero. From the second interval to the third interval, only D_L becomes low, so T_{LF} becomes high while other toggling signals are logical zero. In fact, serialized data, D_M and D_L, are produced from transition signals, however, for simple explanations, the operations were described reversely.

The pre-emphasized PAM-4 signals can be inferred from each of toggling signals intuitively, and it can be expressed as,

$$D_O = 2 \cdot D_M + 2\alpha \cdot (T_{MR} - T_{MF}) + D_L + \alpha \cdot (T_{LR} - T_{LF}) \qquad (2.3)$$

α means the relative amplitude of pre-emphasis when the amplitude of LSB is 1 as shown in Fig. 2-3. Since the amplitude of MSB is twice larger than the amplitude of LSB, the amplitude of pre-emphasis in MSB is also twice larger than that of LSB in order to pre-emphasize MSB and LSB signal equally as shown in Eq. (2.3).

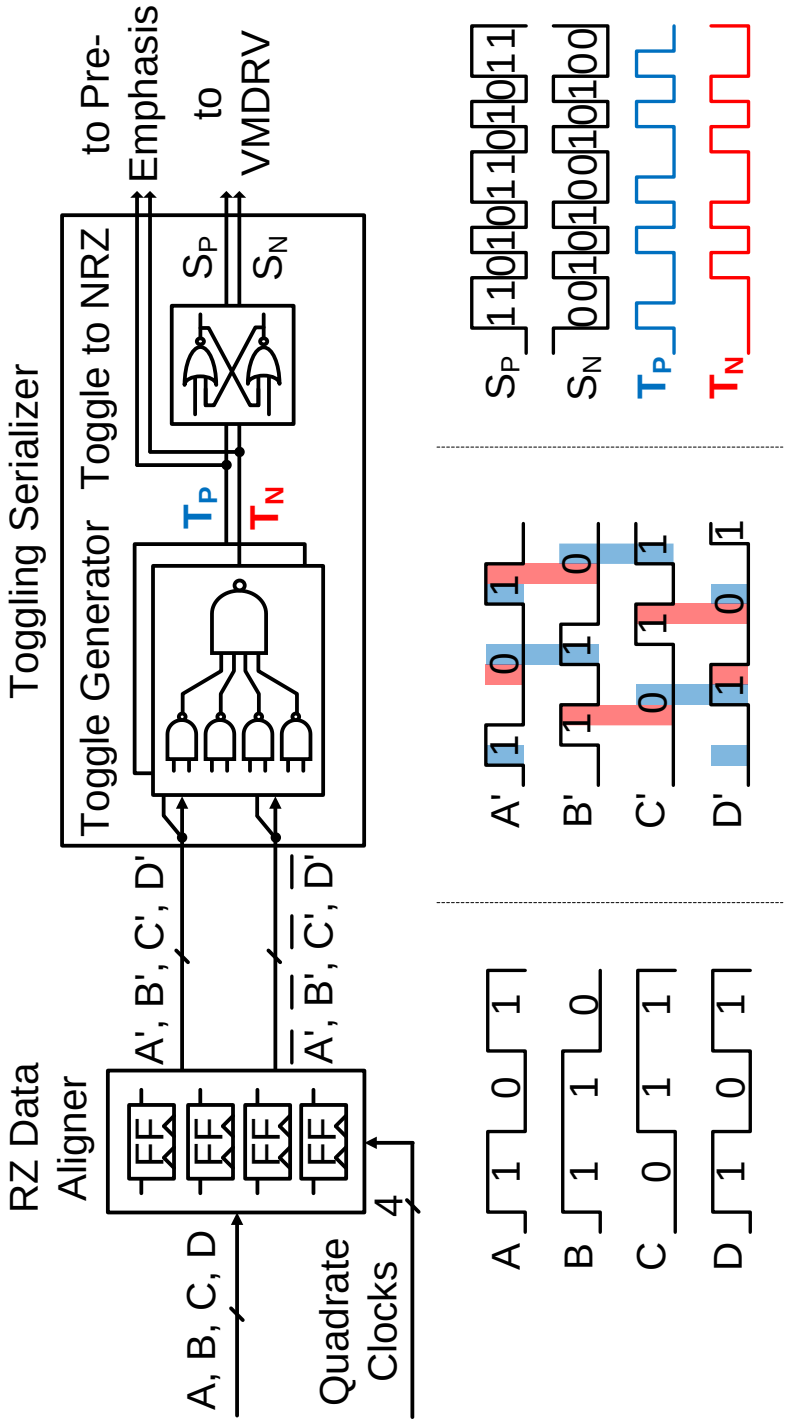


Fig. 2-2. Toggling serializer.

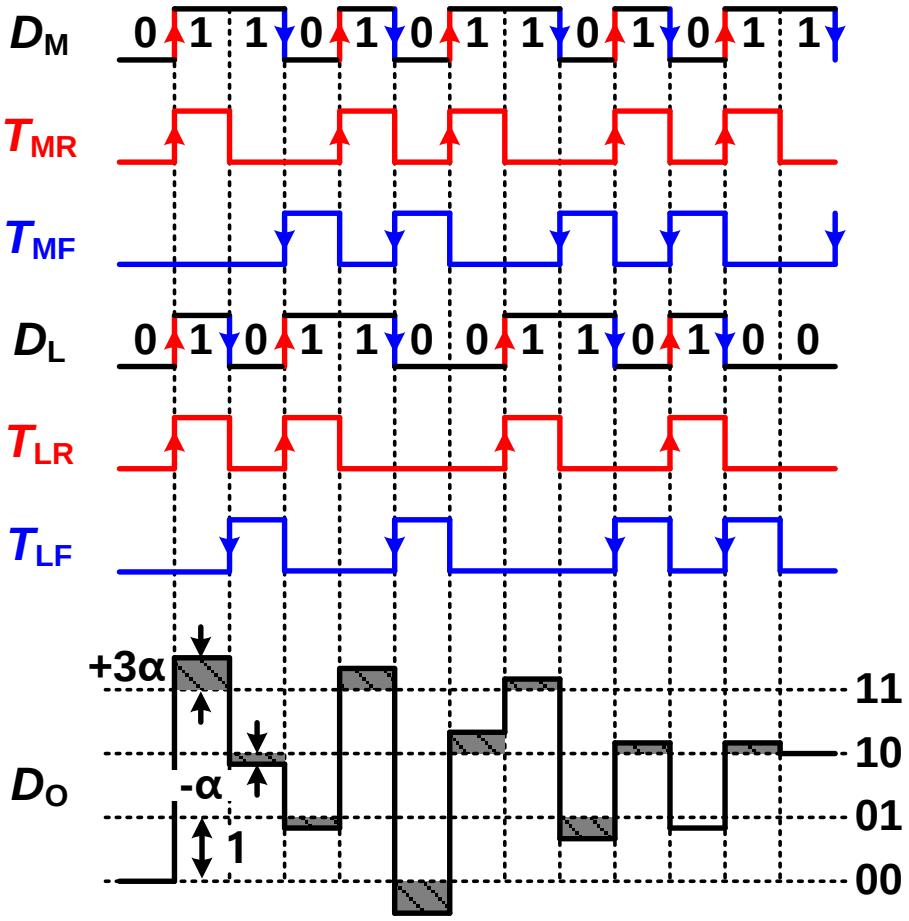


Fig. 2-3. The timing diagram of producing PAM-4 and transition signals.

2.2. Series-Source Terminated Driver for PAM-4

SST driver is an attractive solution as it enables to terminate in large range of voltages and operate with low-power consumption [14] as shown in Fig. 2-4(a). However, 4 stacks of transistors and resistors disturbs high-speed operations cause of additional parasitics between stacks and voltage headroom problems [15].

In order to solve the band-limited issue in the driver, a new type of SST driver has been proposed [15], which needs only two stacks of transistors with series resistor as shown in Fig. 2-4(b). It can be applied to pre-emphasized PAM-4 signal easily as shown in Fig. 2-5(a). D_{M} means MSB signals, and D_{M1UI} is 1UI-delayed MSB signal. It is possible to make the pre-emphasized MSB signal, D_{M}-D_{M1UI}, and the other case, LSB, pre-emphasized LSB signal can be also produced by D_{L}-D_{L1UI}. In order to subtract signals, inverse of D_{M1UI} and D_{L1UI} are used as $\overline{D_{\mathrm{M1UI}}}$ and $\overline{D_{\mathrm{L1UI}}}$. Finally, these two signals are summed up at the last stage of drivers as shown in Fig. 2-5(a). In order to maintain the output impedance including not only series resistors but also turn-on resistance of input transistors in the drivers as 50 Ω by clipping the swing of signals from V_1 to V_2. By using 2 stacks of transistors, it can increase the operation bandwidth dramatically [15], however, it still

needs bunch sets of resistors in order to control the pre-emphasis gain, since the amplitude of signals is decided by the ratio of resistors.

The newly proposed SST driver based on [15] doesn't need any bunch sets of resistors to control the gain. For satisfying the Eq. 2-3, in the case of falling transitions, the inverse signals are used, $\overline{T_{\mathrm{MF}}}$ and $\overline{T_{\mathrm{LF}}}$, and V_{CM} indicates the half of the V_{DD}. Instead of controlling the pre-emphasis gain by selecting one set among bunch sets of resistors, our driver can control the pre-emphasis gain by varying V_{DC} according to the channel response.

In order not to sacrifice the reflection characteristics, with or without pre-emphasis, the output impedance, Z_0, should be maintained as 50 Ω, and it can be expressed as,

$$Z_0 = \frac{\mathrm{R}}{2} \| \frac{\mathrm{R}}{2\alpha} \| \frac{\mathrm{R}}{2\alpha} \| R \| \frac{\mathrm{R}}{\alpha} \| \frac{\mathrm{R}}{\alpha} = 50\,\Omega \tag{2.3}$$

From Eq. (2.3), R can be described as,

$$\mathrm{R} = 150\left(1+2\alpha\right) \tag{2.4}$$

With this resistance, each voltage level according to the transmitted signal can be analyzed. The SST driver can be simplified as an equivalent circuit shown in Fig. 2-6. In our design, the driver turns off the function of pre-emphasis by blocking the transmission of transition signals (T_{MR}, T_{MF}, T_{LR}, and T_{LF}) instead of selecting the adequate resistor set among bunch of sets, so the resistors for transition signals are always remained regardless of using the pre-emphasis function or not.

Firstly, the amplitude of PAM-4 signal without pre-emphasis can be calculated. When $D_M D_L$ = 11, the equivalent circuit can be described as shown in Fig. 2-7. $T_{MR,}$ T_{LR}, T_{MF} and T_{LF} are logical zero for turning off the pre-emphasis, and the output voltage level is calculated as,

. $$V_O = \frac{3 \cdot V_{DD} + 6 \cdot \alpha \cdot V_{CM}}{6 + 12 \cdot \alpha}, \text{when } D_M D_L = 11 \quad (2.5)$$

Other cases of $D_M D_L$ = 10, $D_M D_L$ = 01, and $D_M D_L$ = 00 can be also calculated as shown in Table 2-1. The amplitude of PAM-4 can be derived from Table 2-1, and the smallest amplitude, V_{LSB}, can be expressed as,

. $$V_{LSB} = \frac{V_{DD}}{6 + 12 \cdot \alpha} \quad (2.6)$$

If α = 1 and 1.2-V supply voltage, the amplitude of LSB is 66.7 mV.

Similarly, the pre-emphasis gain can be calculated according to V_{DC}. When $D_M D_L$ = 11 ➔ $D_M D_L$ = 10, D_M and T_{LF} would be logical one, and others would be logical zero. When $D_M D_L$ = 10 ➔ $D_M D_L$ = 11, the D_M, D_L, and T_{LR} would be logical one, and others would be logical zero as shown in Fig. 2-8. From two cases, '11' ➔ '10' and '10' ➔ '11', each output voltage level can be derived respectively as,

. $$V_O = \frac{3 \cdot V_{DD} + 3 \cdot \alpha \cdot V_{DD} + 2\alpha \cdot V_{DC}}{6 + 12 \cdot \alpha}, \text{when } D_M D_L = 11 \rightarrow 10 \quad (2.7)$$

. $$V_O = \frac{2 \cdot V_{DD} + 3 \cdot \alpha \cdot V_{DD} - 2\alpha \cdot V_{DC}}{6 + 12 \cdot \alpha}, \text{when } D_M D_L = 10 \rightarrow 11 \quad (2.8)$$

Then, the amplitude of LSB including pre-emphasis can be derived by subtracting Eq. (2.7) from Eq. (2.8), and it can be expressed as,

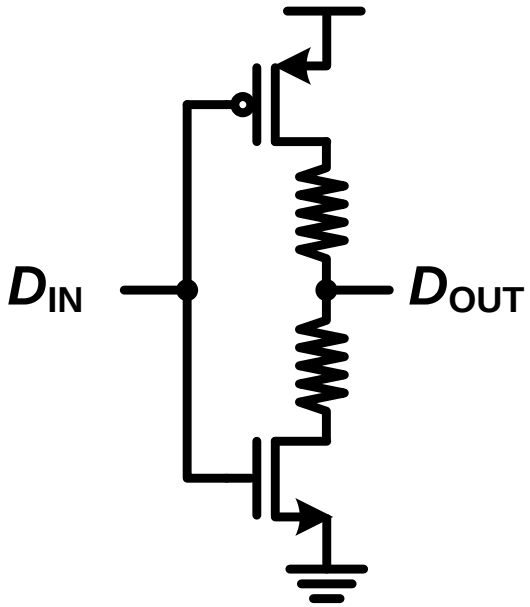
. $$V_{\text{pre-LSB}} = \frac{V_{DD} + 4 \cdot \alpha \cdot V_{DC}}{6 + 12 \cdot \alpha} \quad (2.10)$$

From Eq. (2.6) and (2.10), the pre-emphasis gain according to V_{DC} can

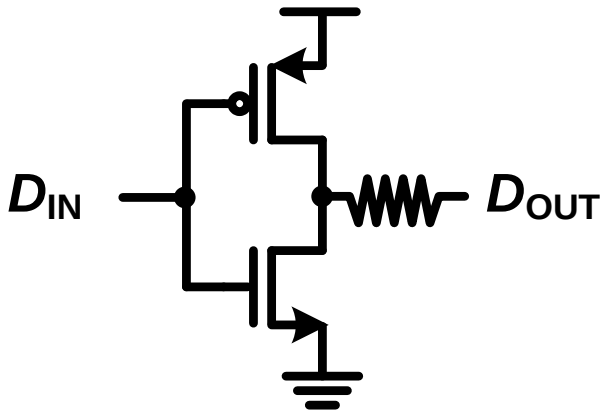
be derived like the pre-emphasis gain of NRZ as,

. $$G_{\mathrm{PRE}} = 20 \cdot \log \frac{V_{\text{pre-LSB}}}{V_{\mathrm{LSB}}} = 20 \cdot \log \frac{V_{\mathrm{DD}} + 4 \cdot \alpha \cdot V_{\mathrm{DC}}}{V_{\mathrm{DD}}} \qquad (2.11)$$

As an example, if α = 1 and V_{DC} = 0.6 V, G_{pre} is 9.54 dB.

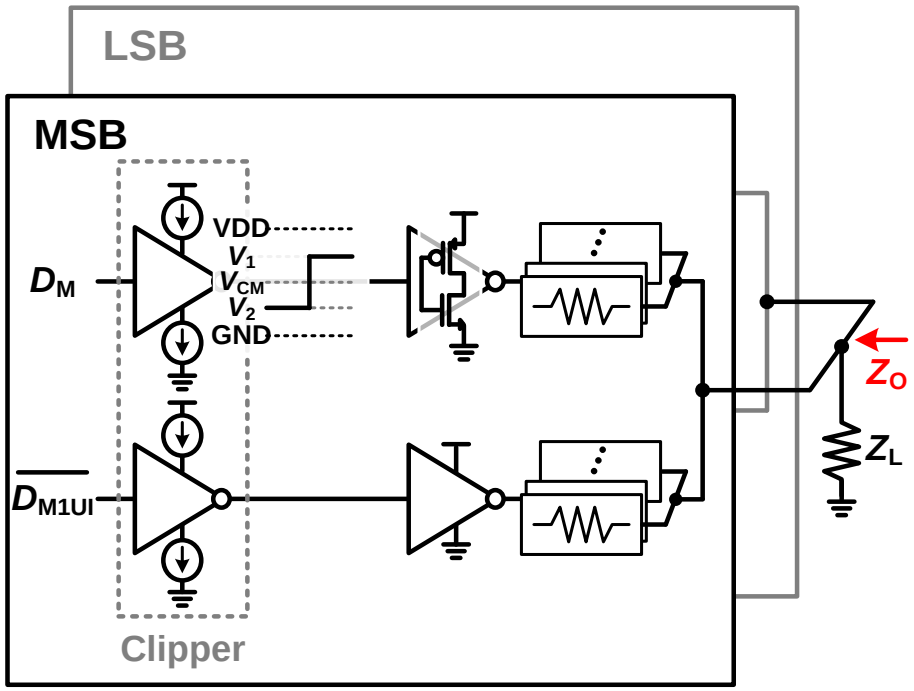


(a)

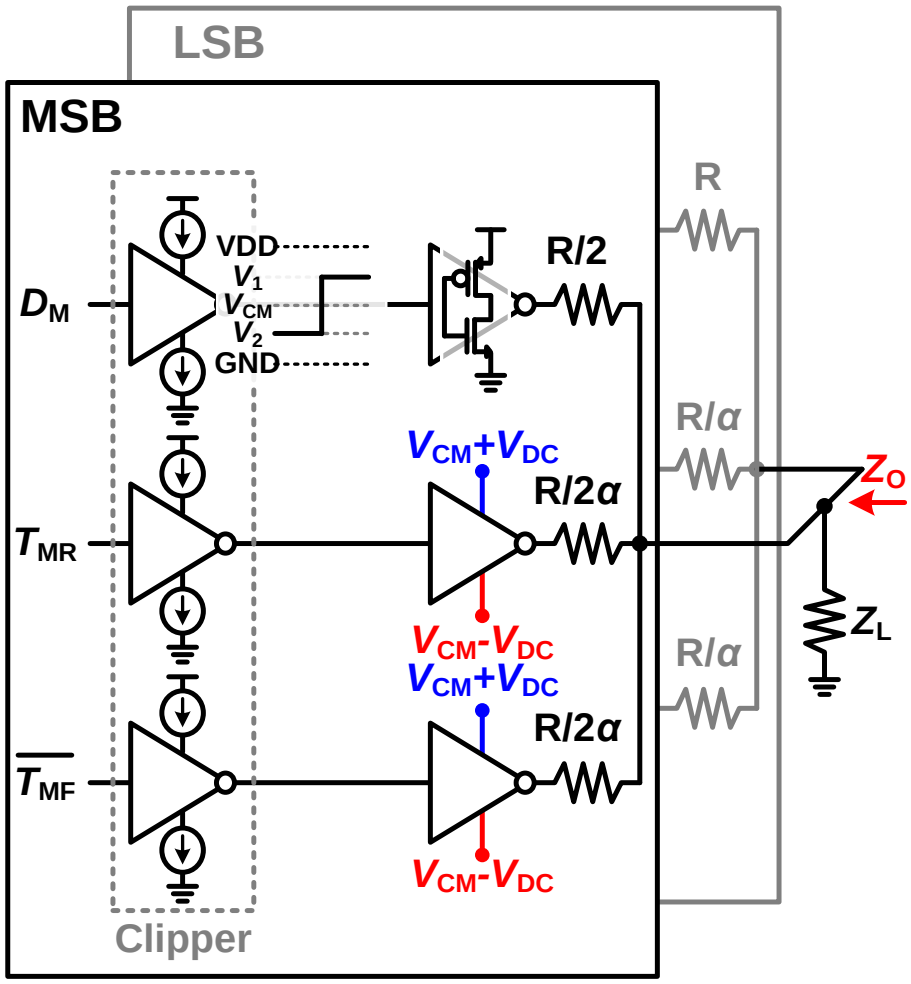


(b)

Fig. 2-4. (a) Conventional SST driver, and (b) SST driver in [15].



(a)



(b)

Fig. 2-5. (a) Conventional PAM-4 SST driver, and (b) proposed PAM-4 SST driver.

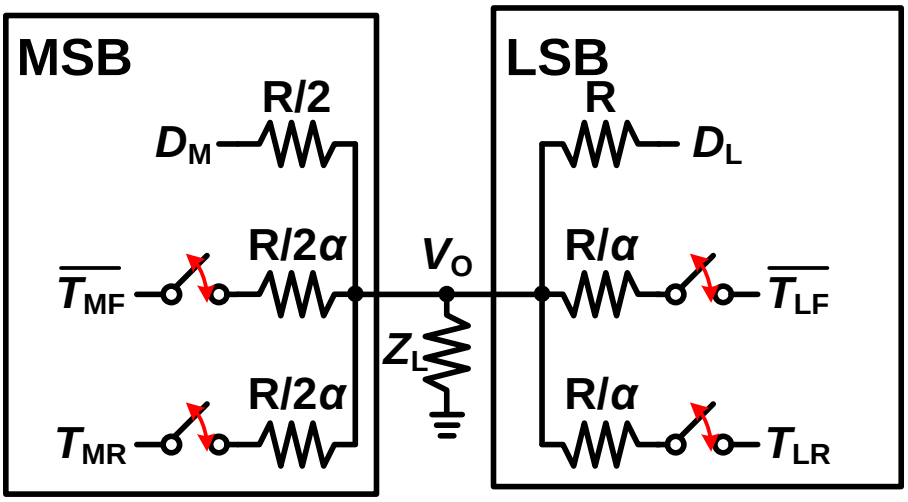


Fig. 2-6. Equivalent circuit of PAM-4 SST driver.

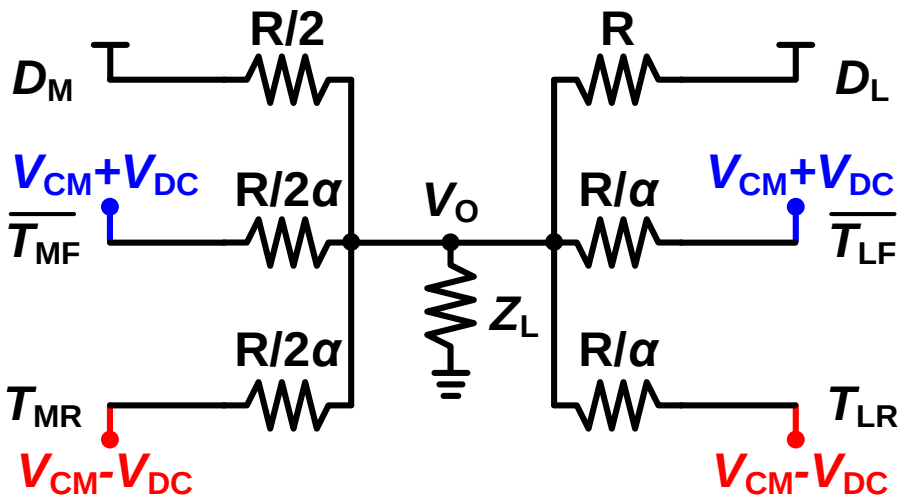
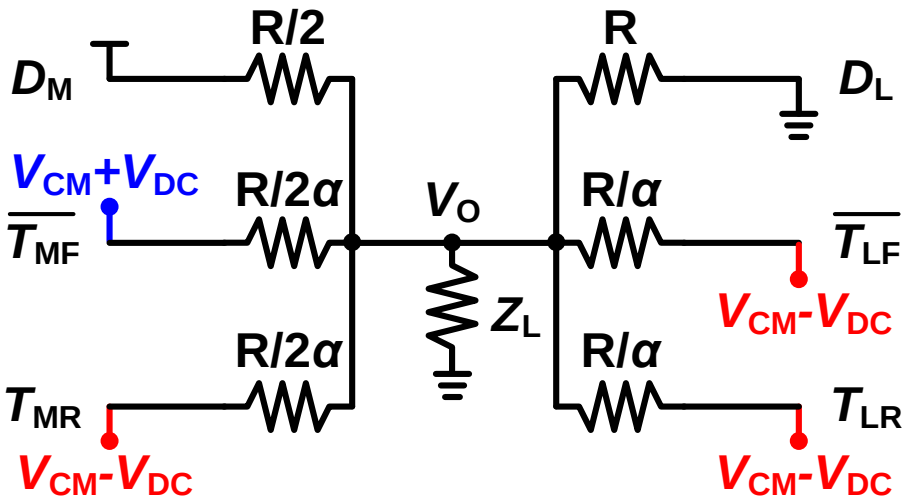


Fig. 2-7. Equivalent circuit of $D_M D_L$ = 11 with no pre-emphasis.

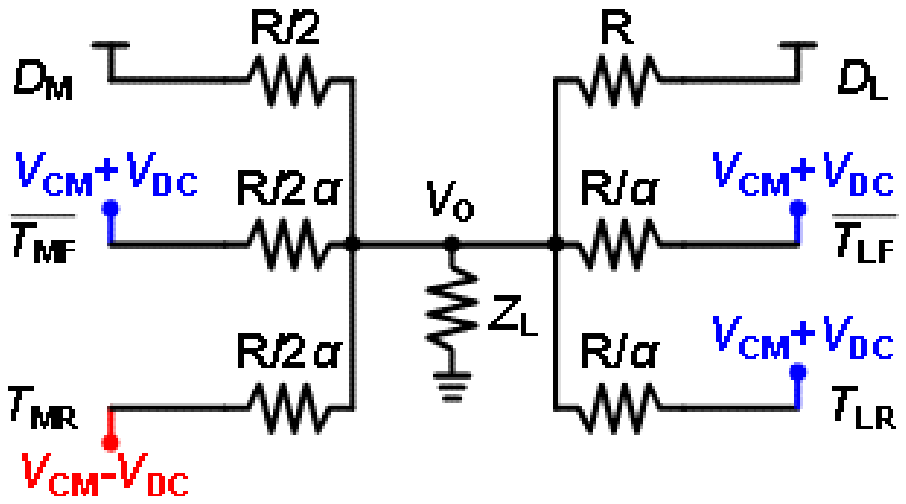
TABLE 2-1

EACH VOLTAGE LEVEL ACCORDING TO $D_M D_L$.

$D_M D_L$	V_O	V_O (when α=1 and V_{DD}=1.2V)
00	$\frac{6\cdot\alpha\cdot V_{CM}}{6+12\cdot\alpha}$	200 mV
01	$\frac{V_{DD}+6\cdot\alpha\cdot V_{CM}}{6+12\cdot\alpha}$	266.67 mV
10	$\frac{2\cdot V_{DD}+6\cdot\alpha\cdot V_{CM}}{6+12\cdot\alpha}$	333.33 mV
11	$\frac{3\cdot V_{DD}+6\cdot\alpha\cdot V_{CM}}{6+12\cdot\alpha}$	400 mV



(a)



(b)

Fig. 2-8. Equivalent circuit of SST driver with pre-emphasis when (a) $D_M D_L$ = 11 ➔ 10, and (b) $D_M D_L$ = 10 ➔ 11.

2.3. Circuit Implementation

Fig. 2-9 shows the block diagram of PAM-4 transmitter which includes a PRBS generator, two NRZ serializers, clock buffers, frequency dividers, single-to-differential (S2D), SR latch, and SST driver.

PRBS generator produces 5-Gb/s 8 PRBS 2^7-1 parallel NRZ signals, and the signals synchronized with clocks (CK_0, CK_{90}, CK_{180}, and CK_{270}) and converted into RZ data by the conventional resettable DFF as shown in Fig. 2-10. The frequency divider generates quadrature clocks from the externally supplied half-rate clocks (CK_P and CK_N) having the frequency, f_{CK} = 10GHz in our design for 40 Gb/s PAM-4 signal, which is a conventional latch type frequency divider as shown in Fig. 2-11. However, the frequency divider might cause the ambiguity in the phase relation. As an example, CK_0 generating node can be inverted, which results in generating CK_{180}. In order not to suffer the ambiguity, the supply voltage is used as a reset signal.

The two serializers composed of simple logic gates as shown in Fig. 2-9 produces transition signals, T_{MR}, T_{MF} for MSB and T_{LR}, T_{LF} for LSB respectively, according to Eq. (2.1) and (2.2). However, the output of serializers are sensitive to the conditions of phase alignment in

multiphase clocks, since there is no additional sampling process after RZ data aligner. Accordingly, the tunable delay buffer is used for controlling the phase of multiphase clocks externally. The buffer can control the phase from 0 ps to 38.5 ps by varying the voltage of V_{BIAS} from 0 V to 0.8 V as shown in Fig. 2-12.

S2Ds generate the differential signals from T_{MR}, T_{MF}, T_{LR} and T_{LF} for the differential signaling as shown in Fig. 2-9. As shown in Fig. 2-13(b), the SR latch [16] converts the transition signals into NRZ data. Additionally, this can be also used for buffering the transition signals as shown in Fig. 2-13(c). So that reason, the pre-emphasized PAM-4 signal can be produced from transition signals and serialized NRZ which have same timing delay, T_D.

The transition signals and serialized signals are supplied directly to the SST driver, and the signals are summed up at the driver for pre-emphasis. Though our SST driver can control the pre-emphasis gain by varying V_{DC}, however, the V_{DC} cannot exceed half of V_{DD}, so the value of α decides the maximum gain of pre-emphasis. According to Eq. (2.4), α = 1 in our design, the maximum gain of pre-emphasis is set to 9.54 dB, and R can be calculated from Eq. (2.4), R = 450 Ω.

In order to maintain output impedance as 50 Ω, the summation of each series resistor, R_L, R_{PRE}, $R_L/2$, and $R_{PRE}/2$, and each turn-on

resistor of input transistors should be equal to R, R, R/2, and R/2 respectively as shown in Fig. 2-6 and 2-14, and each resistor can be calculated from Eq. (2.4) as R = 450 Ω, R/ α = 450 Ω, R/2 = 225 Ω, and R/2α = 225 Ω. For this, the signals supplied to the input transistors should be clipped as shown in Fig. 2-14, which enables to produce the turn-on resistance of input transistors adequately. As an example, when $t < t_0$ in the driver for MSB, the summation of $R_L/2$ and PMOS turn-on resistor should be equal to R/2, and, when $t > t_0$, the summation of $R_L/2$ and NMOS turn-on resistor should be same with R/2. In order to satisfy each case, the signal should be limited as V_1 and V_2, and it is possible by the feedback loop described in Fig. 2-15(a) and (b). Similarly, in the case of driver transmitting transition signals, V_A and V_B should be supplied. However, pre-emphasis gain is controlled by varying supply voltage in our driver, so the same supply voltage, $V_{CM}+V_{DC}$ and $V_{CM}-V_{DC}$, should be also supplied to the feedback loop as shown in Fig. 2-15(c) and (d).

By using this feedback scheme, output impedance can be maintained as 50 Ω regardless of using the pre-emphasis or not, and it can be observed in the SP simulation of Cadence. As shown in Fig. 2-16, the amount of return loss is lower than -15 dB, and it means that the output impedance of our driver is set to 50 Ω regardless of varying V_{DC}.

Fig. 2-17 shows the post-layout simulation results for the eye-diagram of differential pre-emphasized PAM-4 signal. The toggling serializers produce MSB and LSB respectively from the PRBS generator, and they are combined at the driver. As can be seen in the figures, the PAM-4 signal with/without pre-emphasis is successfully produced, and the pre-emphasis gain can be varied according to V_{DC} from 0.2 V to 0.6 V.

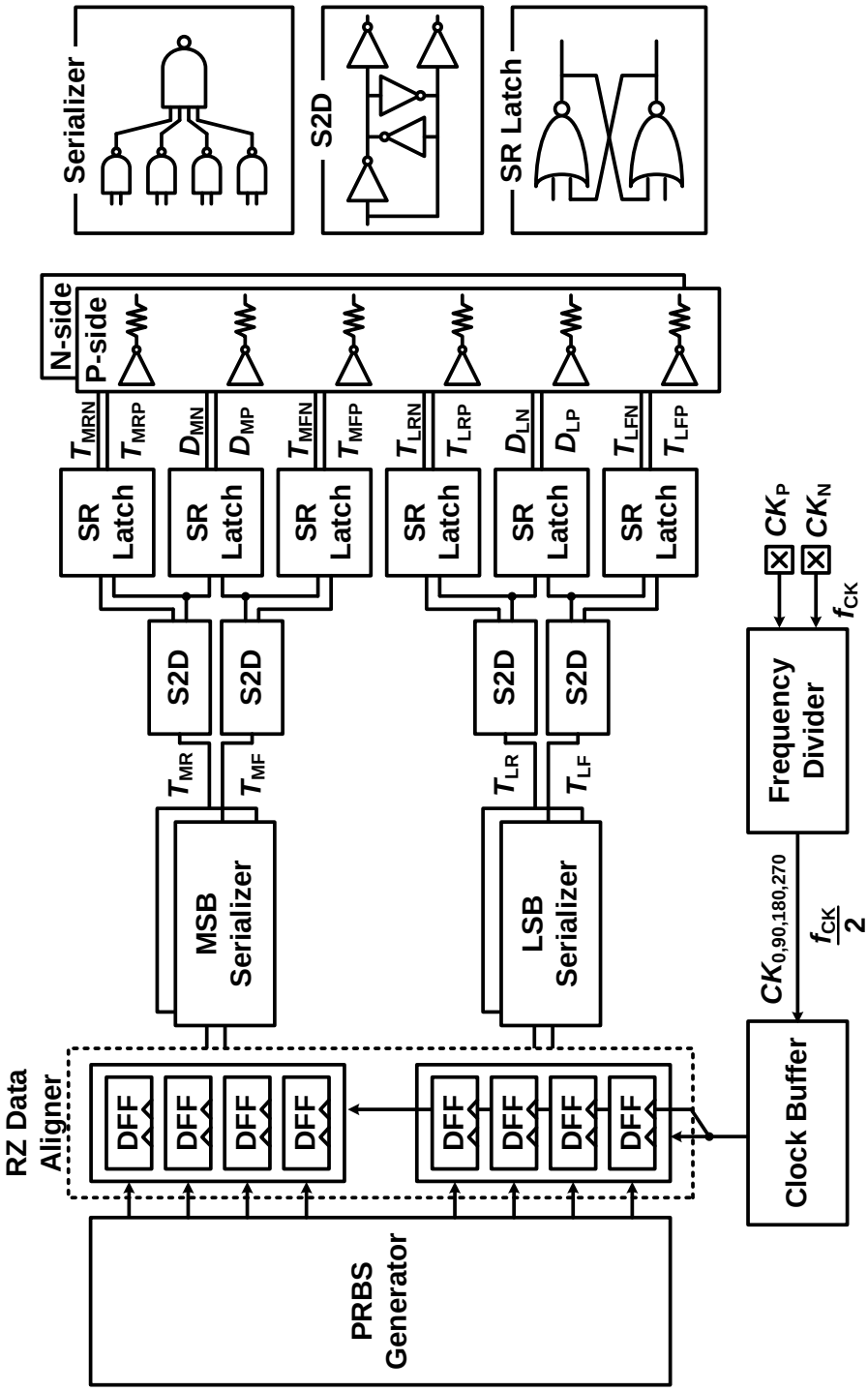
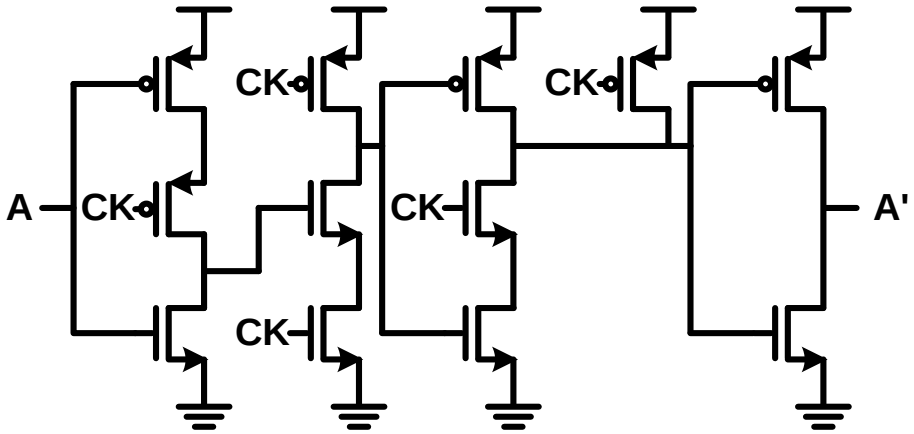
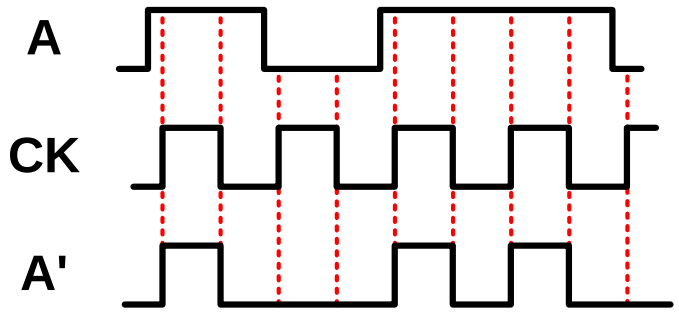


Fig. 2-9. PAM-4 transmitter.



(a)



(b)

Fig. 2-10. (a) Resettable DFF for RZ data aligner, and (b) timing diagram for RZ generation.

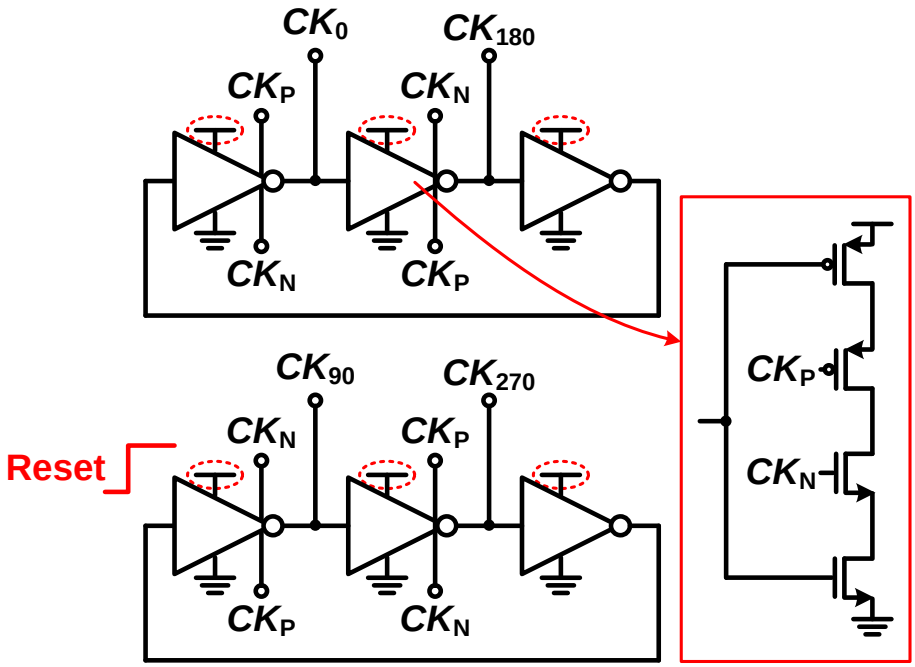
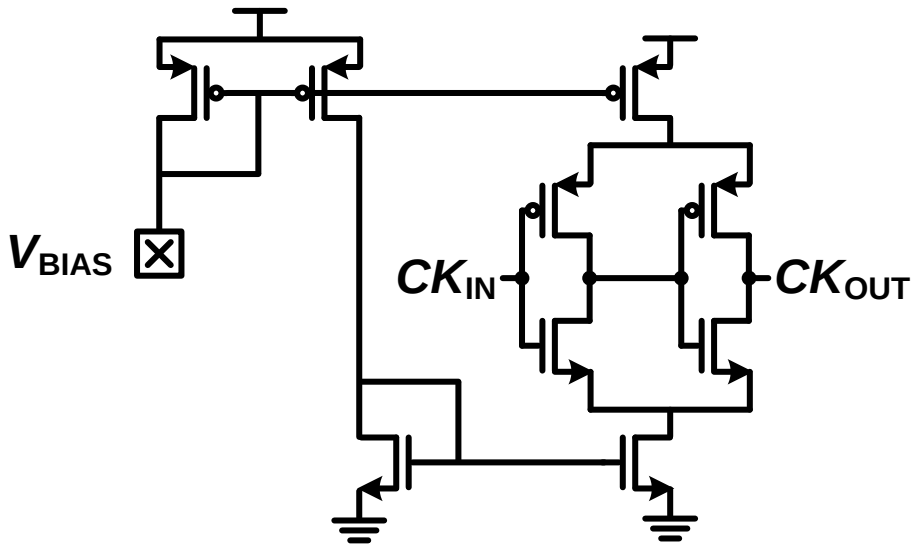
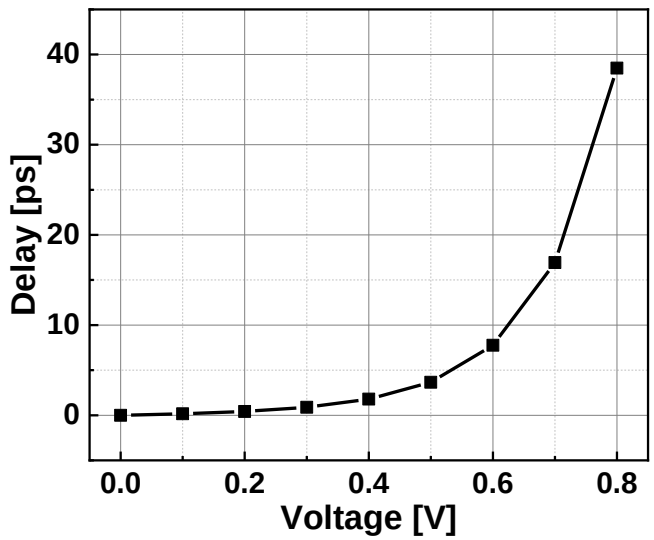


Fig. 2-11. Frequency divider for producing multiphase clocks.

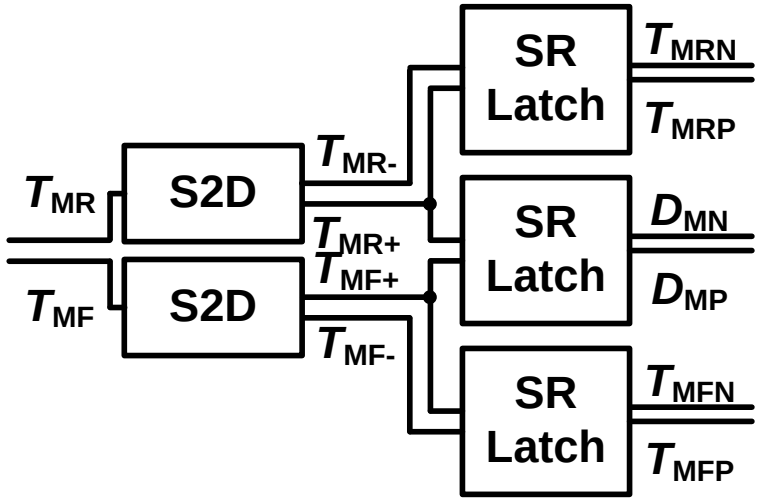


(a)

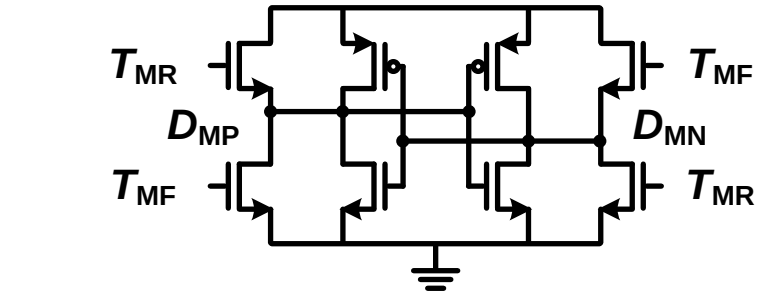


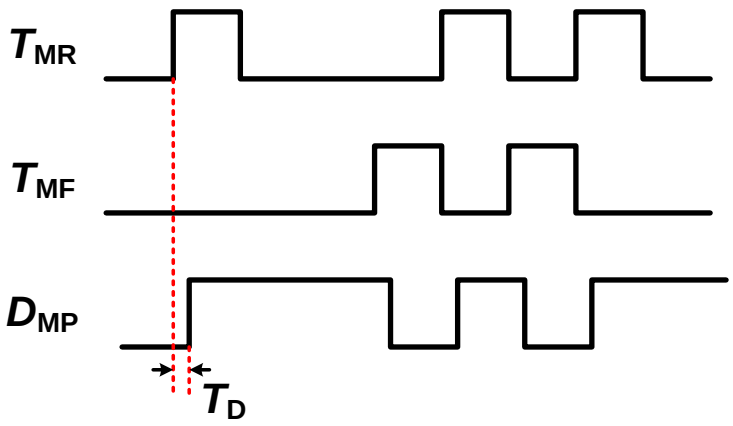
(b)

Fig. 2-12. (a) Tunable delay buffer, and (b) the simulation results of tunable delay.

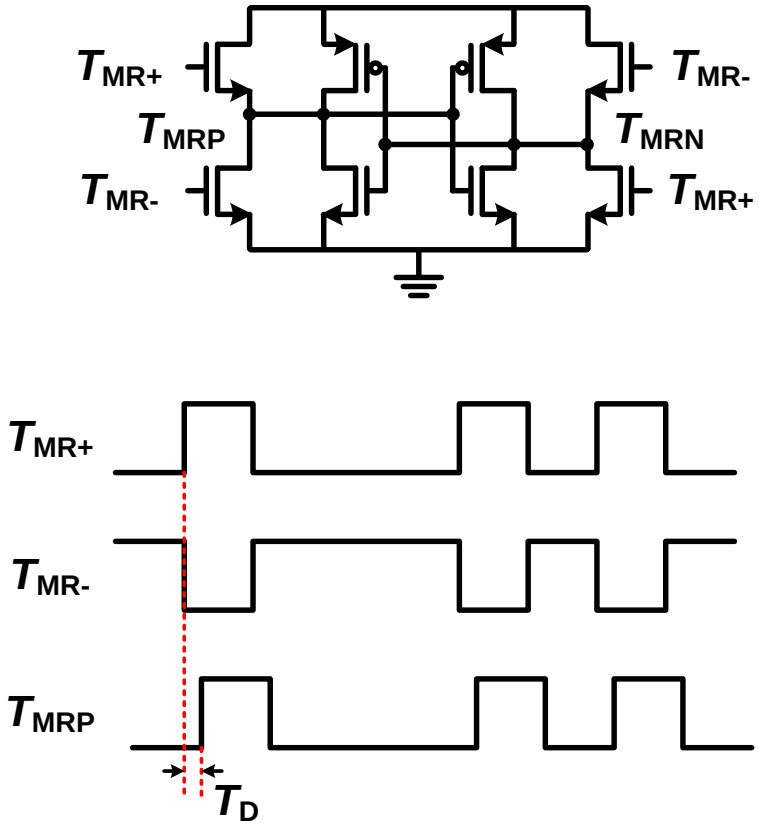

SR
Latch
SR
Latch
SR
Latch
S2D
S2D
T_{MRN}
T_{MRP}
D_{MN}
D_{MP}
T_{MFN}
T_{MFP}
T_{MR}
T_{MF}
T_{MR-}
T_{MR+}
T_{MF+}
T_{MF-}

(a)


T_{MR}
D_{MP}
T_{MF}
T_{MF}
D_{MN}
T_{MR}


T_{MR}
T_{MF}
D_{MP}
T_D

(b)



(c)

Fig. 2-13. (a) The outputs of S2D and SR latch, (b) timing diagram of producing NRZ signals, and (c) buffering transition signals.

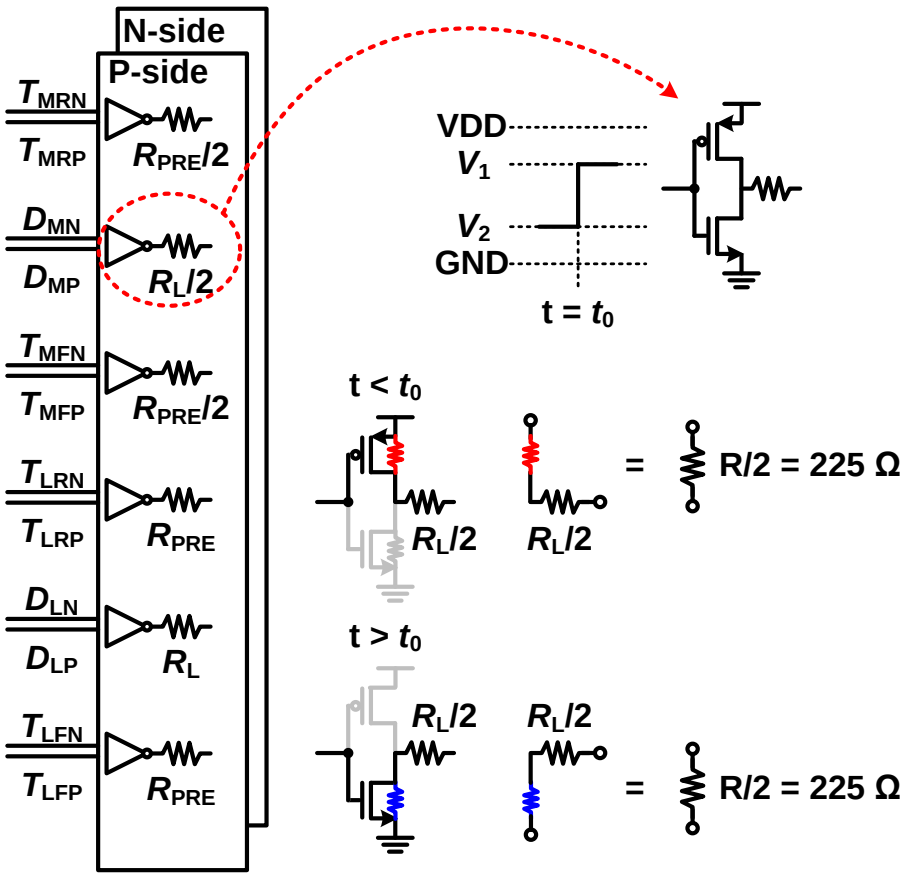
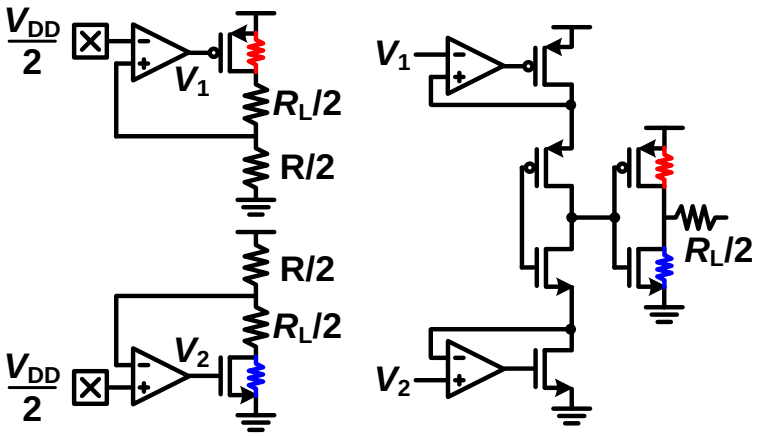
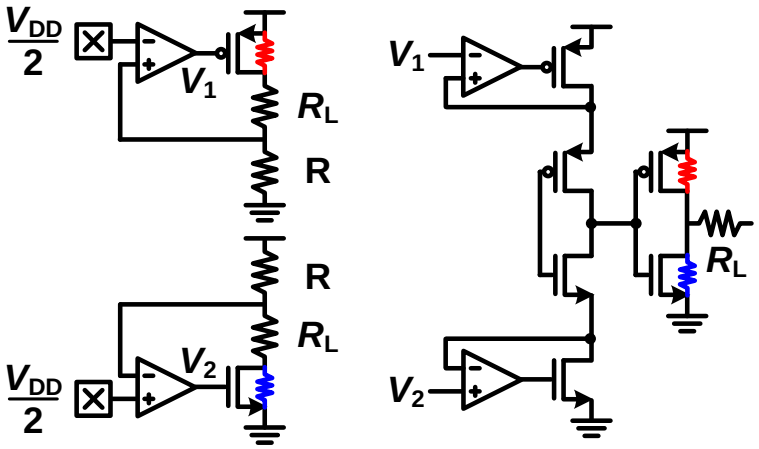


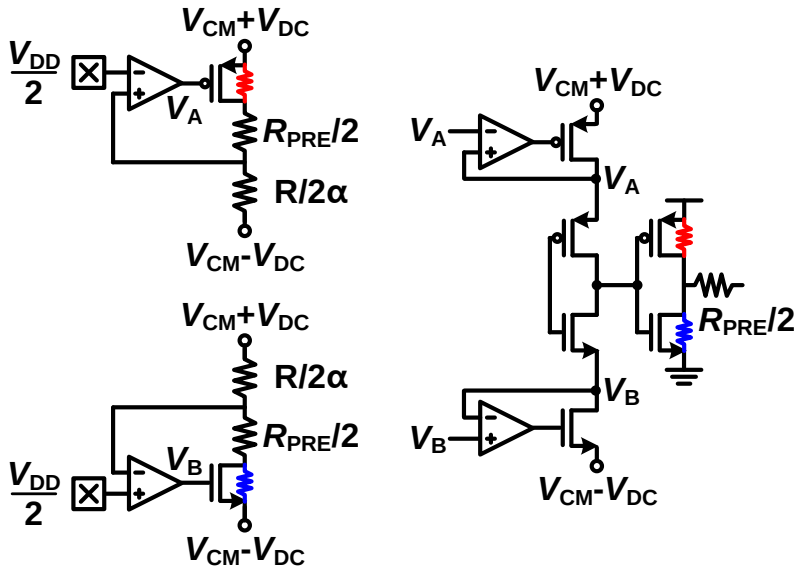
Fig. 2-14. Clipping signals to control turn-on resistance.


$\frac{V_{DD}}{2}$
V_1
$R_L/2$
R/2
R/2
$R_L/2$
V_2
$\frac{V_{DD}}{2}$
V_1
$R_L/2$
V_2

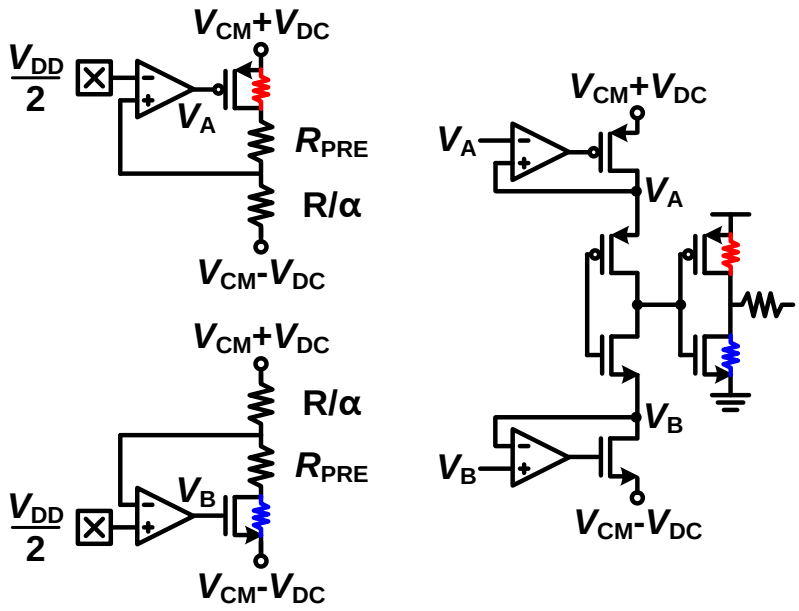
(a)


$\frac{V_{DD}}{2}$
V_1
R_L
R
R
R_L
V_2
$\frac{V_{DD}}{2}$
V_1
R_L
V_2

(b)



(c)



(d)

Fig. 2-15. The feedback loop of SST driver for (a) MSB, (b) LSB, (c) MSB pre-emphasis, and (d) LSB pre-emphasis.

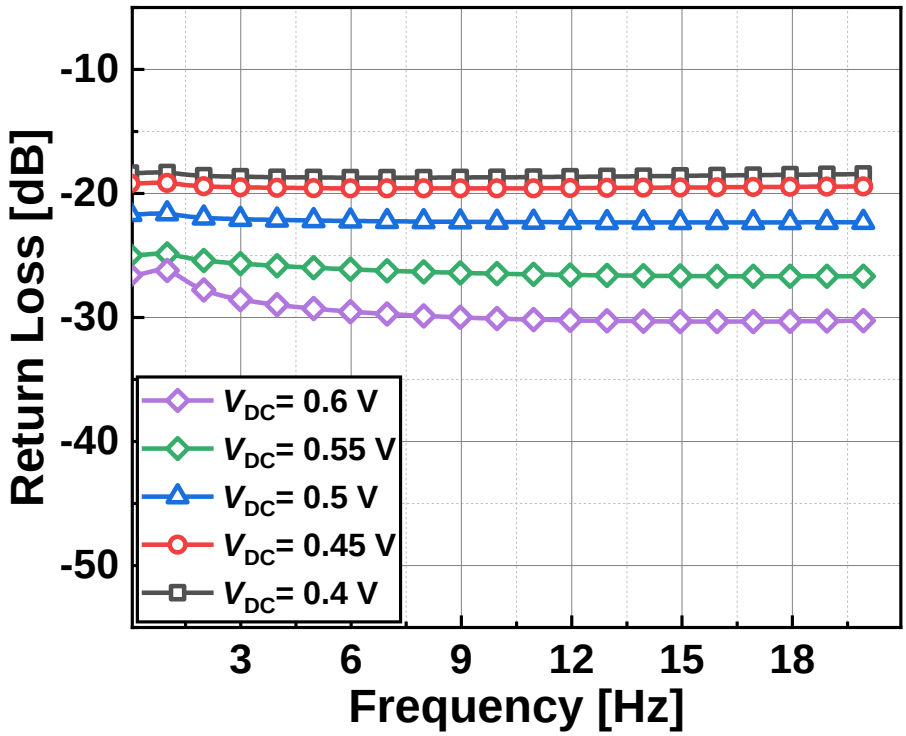
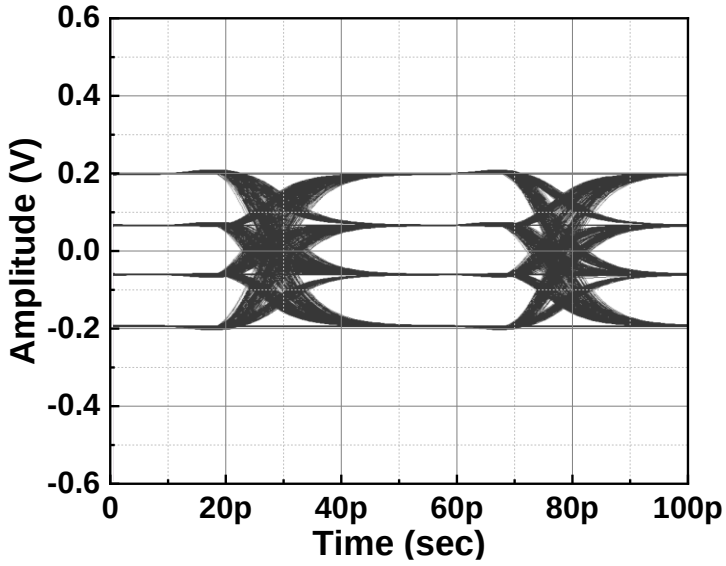
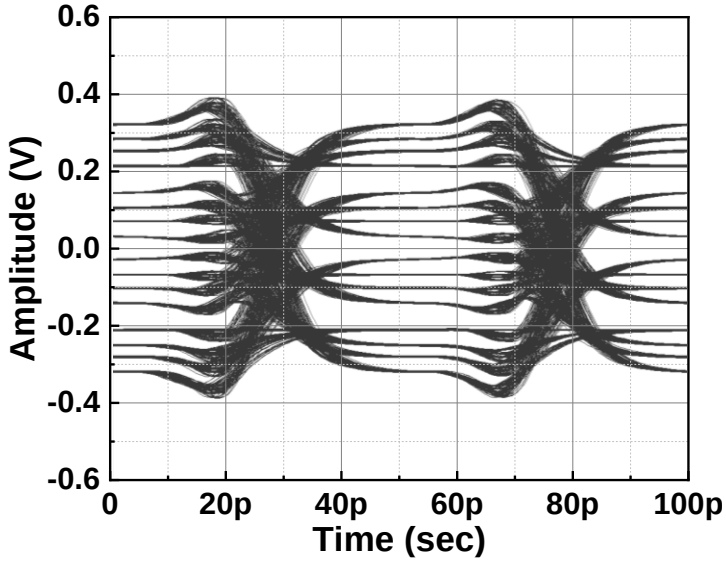


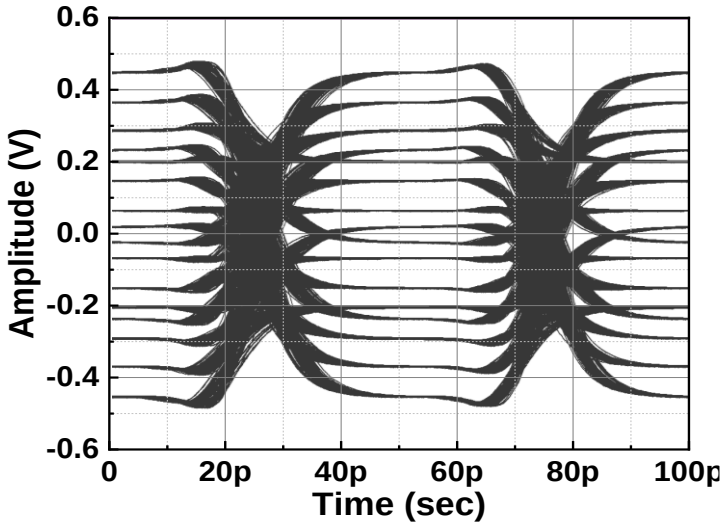
Fig. 2-16. The simulation results of return loss according to the pre-emphasis gain.


0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
Amplitude (V)
0
20p
40p
60p
80p
100p
Time (sec)

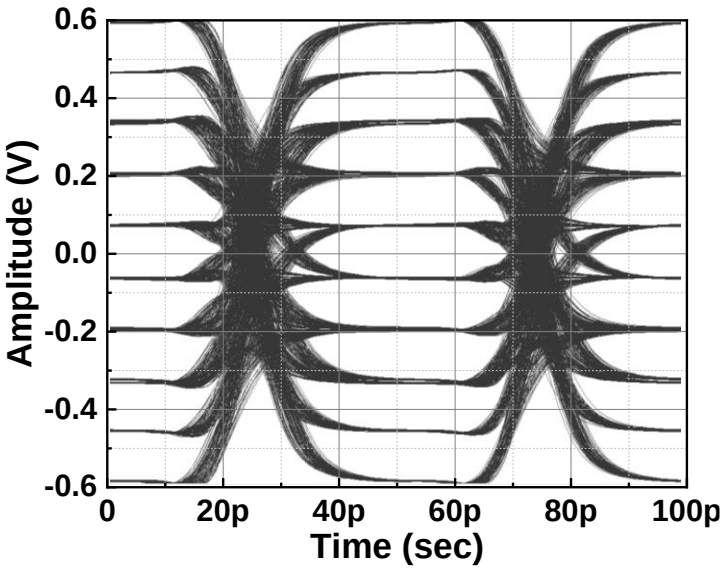
(a)


0.6
0.4
0.2
0.0
-0.2
-0.4
-0.6
Amplitude (V)
0
20p
40p
60p
80p
100p
Time (sec)

(b)



(c)



(d)

Fig. 2-17. The simulated eye-diagrams (a) without pre-emphasis, and with pre-emphasis at (b) V_{DC} = 0.2 V, (c) V_{DC} = 0.4 V, and (d) V_{DC} = 0.6 V.

3. PAM-4 Receiver

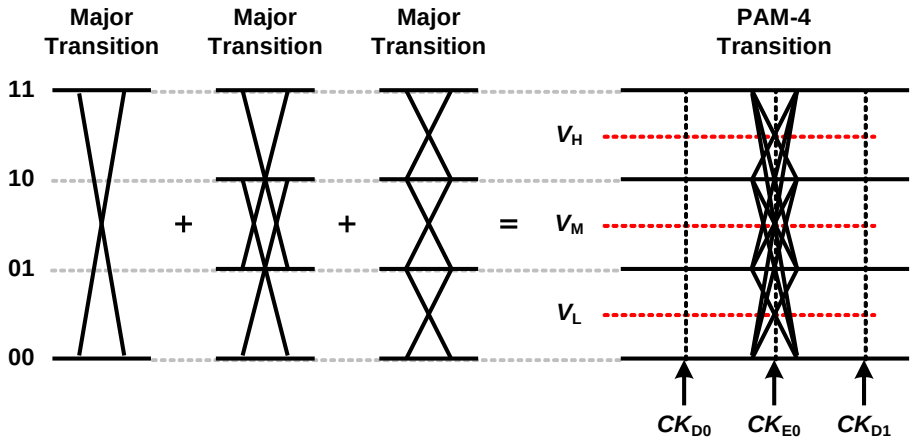
With PAM-4 signaling, the clock and data recovery (CDR) circuit becomes complicated since the phase detector should be able to determine correct phase information from various data transitions among multiple data levels [17]–[20] as shown in Fig. 3-1 (a).

For the bang-bang phase detector (BBPD) operation on PAM-4 data, received data are first sampled with clock signals (CK_{D0}, CK_{D1} for data sampling and CK_E for edge sampling) and compared with three different reference voltages (V_H, V_M, V_L). The comparator outputs are then processed with three different pairs of XOR gates for producing UP_H/DN_H, UP_M/DN_M, and UP_L/DN_L signals for up/down information for each level as shown in Fig. 3-1(b). They subsequently go through additional processing for the middle transition (00 ⇔ 10 or 01 ⇔ 11) elimination and majority voting before final UP and DN signals are produced, as shown in Fig. 3-1(c). The middle transition causes non-uniform jitter distribution [17] as graphically shown in Fig. 3-1(d). In particular, the amount of non-uniform jitter depends on the input data slew-rate as shown in the same figure. PAM-4 transmitters often employ the pre-emphasis technique with the control of the current ratio [4], [21] or output impedance [12], [22] for enhancing transmission

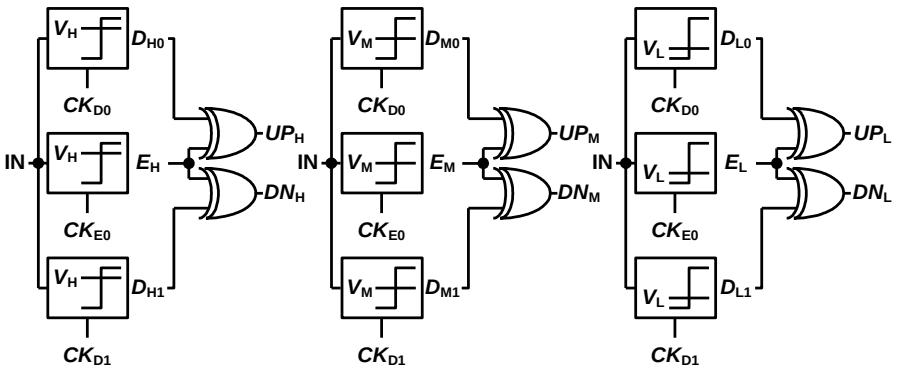
bandwidth and/or distance, resulting in slew-rate changes. With such PAM-4 transmitters, optimal design of CDR would be very difficult.

For middle transition elimination and majority voting, logic gates are used for PAM-4 data gray-coded in the transmitter [17], which complicates the transmitter design. In [18], both middle transition elimination and majority voting are done in the digital domain. But digital processing may cause the latency problem if the mismatch between input data unit interval and the digital processing time becomes significant. In addition, deserialization of sampled data for digital processing requires significant amounts of power and chip area.

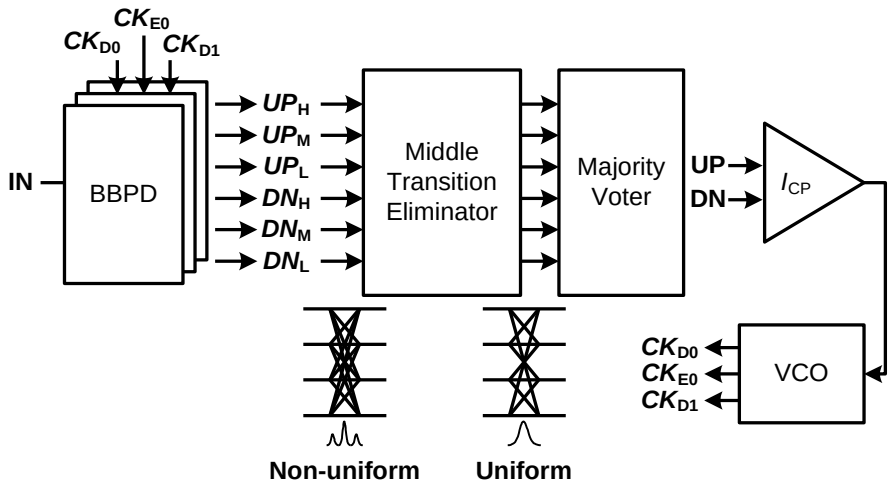
We propose a novel PAM-4 phase detector structure in which a newly proposed selective transition detector (STD) simultaneously performs elimination of the middle transition and majority voting with simple logic gates. Our STD can exclude middle transitions without any pre-coded data or deserializers, which can prevent complex design of transmitters and latency problems. In addition, we use the rotating phase detection scheme [23], [24] for realizing a quarter-rate PAM-4 BBPD for achieving reduction both in power consumption and chip.


Major Transition
Major Transition
Major Transition
PAM-4 Transition
11
10
01
00
+
+
=
V_H
V_M
V_L
CK_{D0}
CK_{E0}
CK_{D1}

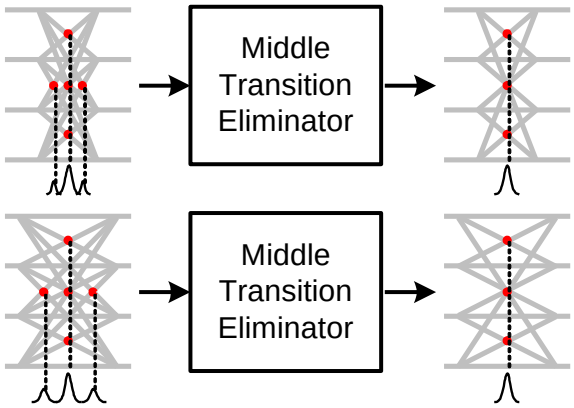
(a)


IN
V_H
D_{H0}
CK_{D0}
E_H
CK_{E0}
D_{H1}
CK_{D1}
UP_H
DN_H
V_M
D_{M0}
E_M
D_{M1}
UP_M
DN_M
V_L
D_{L0}
E_L
D_{L1}
UP_L
DN_L

(b)



(c)



(d)

Fig. 3-1. (a) Data transition in PAM-4, (b) conventional BBPD for PAM-4, (c) middle transition elimination with majority vote for multiple UP/DN signals, and (d) non-uniform jitter distribution for different input slew-rates.

3.1. Selective Transition Detector (STD)

Fig. 3-2 shows the numbers of possible UP and DN signals produced for each of three different types of PAM-4 data transitions (minor, middle, and major) as a function of Δθ representing the phase difference between edge sampling clock and data transition. For minor transitions corresponding to 00 ⇔ 01, 01 ⇔ 10, or 10 ⇔ 11 transitions, only one of three UP signals (UP_H, UP_M, UP_L) becomes high when $\Delta\theta > 0$ and only one of DN signals (DN_H, DN_M, DN_L) becomes high when $\Delta\theta < 0$, which are same with the characteristics of BBPD. For the middle transitions corresponding to 00 ⇔ 10 or 01 ⇔ 11, two among three UP signals become high when $\Delta\theta > \theta_1$ and two among three DN signals become high when $\Delta\theta < -\theta_1$. However, there is one UP signal and one DN signal when $-\theta_1 < \Delta\theta < \theta_1$. As a result, the PAM-4 BBPD exhibits non-ideal characteristics with a dead-zone and, in addition, the charge pump current is twice larger than those of minor transitions. The major transitions also have non-ideal BBPD characteristics with different output current levels as PAM-4 BBPD outputs three UP (or DN) signals when $\Delta\theta > \theta_2$ (or $\Delta\theta < -\theta_2$) and two UP and one DN signals (or one UP and two DN signals) when $0 < \Delta\theta < \theta_2$ (or $-\theta_2 < \Delta\theta < 0$). In order to avoid such transition-induced non-linearity, the outputs of

PAM-4 BBPD should be selectively reflected to the CDR loop and with a constant level.

The middle transition information can be eliminated by taking three-input XOR operation, which produces high value when the odd number of inputs are high, on UP_H, UP_M, UP_L producing UP_{XOR}, and on DN_H, DN_M, DN_L producing DN_{XOR}. As shown in Fig. 3-3(a), for minor transitions, UP_{XOR} and DN_{XOR} contain same characteristics as the conventional BBPD. However, for middle transitions, both of UP_{XOR} and DN_{XOR} are high only when $-\theta_1 < \Delta\theta < \theta_1$, thus providing no UP or DN transition information, or 'Hold' status and achieving middle transition information elimination. However, for major transitions, UP_{XOR} and DN_{XOR} do not correspond to the desired characteristics. In $0 < \Delta\theta < \theta_2$, although the UP_{XOR} should be high, it becomes low, and DN_{XOR} becomes low when $-\theta_2 < \Delta\theta < 0$. This can be corrected with UP_{OR} and DN_{OR}, which are produced with 3-input OR operation on UP_H, UP_M, UP_L and DN_H, DN_M, DN_L, respectively. All PAM-4 signal transition information can be obtained with proper logic combinations of UP_{XOR}, UP_{OR}, DN_{XOR}, and DN_{OR} logic values, as described in Table 3-1. Some transitions that do not occur are not included in Table 3-1. For example, $UP_{XOR}UP_{OR}$ or $DN_{XOR}DN_{OR} = 10$ is not possible because the number of UPs or DNs cannot be less than 1 and odd

simultaneously. $UP_{XOR}UP_{OR}DN_{XOR}DN_{OR}$ = 0101 is also impossible because the total number of UPs and DNs cannot be over 3. Those combinations in Table 3-1 can be implemented with a from Karnaugh map and can be expressed as,

$$\text{UP} = UP_{XOR} \cdot \overline{DN_{OR}} + UP_{OR} \cdot DN_{XOR} \quad (4.1)$$

$$\text{DN} = UP_{XOR} \cdot DN_{OR} + \overline{UP_{OR}} \cdot DN_{XOR} \quad (4.2)$$

As shown in Fig. 3-3(b) and (c), final UP/DN signals produced by STD show same characteristics as BBPD regardless of transition types.

In order to compare the operation of our STD with a conventional BBPD, behavior-level simulations are performed with PAM-4 data having 9 mUI rms jitter. The BBPD structure shown in Fig. 3-1(b) along with/without STD are used with an ideal charge pump having 50μA each. Fig. 3-4 shows the simulation results when PAM-4 input data have three different input slew rates. T_T is the input data rise/ fall time, and T_D represents one UI. As shown in Fig. 3-4, conventional PD has larger total charge pump current than that of our STD, this is because the STD conducts the majority voting and the middle transition eliminations simultaneously which requires only four charge pumps

compared to twelve charge pumps in case of conventional PD. From the simulation results, our STD produces the desired characteristics regardless of the variation of the input slew rate, whereas the PD characteristics of the conventional structure show significant changes when input slew-rate changes.

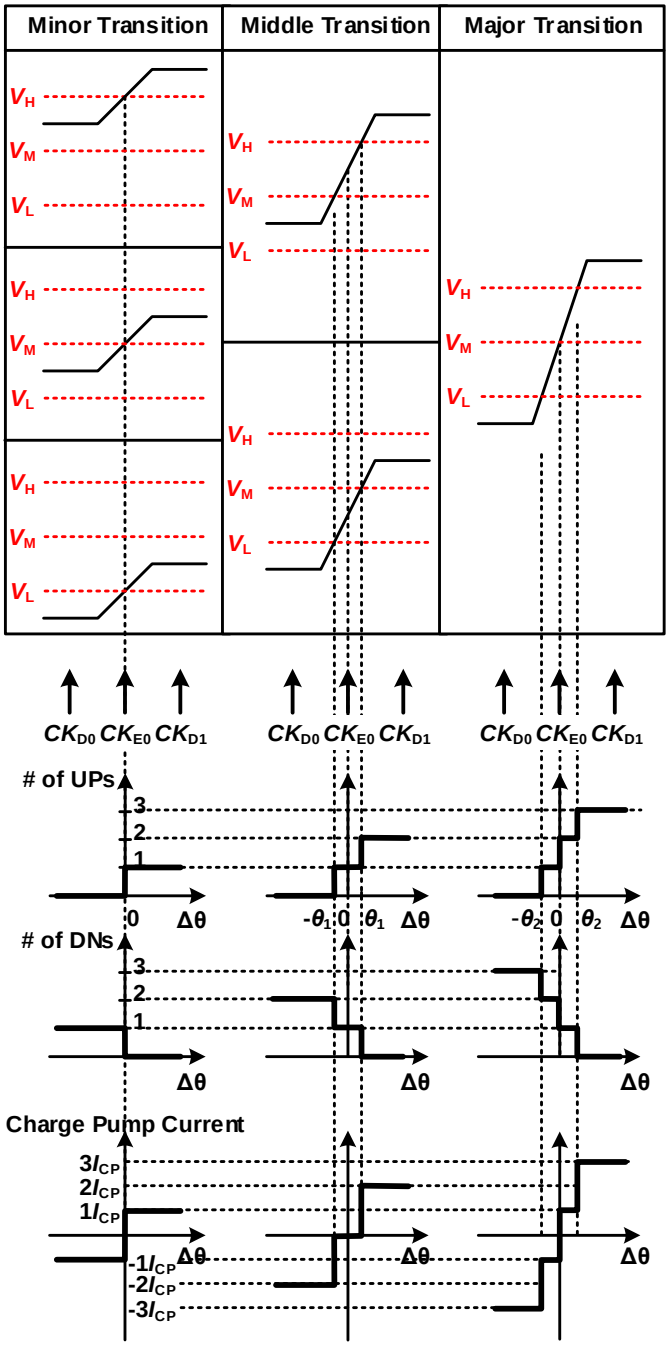
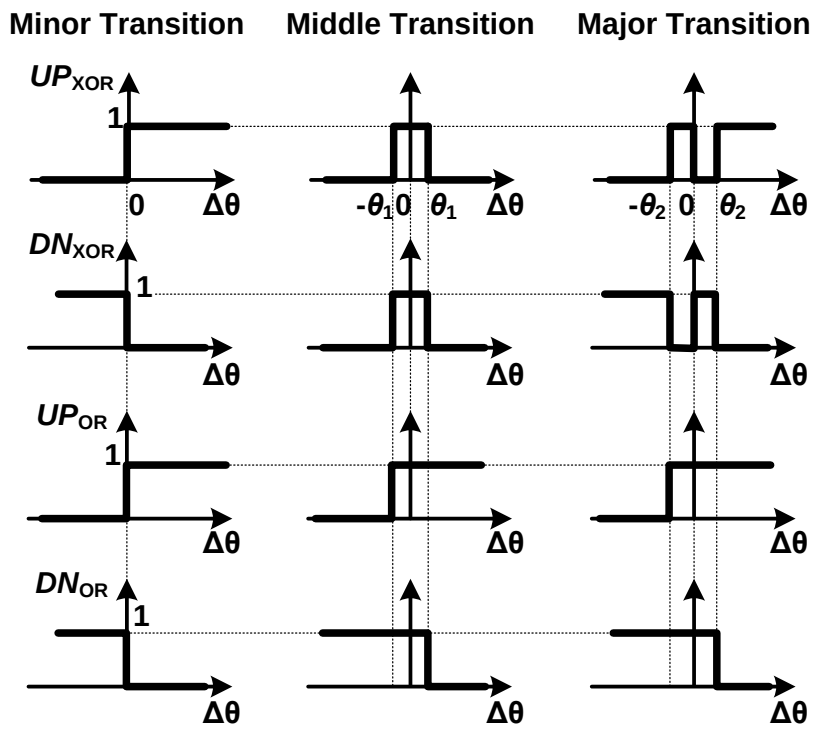
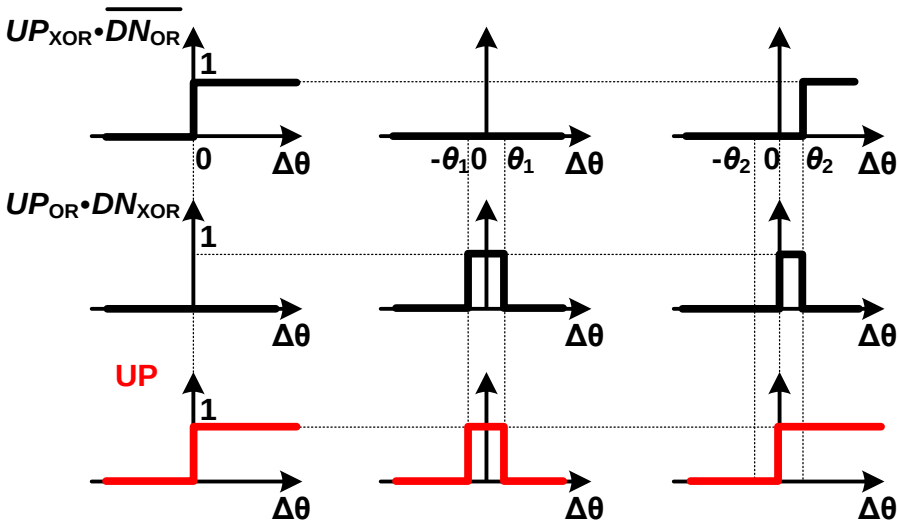


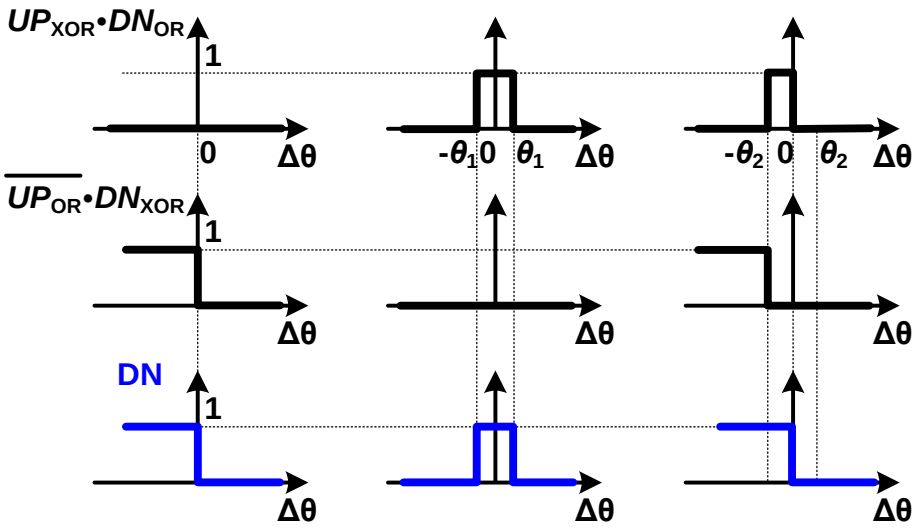
Fig. 3-2. UP/DN numbers for PAM-4 Transitions.


Minor Transition
Middle Transition
Major Transition
UP_XOR
DN_XOR
UP_OR
DN_OR
1
0
Δθ
-θ1
θ1
-θ2
θ2

(a)


UP_XOR•DN_OR
UP_OR•DN_XOR
UP
1
0
Δθ
-θ1
θ1
-θ2
θ2

(b)



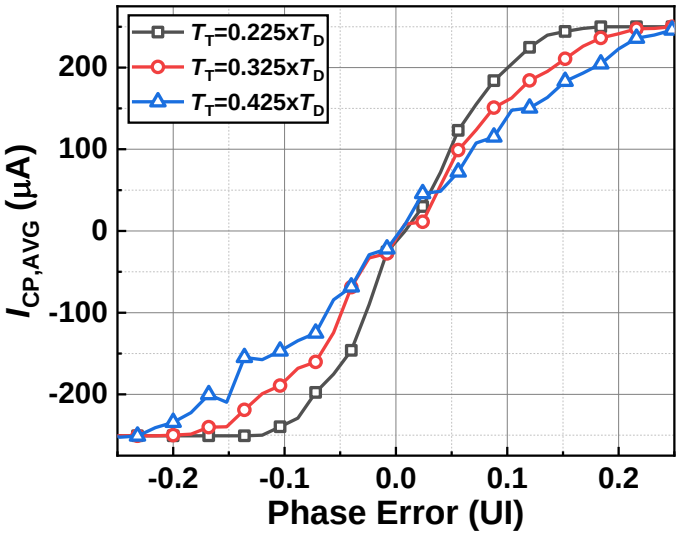
(c)

Fig. 3-3. (a) Output of 3-input XOR and OR for different transitions (b) UP operation (c) DN operation.

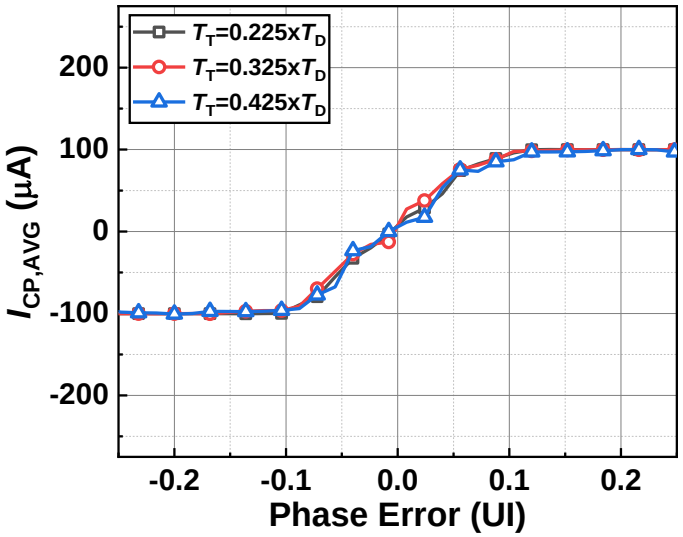
TABLE 3-1

PAM-4 SIGNAL TRANSITION STATE ACCORDING TO $UP_{XOR}UP_{OR}DN_{XOR}DN_{OR}$.

***UP*XOR*UP*OR *DN*XOR *DN*OR**	**Transitions**	**Status**
0000	No transitions	Hold
0001	# of DNs = 2 (Middle Transition)	Hold
0011	# of DNs = 1 or 3 (Minor or Major Transition)	DN
0100	# of UPs = 2 (Middle Transition)	Hold
0111	# of UPs = 2 # of DNs = 1 (Major Transition)	UP
1100	# of UPs = 1 or 3 (Minor or Major Transition)	UP
1101	# of DNs = 2 # of UPs = 1 (Major Transition)	DN
1111	# of DNs = 1 # of UPs = 1 (Middle Transition)	Hold



(a)



(b)

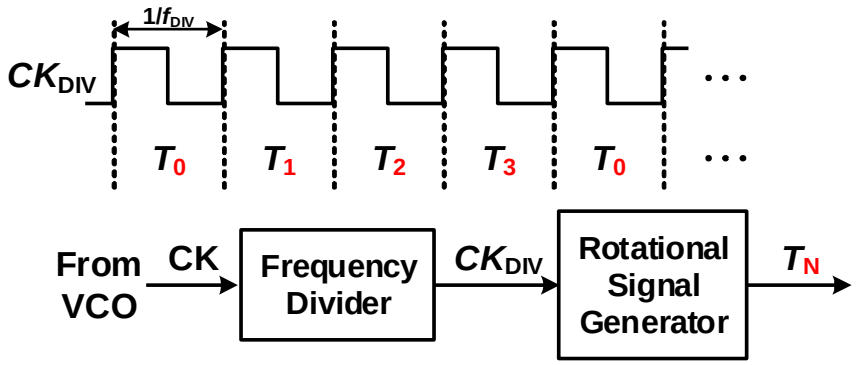
Fig. 3-4. Ideal simulation of (a) conventional phase detector gain with variations of input slew-rate, and (b) phase detector having a STD with variations of input slew-rate.

3.2. Rotational Bang-Bang Phase Detector (RBBPD)

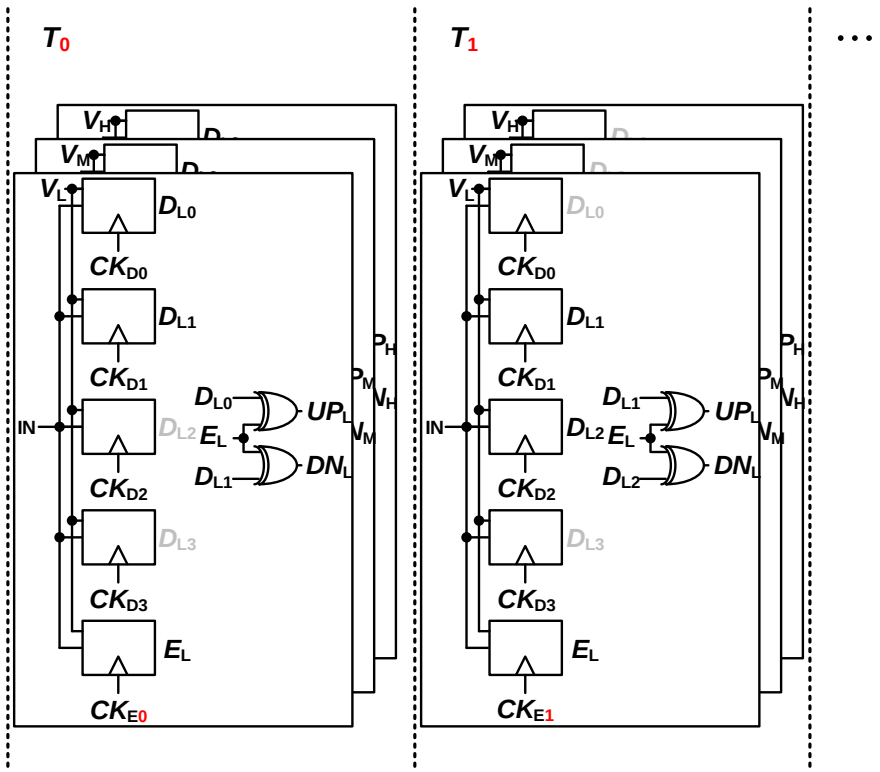
Although our STD can be used for any type of CDR, our CDR is implemented in the quarter rate so that the burden of buffering high-speed signals can be reduced and a simple ring-type VCO, which occupies much less chip area than LC VCO, can be used. Furthermore, in order to further reduce the complexity of our quarter-rate CDR, we use the edge-rotating technique [23] in which the locking point is determined with a single clock phase among sequentially rotating phases. Fig. 3-5 shows the generation of rotational signal, and the timing operation of CDR employing the edge-rotating technique. The dividing ratio of 16 is used in our design in order to make sure the rotation speed is larger than the CDR loop bandwidth and no CDR performance degradation is caused by the edge rotation [24].

Edge-sampling clocks ($CK_{E0\text{-}3}$) are provided from a multiphase VCO, and one of them is selected and used for sampling according to $T_{0\text{-}3}$, which rotates in synchronization with the divided clock (CK_{DIV}). Data sampling clocks ($CK_{D0\text{-}3}$) are continuously supplied to recover data without loss. The required logic operations on sampled data for each rotation signal are shown Table 3-2. Compared with conventional PAM-4 BBPD, we saved 9 comparators, 18 XORs, and require

additional a frequency divider, a rotational signal generator, a 4:1 MUX and 3 4:2 MUXs as shown in Fig. 3-6.



(a)



(b)

Fig. 3-5. (a) Generation of rotational signal, and (b) timing operations of edge-rotating BBPD.

TABLE 3-2

INPUT AND OUTPUT OF EDGE-ROTATING BBPD ACCORDING TO ROTATIONAL SIGNAL.

Rotational Signal	**T0**	**T1**	**T2**	**T3**
$\boldsymbol{UP_H}$	$D_{H0} \oplus E_{H0}$	$D_{H1} \oplus E_{H1}$	$D_{H2} \oplus E_{H2}$	$D_{H3} \oplus E_{H3}$
$\boldsymbol{UP_M}$	$D_{M0} \oplus E_{M0}$	$D_{M1} \oplus E_{M1}$	$D_{M2} \oplus E_{M2}$	$D_{M3} \oplus E_{M3}$
$\boldsymbol{UP_L}$	$D_{L0} \oplus E_{L0}$	$D_{L1} \oplus E_{L1}$	$D_{L2} \oplus E_{L2}$	$D_{L3} \oplus E_{L3}$
$\boldsymbol{DN_H}$	$E_{H0} \oplus D_{H1}$	$E_{H1} \oplus D_{H2}$	$E_{H2} \oplus D_{H3}$	$E_{H3} \oplus D_{H0}$
$\boldsymbol{DN_M}$	$E_{M0} \oplus D_{M1}$	$E_{M1} \oplus D_{M2}$	$E_{M2} \oplus D_{M3}$	$E_{M3} \oplus D_{M0}$
$\boldsymbol{DN_L}$	$E_{L0} \oplus D_{L1}$	$E_{L1} \oplus D_{L2}$	$E_{L2} \oplus D_{L3}$	$E_{L3} \oplus D_{L0}$

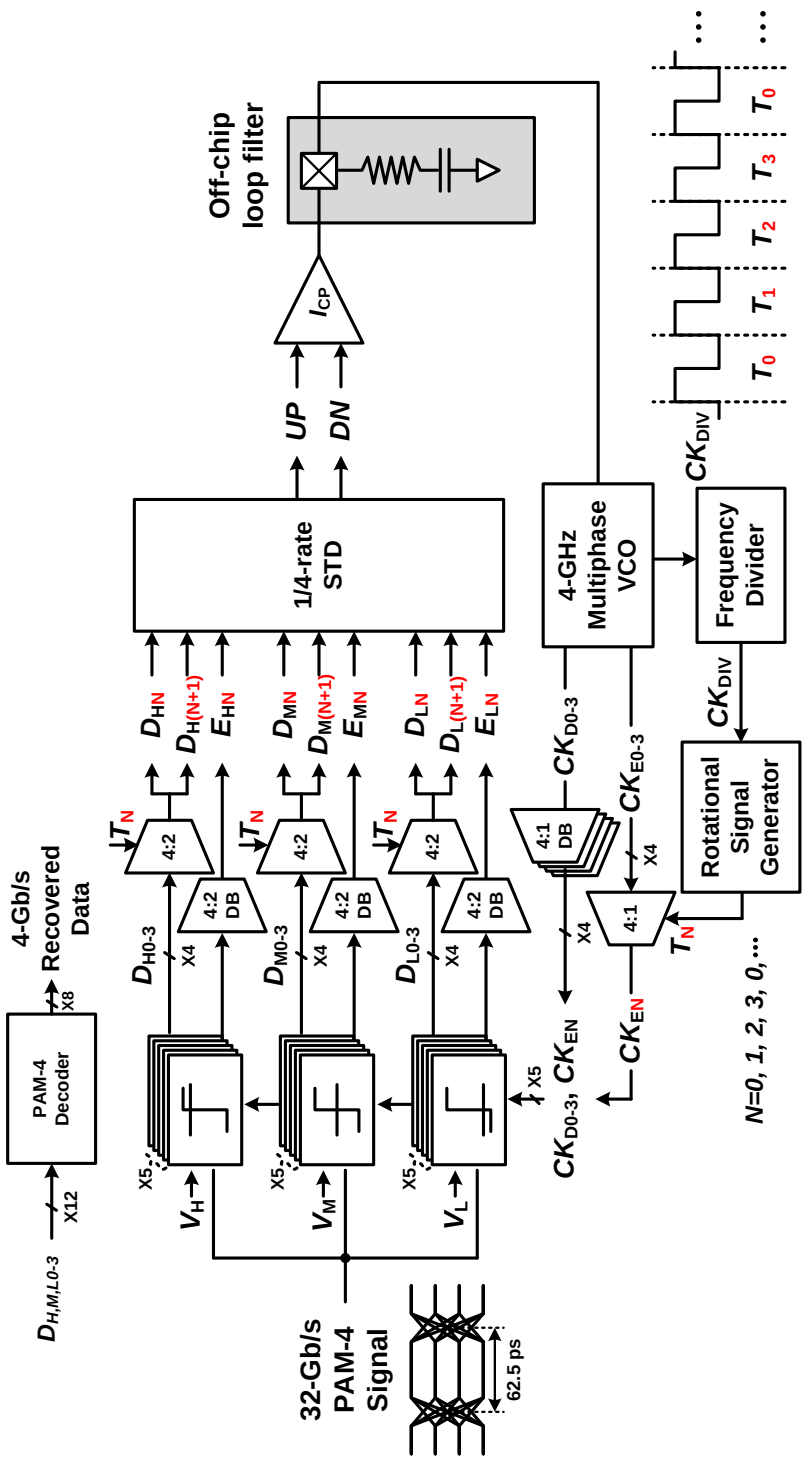


Fig. 3-6. Block diagram of proposed PAM-4 CDR.

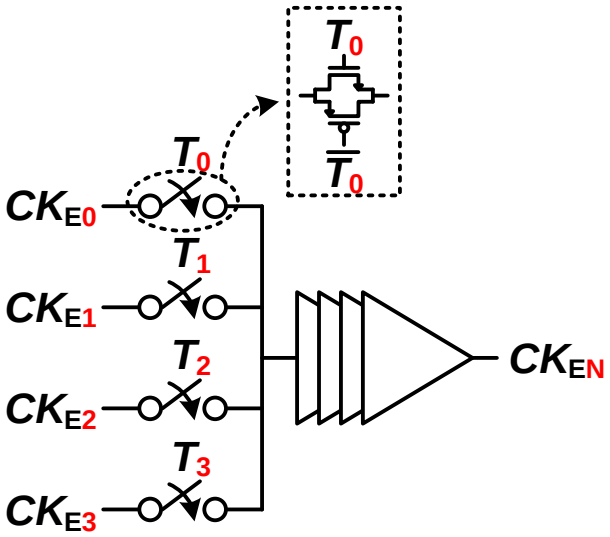
3.3. Circuit Implementation

Fig. 3-6 shows the block diagram of our quarter-rate edge- rotating PAM-4 CDR with the STD. It is composed of 15 comparators, three 4:2 MUXs, one of 4:1 MUX, frequency divider, rotational signal generator, charge pump, multiphase VCO and 1/4-rate STD. The reference voltages (V_H, V_M, and V_L) for comparators, clocked sense amplifiers [25], are externally provided. The charge pump has the structure given in [26]. The loop filter is implemented off-chip. The divided-by-16 clock signal is used for generating rotating signals.

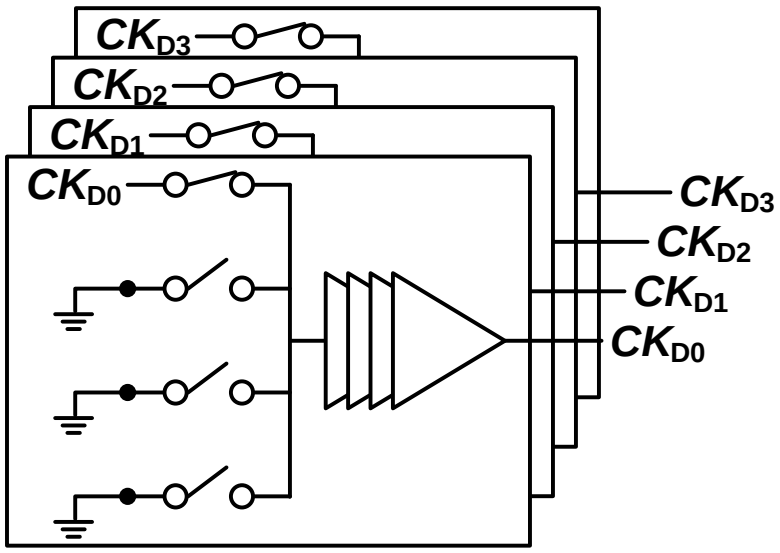
4:1 MUXs for rotating edge-sampling clocks are designed with the structure shown in Fig. 3-7. 4:1 dummy buffers (DB) having the same structures are also used to minimize the phase skew between data-sampling and edge-sampling clocks. These schemes are also used for 4:2 MUXs and 4:2 DBs for BBPD outputs to minimize the skew between sampled data by CK_{EN} and $CK_{D0\text{-}3}$. As shown in Fig. 3-8, 3-input XOR and 3-input OR gates are designed with the same structure for 2-input NAND gates, to minimize the delay mismatch between UP/DN signals. Fig. 3-9 shows the schematics of the 4-stage pseudo-differential ring-type 8 phase VCO with Lee-Kim delay cell [17] used in our design.

As shown in the Fig. 3-10, a 2-bit counter and a 2-to-4 binary decoder generate 4-bit digital codes (T_0, T_1, T_2, T_3) for selecting the correct edge-tracking clock and sampled data outputs in synchronization with divided-by-16 clock signal. Fig. 3-10(c) shows the timing diagram of output signals.

PAM-4 decoder recovers PAM-4 signal into deserialized 8 lanes. As shown in Fig. 3-11, MSB is that same as D_{M0} and LSB becomes high when the number of sampled data (D_{H0}, D_{M0}, D_{L0}) is odd. The recovered and deserialized MSB can be produced by sharing the sampler used in BBPD, and the LSB is produced by 3-input XORs using BBPD outputs (D_{H0}, D_{M0}, D_{L0}) when the sampling clock is CK_{D0}. Though our CDR can produce 8 outputs simultaneously, we designed a 8:1 MUX for decreasing the number of outputs. The same structure shown in Fig. 3-7(a) is used for a 4:1 MUX which select the output among recovered signals by CK_0, CK_{90}, CK_{180}, CK_{270}. Then, from the decoder, MSB and LSB is produced, and one of them is selected at the final MUX as shown in Fig. 3-12. The sampler finally samples the selected data with the recovered clock, and the tunable buffer as shown in Fig. 2-12 varies the phase of the clock externally in order not to sacrifice the BER performance.

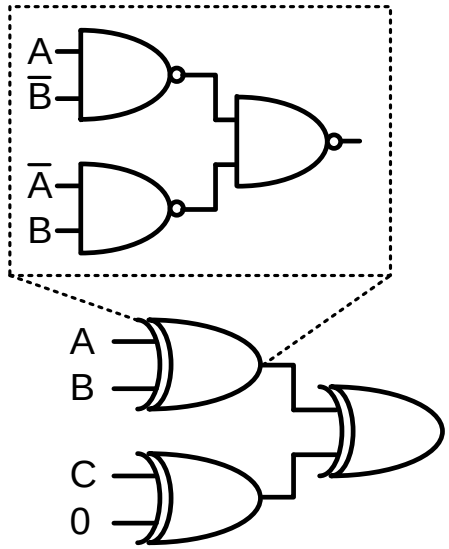


(a)

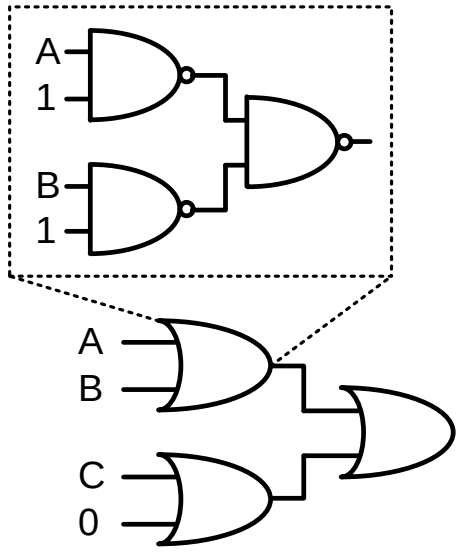


(b)

Fig. 3-7. (a) Clock buffers for edge-sampling locks, and (b) dummy buffers for data sampling clocks.

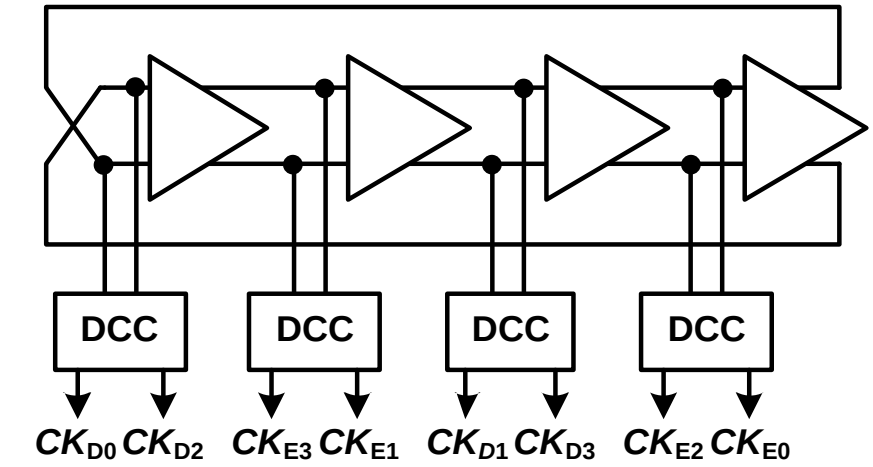


(a)

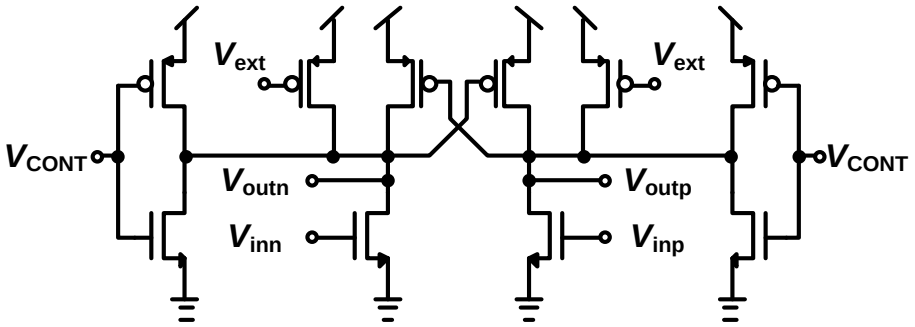


(b)

Fig. 3-8. (a) 3-input XOR, and (b) 3-input OR.

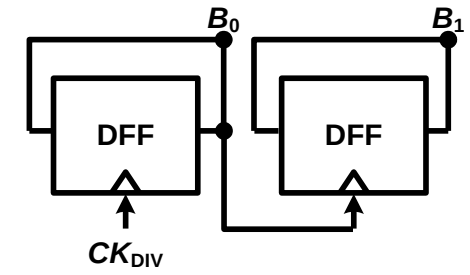


(a)

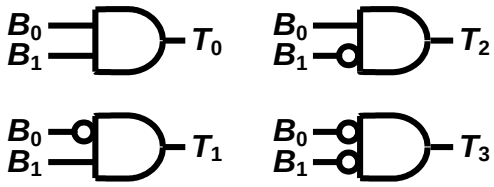


(b)

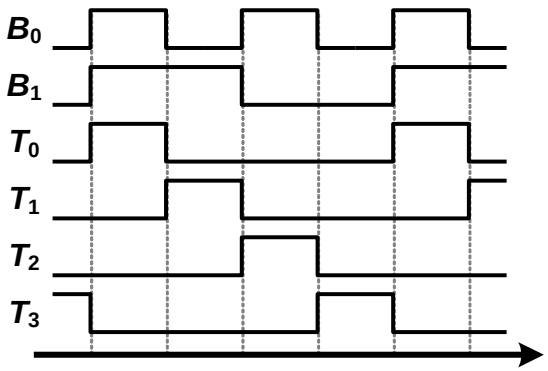
Fig. 3-9. (a) 8-phase VCO, and (b) delay-cell.



(a)



(b)



(c)

Fig. 3-10. (a) Rotational signal generator, (a) 2-bit counter, (b) 2-to-4 binary decoder, and (c) timing diagram of the decoder.

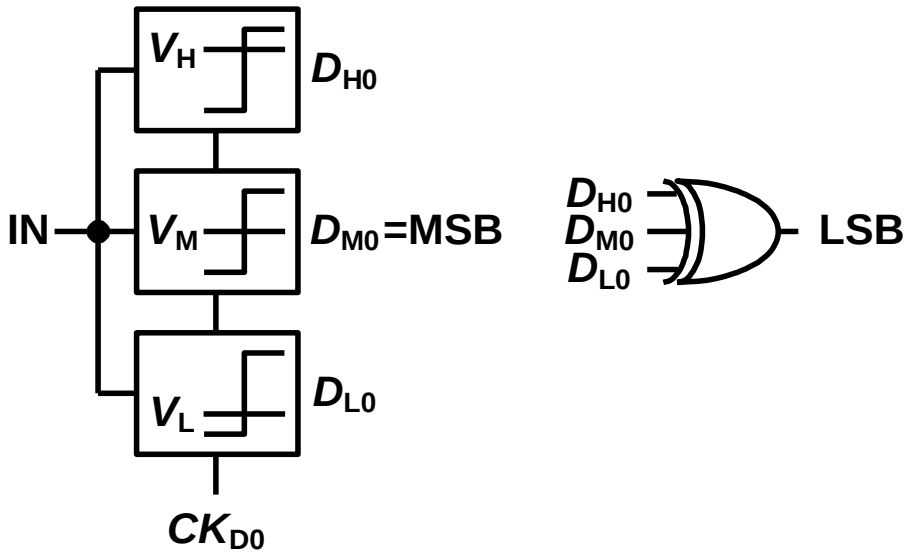


Fig. 3-11. PAM-4 decoder.

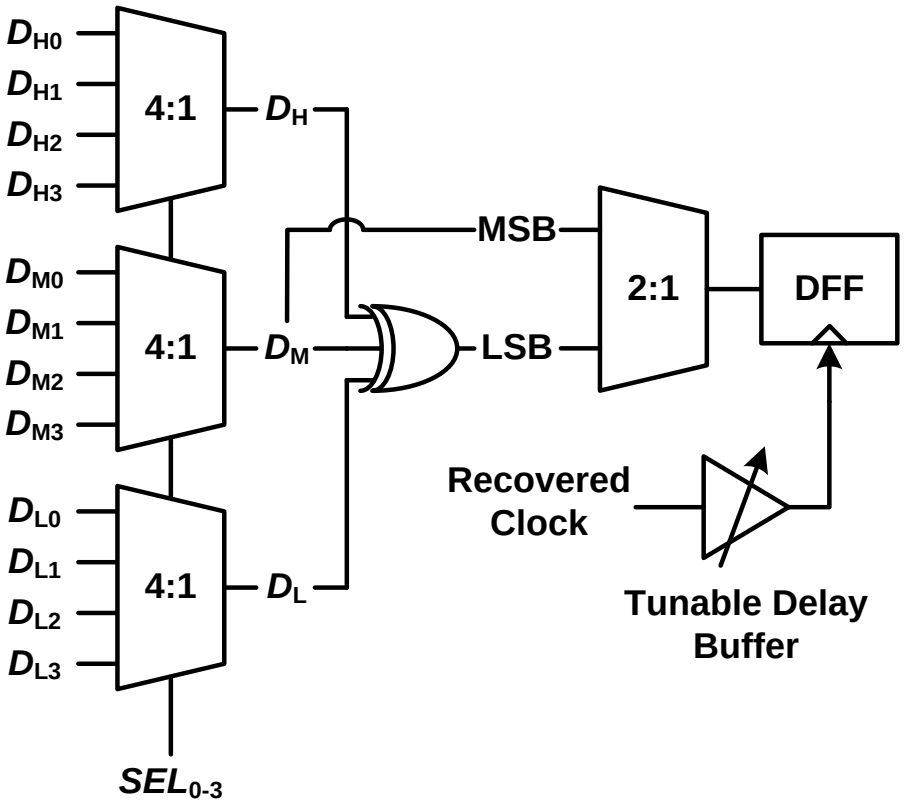


Fig. 3-12. PAM-4 decoder with a 8:1 MUX.

4. Measurement Results

4.1. PAM-4 Transmitter

A prototype 40-Gb/s PAM-4 transmitter is implemented in 28-nm CMOS technology. The chip microphotograph and the measurement setup are shown in Fig. 4-1. The chip is mounted on a FR-4 printed circuit board. The high frequency signals are probed while the low frequency signals including DC voltage are wire-bonded. The circuit consumes 47.9 mW at 1.2-V supply voltage without pre-emphasis and 67.3 mW with the highest pre-emphasis gain, and it occupies 0.0084 mm^2, and the power consumption and chip area of each block shown in Table 4-1.

An integrated pulse pattern generator (PPG) produces eight 5-Gb/s PRBS 2^7-1 data sequences, four for MSB and others for LSB, and generated PAM-4 signals from the transmitter are observed by a digital sampling scope. Fig. 4-2 shows the eye-diagram of input PAM-4 data without pre-emphasis.

In order to confirm controlling of the pre-emphasis gain, three types of channel are used as shown in Fig. 4-3. According to the channel response, V_{DC} is changed to compensate the channel loss. As shown in Fig. 4-4, it can compensate the loss according to the channel response

by controlling the pre-emphasis gain. In our design, α is set to 1, and the V_{DD} is 1.2 V. The 0.2-V, 0.4-V, 0.6-V V_{DC} are used to control the gain, so the pre-emphasis gain are 4.44-dB, 7.36-dB, and 9.54-dB respectively.

Fig. 4-5 shows the measured return loss according to V_{DC}. As shown in the figure, our driver can satisfy the return loss mask of CEI-56G-VSR regardless of the change of the pre-emphasis gain.

The performance of our PAM-4 transmitter is compared with previously reported PAM-4 transmitter in Table 4-1. As can be seen in the table, our PAM-4 transmitter occupies the smallest chip area and achieves relatively small power efficiency.

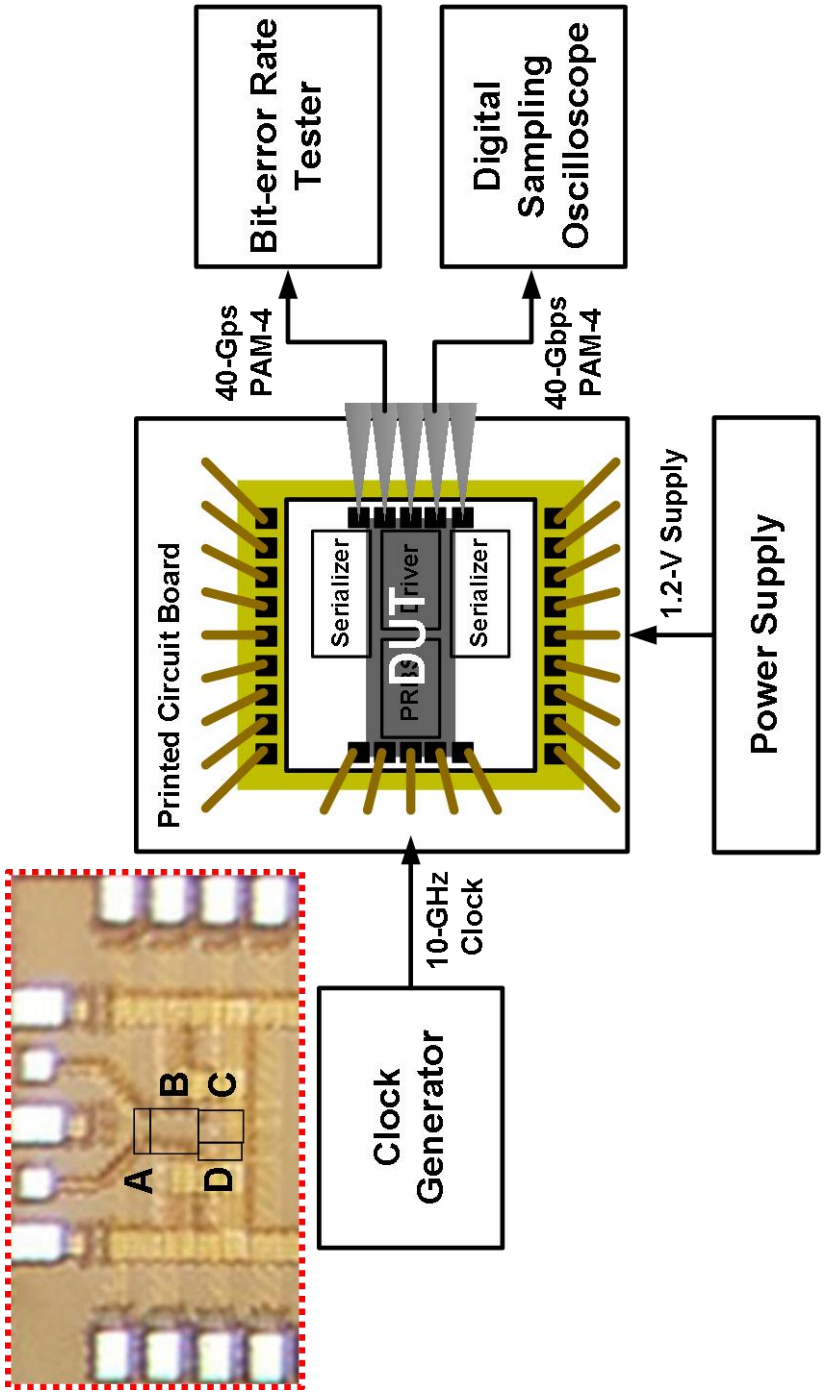


Fig. 4-1. Chip microphotograph and measurement setup of PAM-4 transmitter.

TABLE 4-1
POWER AND AREA CONSUMPTION OF EACH BLOCK.

	Blocks	**Power (mW)**	**Area (mm^2)**
A	SST driver	7.53	0.0009
B	Serializer	15.1	0.0038
C	PRBS generator	3.82	0.0024
D	Clock buffer	15.7	0.0013

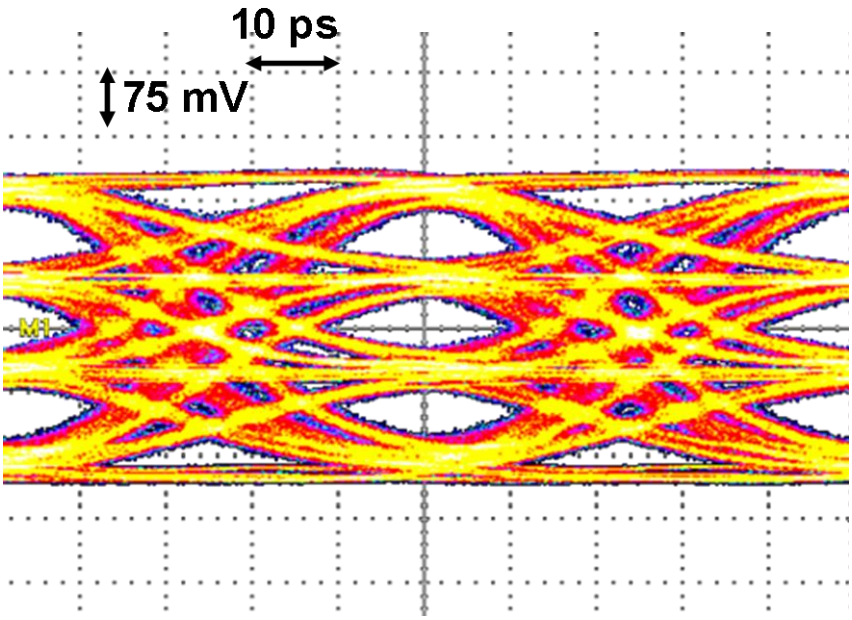


Fig. 4-2. 40-Gbps PAM-4 eye-diagram.

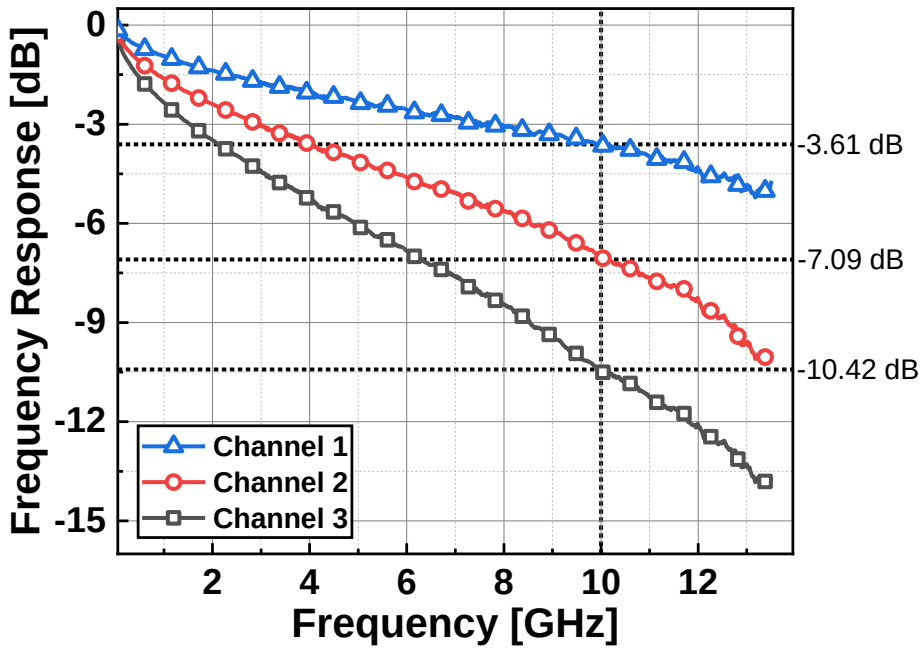


Fig. 4-3. Three types of channel.

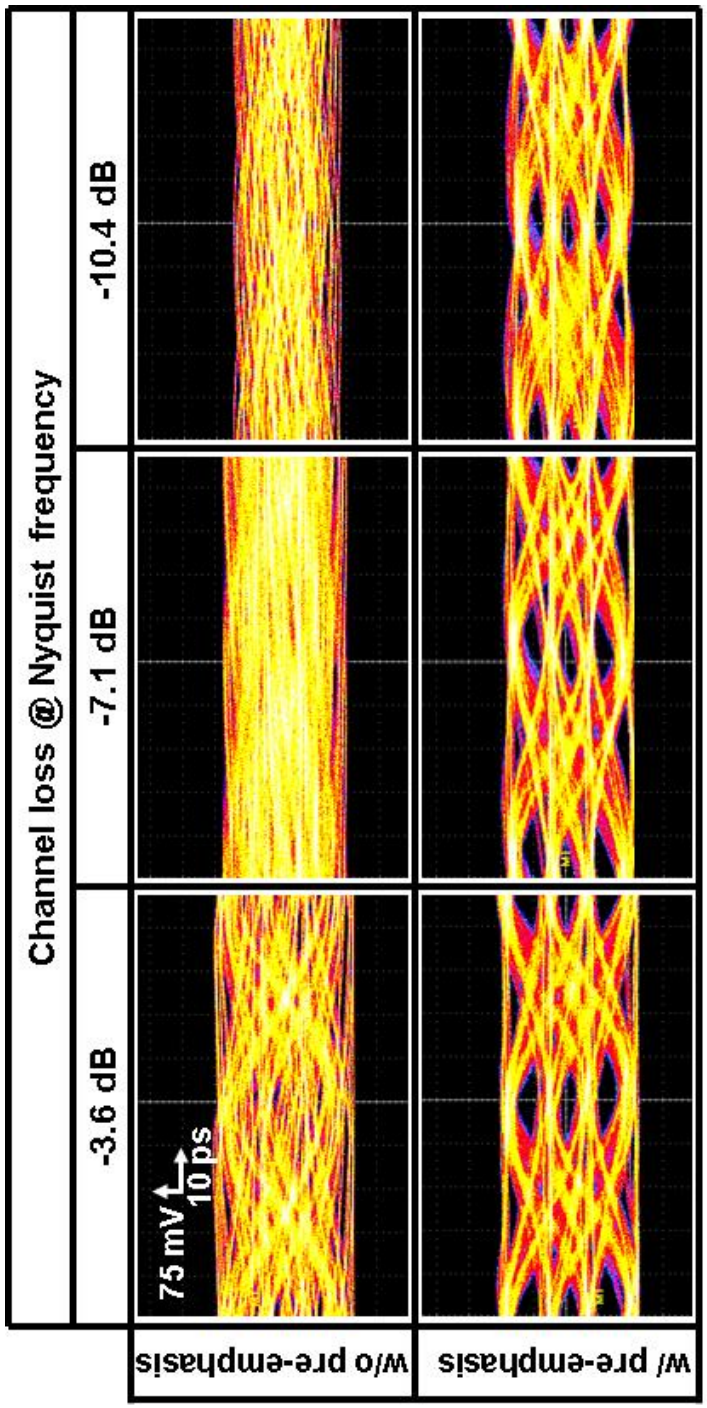


Fig. 4-4. Eye-diagrams of with/without pre-emphasis according to the channel response.

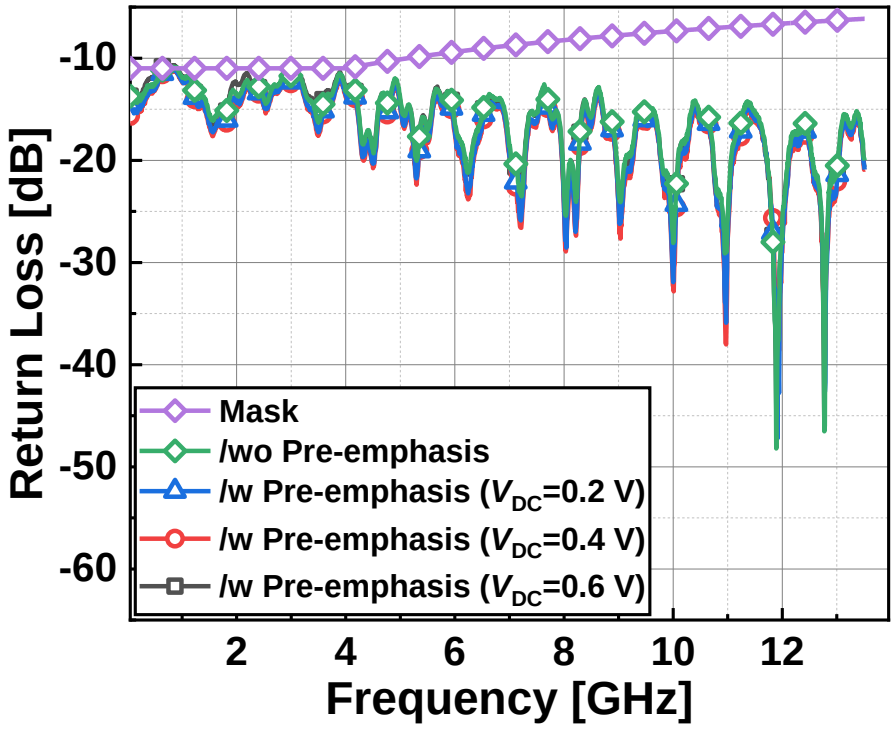


Fig. 4-5. Measured return loss.

TABLE 4-2.

PERFORMANCE COMPARISON WITH PAM-4 TRANSMITTER.

	[29]	[28]	[27]	[19]	[12]	[4]	This Work
Data-rate	16-40	64	56	56	56	45	40
Equalization	No Eq.	4-taps	3-taps	3-taps	3-taps	4-taps	2-Taps
Power (mW)	167.5	145	140	200	`100.7	120	67.3
Active area (mm^2)	0.0279	N/A	N/A	0.8	0.035	0.28	0.0084
Technology (nm)	14	28	16	40	14	28	28
pJ/bit	4.1	2.26	2.5	3.57	1.8	2.6	1.68

4.2. PAM-4 Receiver

A prototype quarter-rate 32-Gb/s PAM-4 STD CDR is implemented in 28-nm CMOS technology. The chip microphotograph and the measurement setup are shown in Fig. 4-6. The circuit consumes 32 mW at 1.2-V supply voltage and occupies 0.0152 mm^2 excluding output buffers, and details are given in Table 4.3. The chip is mounted on a FR-4 printed circuit board and wire-bonded for measurement. A 2-channel pulse pattern generator (PPG) produces two 16-Gb/s PRBS 2^7-1 data sequences, one for MSB and the other for LSB. They are combined with a power combiner and introduced to our CDR. The recovered deserialized NRZ data and clock signals are measured by a digital sampling scope and the bit error rate is measured by a BERT. Fig. 4-7 shows the eye-diagram of input PAM-4 data, the recovered and de-serialized data/clock signal. No error was observed and the recovered clock has rms jitter of 0.0136 UI, which was accumulated during BER test.

Fig. 4-8 shows the result of jitter tolerance measurement for BER less than 10^{-12} with PRBS 2^7-1 input data. Although the amount of data edges our CDR samples in a given time interval is four times less than the conventional multiphase CDR, our CDR can satisfy the jitter

tolerance mask of CEI-56G-VSR.

The performance of our CDR is compared in Table 4-4 with those of previously reported PAM-4 CDRs. As can be seen in the table, our CDR has smaller power consumption and chip area. Our CDR shows worse jitter performance for the recovered clock. This is primary due to the ring-type VCO that we used. An external clock is used in [18] and LC VCO is used in [11], both of which should provide much better jitter performance for the recovered clock signal.

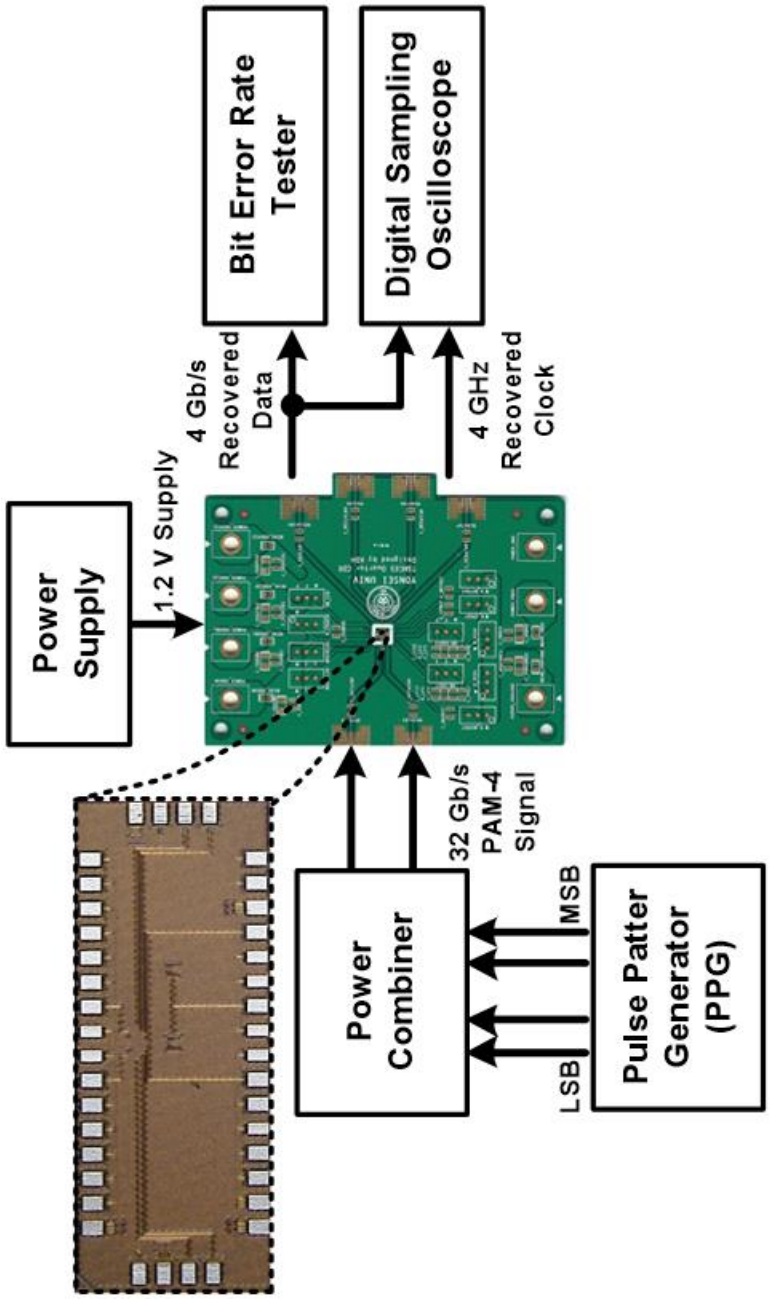
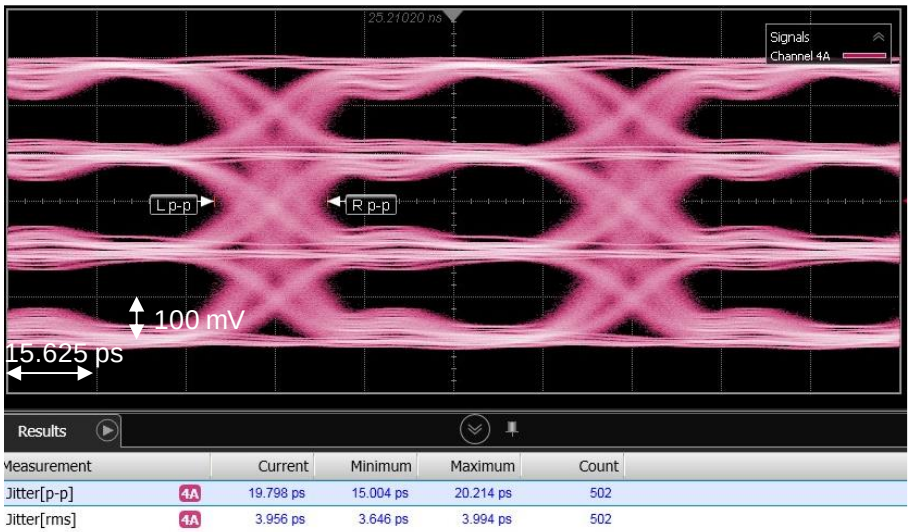


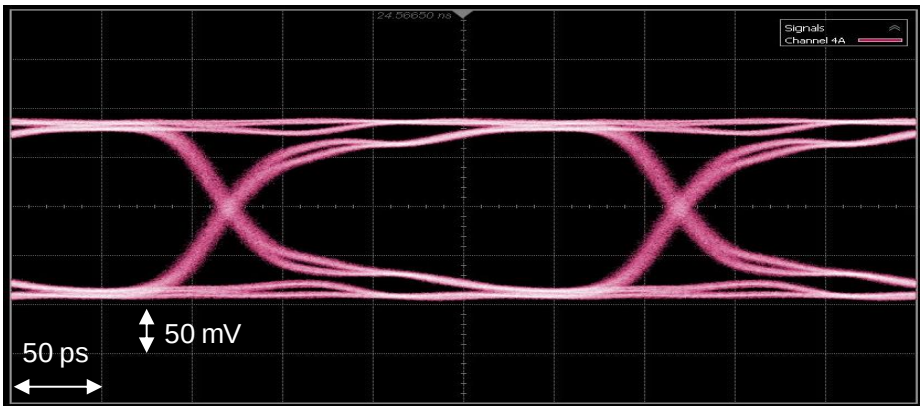
Fig. 4-6. Chip microphotograph and measurement setup.

TABLE 4-3
POWER AND AREA CONSUMPTION.

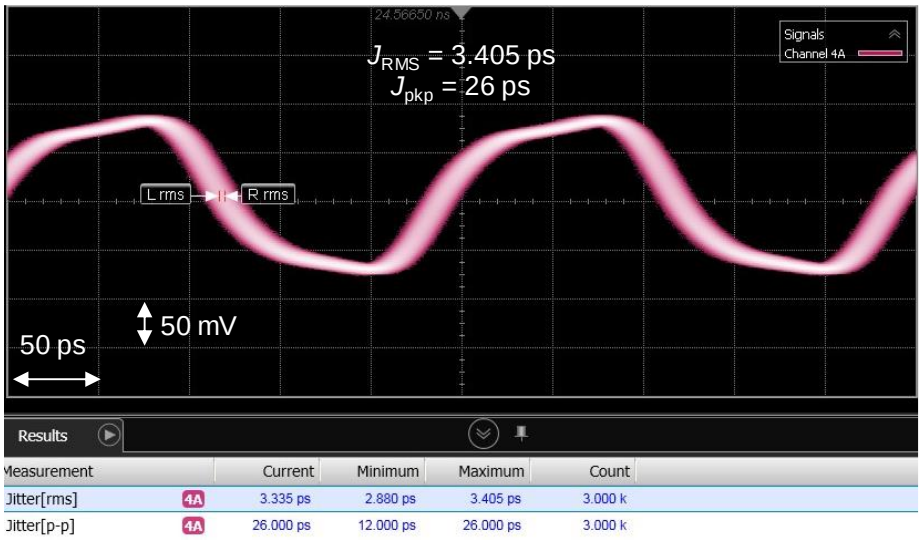
Blocks	**Power (mW)**	**Area (mm^2)**
Phase Detector w/ STD	11.75	0.0072
Rotational Signal Generator	0.6	0.0006
Clock Buffer	11.16	0.0023
VCO	5.3	0.003
PAM Decoder	3.12	0.0021
Total	31.93	0.0152


25.21020 ns
Signals
Channel 4A
L p-p
R p-p
100 mV
15.625 ps
Results
Measurement
Current
Minimum
Maximum
Count
Jitter[p-p]
19.798 ps
15.004 ps
20.214 ps
502
Jitter[rms]
3.956 ps
3.646 ps
3.994 ps
502

(a)


24.56650 ns
Signals
Channel 4A
50 mV
50 ps

(b)



(c)

Fig. 4-7. Eye-diagrams of (a) PAM-4 input, (b) recovered data, and (c) recovered clock.

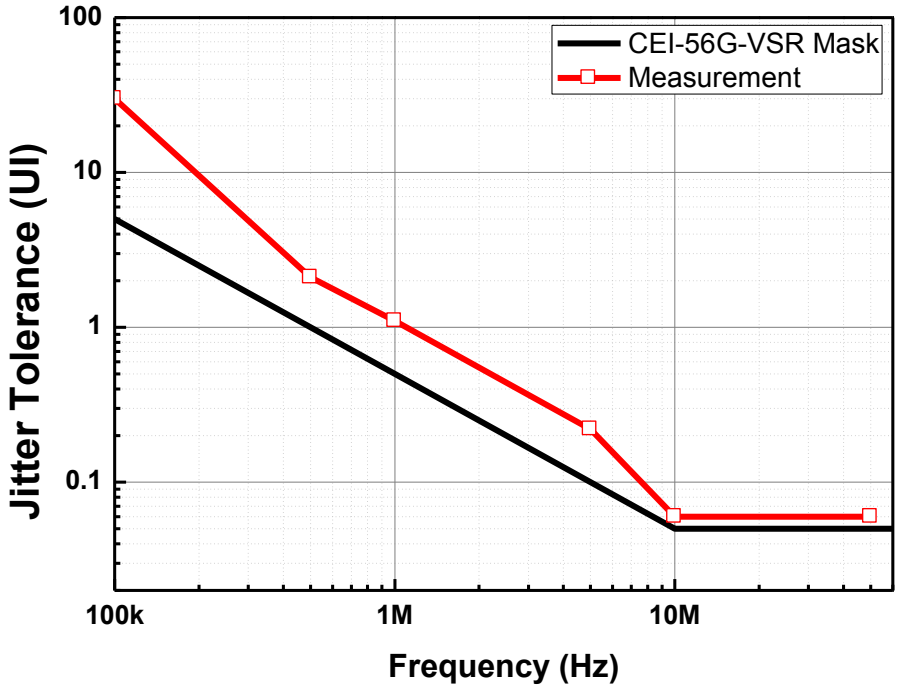


Fig. 4-8. Measured jitter tolerance.

TABLE 4-4

PAM-4 CDR PERFORAMNCE COMPARISON.

	[17]	**[11]**	**This Work**
Data Rate (Gb/s)	22	54.1-56.8	32
Receiver Clock Jitter	J_{rms}= 1.64 ps J_{pkp}= 13.3 ps @ 1.4 GHz	J_{rms}= 0.53 ps J_{pkp} = 2 ps @ 28 GHz	J_{rms}= 3.4 ps J_{pkp}= 26 ps @ 4 GHz
Power consumption (mW)	228*	180**	32**
Power Efficiency (mW/Gbit/s)	10.4	3.2	1
Chip Area (mm^2)	1	1.6	0.0152
Technology	90 nm SOI CMOS	40 nm CMOS	28 nm CMOS

* CDR logic, PRBS checker

** CDR logic only

5. Summary

In this dissertation, we propose a new type of PAM-4 transmitter and receiver, and they enable to decrease power consumption and chip area compared with a conventional transmitter and receiver.

In PAM-4 transmitter, the toggling serializer enables to produce serialized MSB and LSB without the use of high-speed clocks. Multiphase clocks are supplied to the transmitter, and the phase of each clock can be controlled externally for a stable operation. Serialized NRZ signal and transition signals are summed up at the driver without the timing skew by using the SR latch as not only a toggle-to-NRZ converter but also a buffer for transition signals. The newly proposed SST driver maintains the output impedance as 50 Ω, and it enables to control the pre-emphasis gain easily without using bulky sets of resistors. A prototype transmitter realized in 28-nm CMOS technology successfully demonstrates that our transmitter operates properly, and it achieves 1.2 pJ/bit at 40 Gb/s without pre-emphasis, and 1.7 pJ/bit with 2-taps pre-emphasis providing 9.5-dB equalization gain.

In PAM-4 receiver, the new type of PD is used for filtering the middle transitions in PAM-4 signals, which is composed of simple logic gates. By eliminating the middle transitions, the PAM-4 CDR can

be optimized regardless of the variations of input slew-rate which can be caused by the controlling the pre-emphasis gain or the amplitude of signals in the transmitter. In addition, the rotational scheme is also used for decreasing the complexity of design, and it enables to decrease power consumption and chip area. A prototype PAM-4 receiver is realized with 28-nm CMOS technology and clock signal recovery from 32-Gb/s PAM-4 data is successfully demonstrated. The CDR circuit consumes 32 mW with 1.2-V supply and the recovered clock signal has 0.0136-UI rms jitter.

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Abstract (In Korean)

저전력 다중레벨 송신기와 수신기

직렬 데이터 통신의 데이터 속도가 56-Gb/s까지 증가함에 따라, 데이터를 여러 레벨로 나누어 보내는 PAM (Pulse Amplitude Modulation) 기법이 각광받게 되었다. 또한, 이러한 변조 기술은 차세대 표준으로 승인되어, 고속 및 저전력 PAM-4 송수신기를 설계하고 제안하고자 하는 많은 연구가 진행되고 있다.

본 논문에서는 저전력임과 동시에 고속으로 동작하는 새로운 구조의 PAM-4 송신기 및 수신기를 제안한다. PAM-4 송신기는 병렬 데이터로부터 데이터 천이 정보를 뽑아내어, 고속의 클락을 사용하지 않고 간단한 로직 동작으로 구현가능한 NRZ 송신기를 기반으로 제작되었다. 이러한 구조는 직렬화 된 데이터뿐만 아니라 PAM-4의 프리앰퍼시스(Pre-emphasis) 된 PAM-4 신호도 간단하게 만들어 낼 수 있다. 또한 새로운 유형의 SST 드라이버는 다양한 채널 응답에 따라 프리앰퍼시스 이득을 제어 할 수 있습니다. 28-nm CMOS 기술로 구현하였고, 40-Gb/s의 고속 데이터를 생성해 낼 수 있었다. 프리앰퍼시스 기능을 사용하는 경우에는 1.17 pJ/bit 의 에너지 효율을 보였고, 프리앰퍼시스 기능을 사용하지 않는 경우에는 1.68

pJ/bit 의 에너지 효율을 보였다. 총 칩면적은 0.0084 mm^2 이다.

PAM-4 수신기에서는 새로운 구조의 위상 검출기를 제안하였다. 이 위상 검출기는 특정 데이터 천이를 필터링함으로써, 기존의 구조에 비해 데이터 천이 상승/하강 속도에 둔감한 성능을 갖을 수 있었다. 또한, 에지 샘플링 클럭을 주기적으로 회전 시킴으로써, 기존 구조와 비교하여 성능 저하없이 저전력 저면적의 고속 PAM-4 수신기의 설계를 가능하게 하였다. 28nm CMOS 기술로 구현되었고, 32-Gb/s PAM-4 신호를 성공적으로 복원 및 병렬화 하였다. 1.2V 전원으로 32mW를 소비하며 PAM-4 입력 데이터에서 복구 된 클록 신호는 0.0136UI 지터를 갖는다.

핵심 단어: PAM-4 송신기, PAM-4 수신기, 시리얼라이저, SST 드라이버, 뱅뱅 위상 검출기, 클럭 데이터 복원 회로, 고속 직렬 회로, 다중 위상

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