High-Speed Power-Efficient 850-nm Si Optoelectronic Integrated Receivers

Jin-Sung Youn

The Graduate School

Yonsei University

Department of Electrical and Electronic Engineering

High-Speed Power-Efficient 850-nm Si Optoelectronic Integrated Receivers

by

Jin-Sung Youn

A Dissertation

Submitted to the Department of Electrical and Electronic Engineering

and the Graduate School of Yonsei University

in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

February 2014

This certifies that the dissertation of Jin-Sung Youn is approved.

_____

Thesis Supervisor: Woo-Young Choi

_____

Sang-Kook Han

_____

Tae-Wook Kim

_____

Holger Rücker

_____

Sung-Min Park

The Graduate School

Yonsei University

February 2014

Table of Contents

List of Tables

List of Figures

Abstract

High-Speed Power-Efficient 850-nm Si Optoelectronic Integrated Receivers

Jin-Sung Youn

Dept. of Electrical and Electronic Engineering

The Graduate School

Yonsei University

High-speed and power-efficient Si optoelectronic integrated circuit (OEIC) receivers for cost-effective 850-nm short-distance optical interconnect applications are investigated and realized with standard complementary metal-oxide-semiconductor (CMOS) technology and silicon-germanium (SiGe) bipolar CMOS (BiCMOS) technology. In these OEIC receivers, a silicon avalanche photodetector (APD) is monolithically integrated with electronic circuits.

In order to characterize the fabricated APD, DC and photodetection frequency response are measured. In addition, signal-to-noise ratio (SNR) characteristics are investigated to understand its bias-dependent characteristics. With these, an equivalent circuit model of APD including noise current source is developed that can be used in integrated design with electronic circuits.

A high-speed OEIC receiver fabricated with standard 0.13-μm CMOS technology is presented. It is composed of an APD, a transimpedance amplifier (TIA) with a DC-balanced buffer, an equalizer, a limiting amplifier, and an output buffer with 50-Ω loads. With the fabricated OEIC receiver, 10-Gb/s optical data is successfully detected with a bit-error rate (BER) less than 10^{-12} at incident optical power of –4 dBm. The OEIC core has 1 mm × 0.26 mm chip area, and consumes 66.8 mW with 1.2-V supply voltage.

A high-speed OEIC receiver is also realized with standard 0.25-μm SiGe BiCMOS technology. It consists of APD and BiCMOS circuits. Especially, SNR characteristics of the APD and OEIC receiver are investigated to improve OEIC receiver performance. The fabricated OEIC receiver successfully detects 12.5-Gb/s optical data with a BER less than 10^{-12} at incident optical power of –7 dBm. The core chip area and power consumption of the fabricated OEIC receiver are 1 mm ×

0.28 mm and 59 mW with 2.5-V supply voltage, respectively.

A power-efficient OEIC receiver fabricated with standard 65-nm CMOS technology is presented. It is composed of APD and CMOS circuits including an inverter-based TIA, an equalizer, and a post amplifier. To improve power efficiency of OEIC receiver, the TIA is designed in inverter-based configuration with optimal transistor size. In addition, asynchronously under-sampled histogram is included in the OEIC receiver to observe on-chip signal amplitude. With the fabricated CMOS OEIC receiver, 8-Gb/s optical data transmission is successfully demonstrated with a BER less than 10^{-12} at incident optical power of –4.5 dBm. This OEIC receiver achieves power efficiency of 0.63 mW/Gbps.

To the best of my knowledge, the fabricated OEIC receivers achieve the highest data rate with the smallest optical sensitivity as well as the best power efficiency among previously reported 850-nm Si OEIC receivers. It is expected that Si OEIC receivers can provide promising solution for 850-nm short-distance optical interconnect systems.

Keywords: Avalanche photodetectors (APDs), asynchronously under-sampled histogram, bit-error rate (BER), CMOS technology, continuous-time linear equalizer, equivalent circuit model, limiting amplifier, optical interconnect applications, optoelectronic integrated circuits, power efficiency, silicon photonics, SiGe BiCMOS technology, signal-to-noise ratio (SNR), transimpedance amplifier (TIA).

1. Introduction

1-1. Short-Distance Optical Interconnect Applications

The requirement of data transmission rate is continuously increasing in many short-distance interconnect applications such as board-to-board (< 1 m), chip-to-chip (< 10 cm), and intrachip (< 1 cm) interconnects [1]. As an example, the CPUs-memory interface is expected to require 100's GB/s data transmission in the near future [2]. In order to achieve these requirements, various types of parallel optical transceivers have been demonstrated [3]–[5], and each channel data rates are 10, 12.5, and 25 Gb/s, respectively.

However, the existing electrical interconnects face severe performance limitations due to their link distance limitation as well as increasing cross-talk noise, size, and power consumption [6]–[9]. To overcome these problems, fiber-optic techniques are gaining more and more popularity and rapidly expanding its application areas into short-distance interconnect applications and copper-based electrical connectors are being replaced by optical fiber. As shown in Fig. 1-1, the boundary between optical and electrical interconnect applications is gradually moving from left to right [10].

However, there are strong requirements for optical interconnects to be successfully applied to the existing electronic systems. Above all, the required optical devices should be developed in a cost-effective manner. In addition, they should be easily integrated and compatible with the existing electronic system architecture and foundry technology [11]. To fulfill these requirements, there is a great demand for integration of optical devices and electronic circuits on a single silicon substrate. For this, there are active research activities in the area of silicon photonics in which 1.3-μm and 1.5-μm light is usually used [12]–[14]. Fig. 1-2 illustrates a conceptual block diagram of silicon photonics [15]. The ultimate goal of silicon photonics is full integration of various optical devices and electronic circuits on the same silicon substrate as shown in Fig. 1-2.

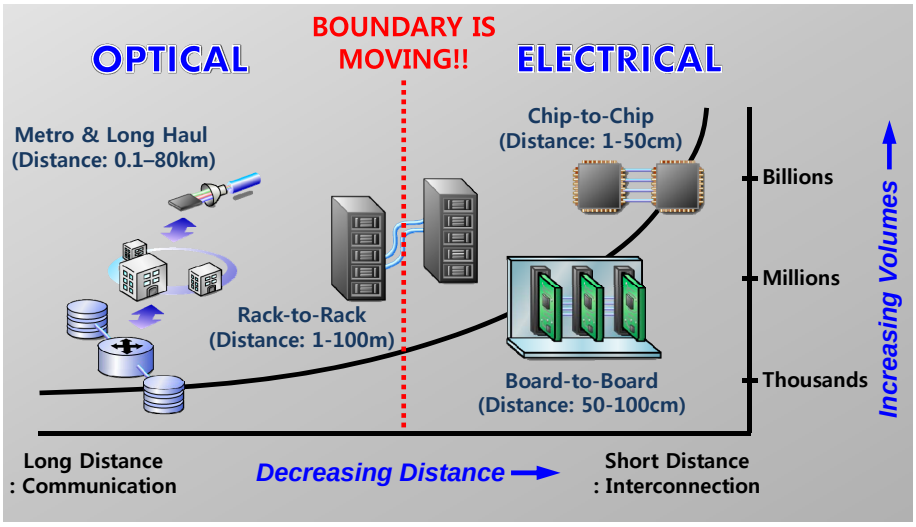


Fig. 1-1. Trends in high-speed optical and electrical interconnects [10].

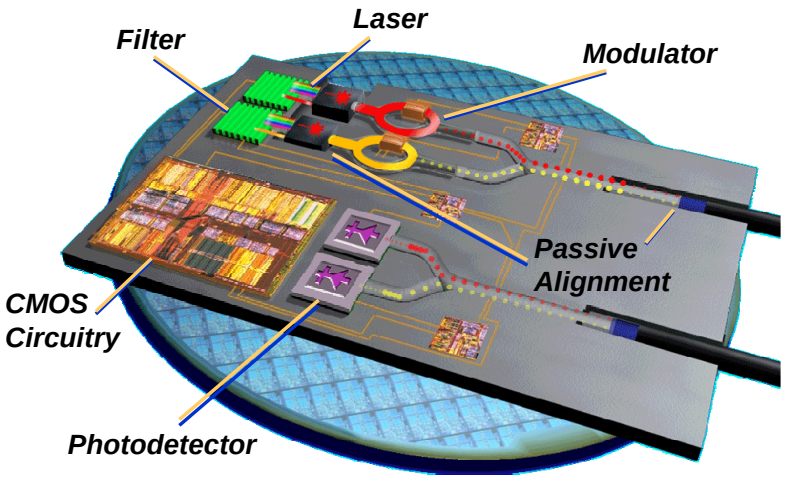


Fig. 1-2. Conceptual block diagram of silicon photonics [15].

1-2. 850-nm Optical Interconnect Systems

Besides 1.3-μm and 1.5-μm applications, there is also strong interest for cost-effective 850-nm optical interconnect systems based on vertical-cavity surface-emitting lasers (VCSELs) and multimode fibers (MMFs) [16]. VCSELs are usually cheaper than edge-emitting lasers, and MMFs with larger core diameter allow more cost-effective packaging solutions. Since 850-nm light can be detected by silicon, there is a strong motivation for realizing 850-nm optoelectronic integrated circuit (OEIC) receivers with silicon technologies such as complementary metal-oxide-semiconductor (CMOS) or bipolar CMOS (BiCMOS) technology. These OEIC receivers can take a full advantage of powerful silicon technology such as low fabrication cost and high volume manufacturability. Furthermore, monolithic integration of silicon photodetectors (PDs) and electronic circuits can provide performance improvement by eliminating undesired parasitic inductance and capacitance due to bonding wires and pads [17], [18].

Fig. 1-3 illustrates a simplified block diagram of an 850-nm optical interconnect systems. The transmitter consists of VCSEL and electronic circuits including serializer, phase-locked loop, and driver circuits with pre-emphasis. The receiver is composed of PD and electronic circuits

including amplifiers, equalizer, de-serializer, and clock and data recovery circuit. Table 1-1 shows I/O link budget for 850-nm optical interconnect systems [9]. The estimated total link loss is about −6.8 dB from the transmitter to the receiver owing to coupling loss, extinction ratio penalty, and link margin. With the VCSEL having average output power of 3 dBm, the required receiver sensitivity is about −3.8 dBm.

In addition, power efficiency is also key design issue in optical interconnect systems, and it should be optimized to have advantage compared with the existing electrical interconnect systems. The suggested value for overall transceiver is about 1 pJ/bit (= 1 mW/Gbps), and it is expected that the receiver will be occupied 40 % among total power efficiency [8], [9].

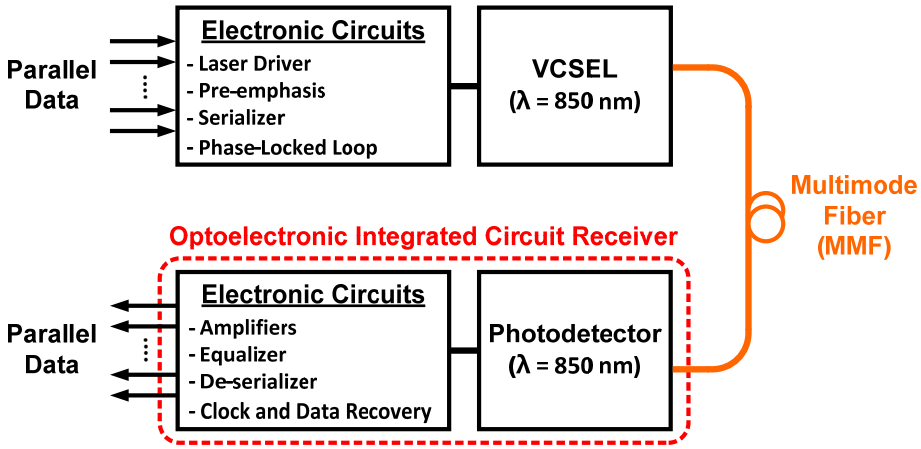


Fig. 1-3. Block diagram of 850-nm optical interconnect systems.

Table 1-1
Optical I/O Link Budget [9]

Avg. VCSEL Tx Power		**3.0 dBm**
Link Budget (−6.8 dB)	VCSEL to MMF Coupling	−1.1 dB
	MMF to PD Coupling	−1.1 dB
	Extinction Ratio (7.3 dB) Penalty	−1.6 dB
	Margin	−3.0 dB
Required Rx Sensitivity		**−3.8 dBm**

However, one big challenge for high-performance OEIC receivers with silicon technology is realization of good PDs because silicon PDs suffer from low detection efficiency and gain-bandwidth product due to low absorption coefficient of silicon and the narrow depletion regions. Moreover, their detection bandwidth can be limited by slow diffusion of photo-generated carriers in the charge neutral region [19]. These problems can be mitigated by using a low-doped epitaxial layer [20] or silicon-on-insulator substrate [21]. However, these approaches require significant process modification, which increases fabrication cost and decreases process yields. To improve PD performance while maintaining advantages of silicon technology, various types of 850-nm silicon PDs have been investigated in standard silicon technology without any process modification.

1-3. 850-nm Photodetectors in Standard Si Technology

Fig. 1-4(a) shows a PD using N-well/P-substrate junction [22], [23]. This junction can provide wider depletion regions, and consequently, better detection efficiency can be achieved than any other PN junctions available in standard silicon technology. However, this type of PD has limited photodetection bandwidth in the MHz range since many photons are absorbed in the region where photo-generated carriers experience slow diffusive transport. Therefore, equalizer circuits having high-pass filter characteristics are essential for multi-gigabit data transmission. In [22], Radovanović *et al*. achieved a 3-Gb/s OEIC receiver with on-chip PD using N-well/P-substrate junction including electronic equalizer circuits. However, it is still strongly desired to achieve as large intrinsic PD bandwidth as possible because equalizer circuits can be complex, and photodetection bandwidth can be further enhanced by additional equalizer circuits.

To further improve photodetection bandwidth, spatially-modulated light (SML) PDs based on N-well/P-substrate junction have been investigated [24]–[30]. As shown in Fig. 1-4(b), it is composed of uncovered and covered regions with a light-blocking metal. These SML PDs have the enhanced photodetection bandwidth by eliminating slow

diffusion currents with differential operation [24]. In [29], Lee *et al*. reported an 8.5-Gb/s OEIC receiver with on-chip SML PD including an equalizer circuit. In [30], Huang *et al*. achieved a 10-Gb/s OEIC receiver with a meshed SML PD as well as high-speed circuits with on-chip passive inductors. Although SML PDs achieve speed enhancement, their responsivity is relatively low due to large optical loss from the light-blocked area.

Another approach is a lateral PIN PD realized by a P^+/P-substrate/N^+ interleaved structure as shown in Fig. 1-4(c) [31]. The active region is surrounded by N-well and deep N-well regions, and photo-generated carriers created in lateral depletion regions contribute to photocurrents. With PIN PD, Chen *et al*. achieved a 2.5-Gb/s OEIC receiver without any equalizer circuits. The PIN PD has larger photodetection bandwidth of about 1.9 GHz, but it has drawbacks of relatively low responsivity.

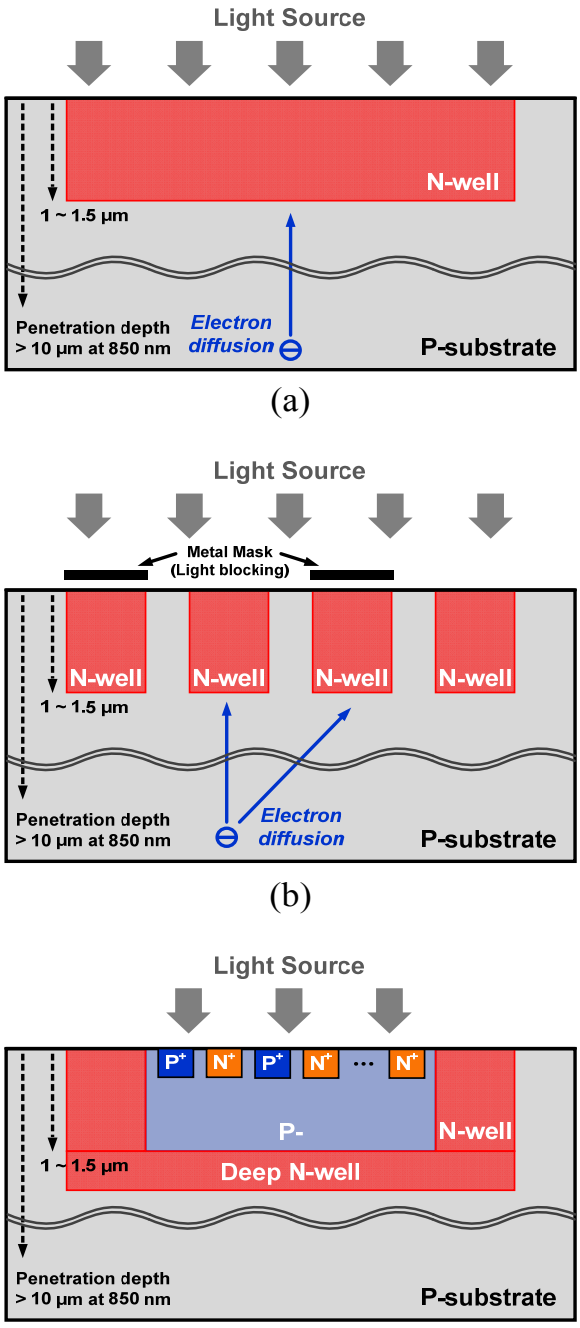


Fig. 1-4. Cross sections of silicon PDs: (a) N-well/P-substrate, (b) spatially-modulated light, and (c) lateral PIN.

In this dissertation, a different approach has been pursued to improve silicon PD performance. Instead of N-well/P-substrate junction, P^+/N-well junction is used to exclude the slow diffusion currents from P-substrate region. However, the PD having P^+/N-well junction suffers from reduced responsivity since the volume for photodetection is small. This problem can be solved by using avalanche gain, and consequently, the silicon avalanche PD (APD) based on P^+/N-well junction has large photodetection bandwidth of several GHz as well as high detection efficiency [32]. Using the APD, monolithically integrated OEIC receivers have been developed [33]–[35]. Further details on the APD and OEIC receivers will be discussed in the following chapters.

1-4. Outline of Dissertation

This dissertation will be dedicated to realization of high-performance 850-nm OEIC receivers with standard CMOS/BiCMOS technology and demonstration of high-speed 850-nm optical data transmission utilizing them. The remainder of this dissertation is organized as follows.

Chapter 2 illustrates structure and characteristics of the fabricated silicon APD. Section 2-2 shows current-voltage and photodetection frequency response characteristics. In addition, signal-to-noise ratio (SNR) characteristics are presented in Section 2-3. An equivalent circuit model of APD including noise current source is presented in Section 2-4.

Chapter 3 shows a high-speed 850-nm OEIC receiver fabricated with standard CMOS technology. In section 3-2, circuit implementation is described. Section 3-3 shows measurement results and demonstration of 10-Gb/s optical data transmission using the fabricated CMOS OEIC receiver.

Chapter 4 presents a high-speed 850-nm OEIC receivers fabricated with standard silicon-germanium (SiGe) BiCMOS technology. Section 4-3 and 4-4 explain SNR characteristic and circuit implementation of the OEIC receiver, respectively. Measurement results and

demonstration of 12.5-Gb/s optical data transmission using the fabricated SiGe BiCMOS OEIC receiver are presented in section 4-5. In section 4-6, SNR characteristics of OEIC receiver is verified with bit-error rate (BER) measurements.

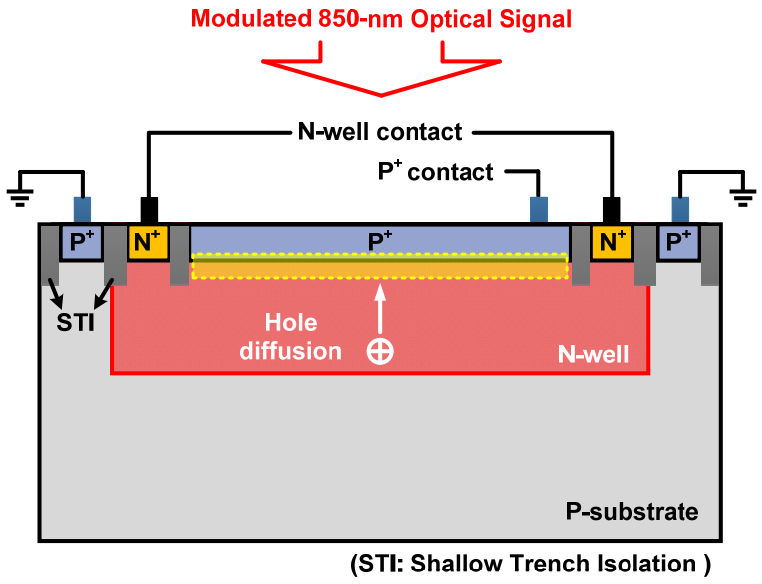
Chapter 5 shows a power-efficient 850-nm OEIC receiver fabricated with standard CMOS technology. In section 5-3, circuit implementation is described. Section 5-4 shows measurement results and demonstration of 8-Gb/s optical data transmission using the fabricated CMOS OEIC receiver.

Finally, this dissertation will be summarized with conclusions and discussions in chapter 6.

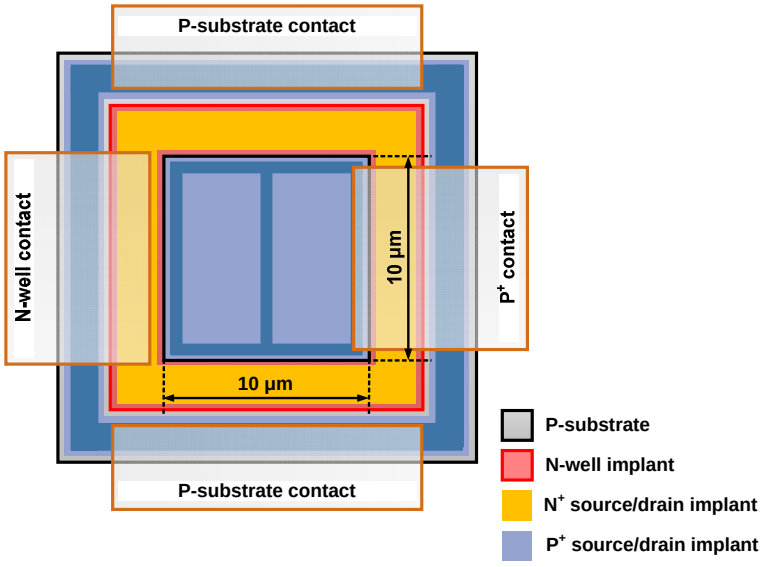
2. APD in Standard Si Technology

2-1. Device Description

Fig. 2-1 shows the simplified cross-sectional and top views of the silicon APD which can be fabricated with standard CMOS/BiCMOS technology without any design and layout rule violation. The APD is formed by a vertical P^+ source/drain and N-well junction [32]. The P^+/N-well junction can exclude the slow diffusion currents from P-substrate region, and most of photogenerated carriers can swiftly reach to electrodes through much thinner N-well region. The vertical PN junction is surrounded by shallow trench isolation in order to achieve large and uniform electric fields at the junction without premature edge breakdown [36]. The active area for the optical window is about 10 μm × 10 μm. The photogenerated currents are extracted from P^+ contacts and delivered to the following circuits. The positive voltage is applied to the N-well contacts, and P-substrate is grounded. As shown in Fig. 2-1(a), optical signal is injected into the APD by using vertical coupling. It can provide lower fabrication and packaging cost than edge coupling which requires additional processing step and tight optical coupling due to narrow depletion width of the fabricated APD.



(a)



(b)

Fig. 2-1. (a) Cross-sectional and (b) top views of APD.

2-2. DC and AC Characteristics

Fig. 2-2 shows experimental setups for APD characterization. An 850-nm laser diode and an external electro-optic modulator are used to generate the modulated optical signals. These signals are transmitted through MMF and injected into the APD using a lensed fiber with 10-μm spot diameter. A power monitor-attenuator is used to control the incident optical power. A semiconductor parameter analyzer is used to measure current-voltage characteristics, and an S-parameter vector network analyzer is used to measure photodetection frequency response with cables and RF connector calibration. All measurements are done on-wafer probing at room temperature.

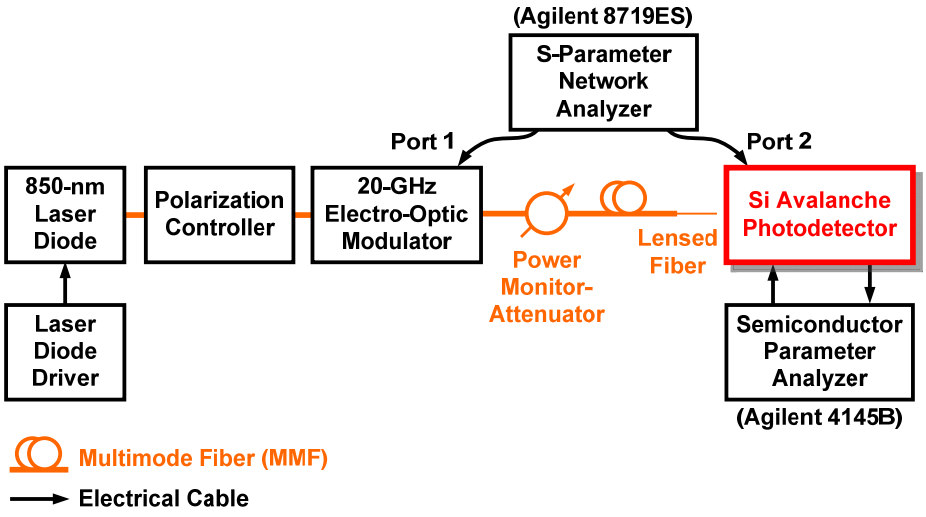


Fig. 2-2. Experimental setups for APD characterization.

2-2-1. Current-Voltage (I-V) Characteristics

Fig. 2-3(a) shows the measured current-voltage characteristics of the fabricated APD as a function of reverse bias voltage (V_R) under dark and optical illumination conditions. The incident optical power (P_{opt}) is −10 dBm (= 0.1 mW). The dark current remains less than a few nanoamperes at V_R below 12.3 V. However, dark current dramatically increases at the breakdown voltage (V_{bk}) of about 12.4 V because of avalanche multiplication process. Under optical illumination, the photogenerated current also increases with internal gain provided by avalanche multiplication process.

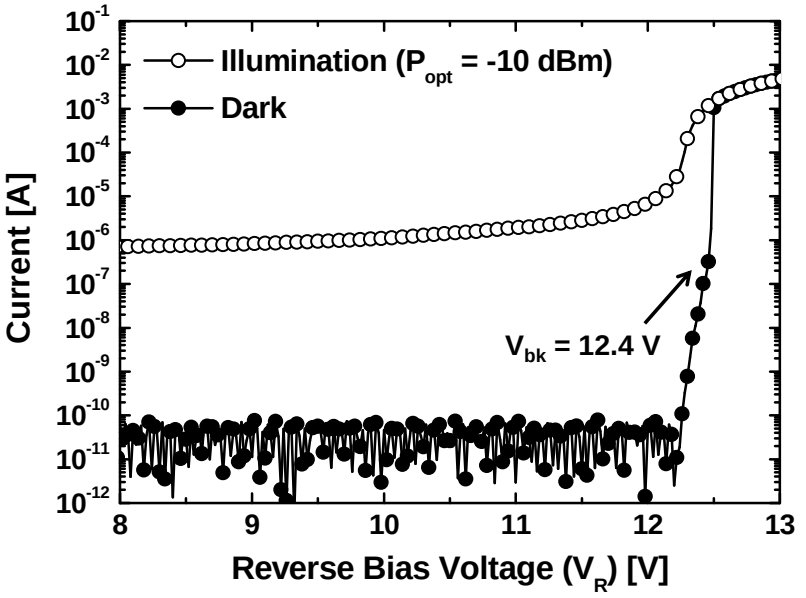
With the measured current-voltage characteristics, photocurrent (I_{ph}), responsivity (R), and avalanche multiplication factor (M) (= avalanche gain) of the fabricated APD can be determined with the following equations [37]:

$$I_{ph} = I_{illumination} - I_{dark} \ [\mathrm{A}] \tag{2.1}$$

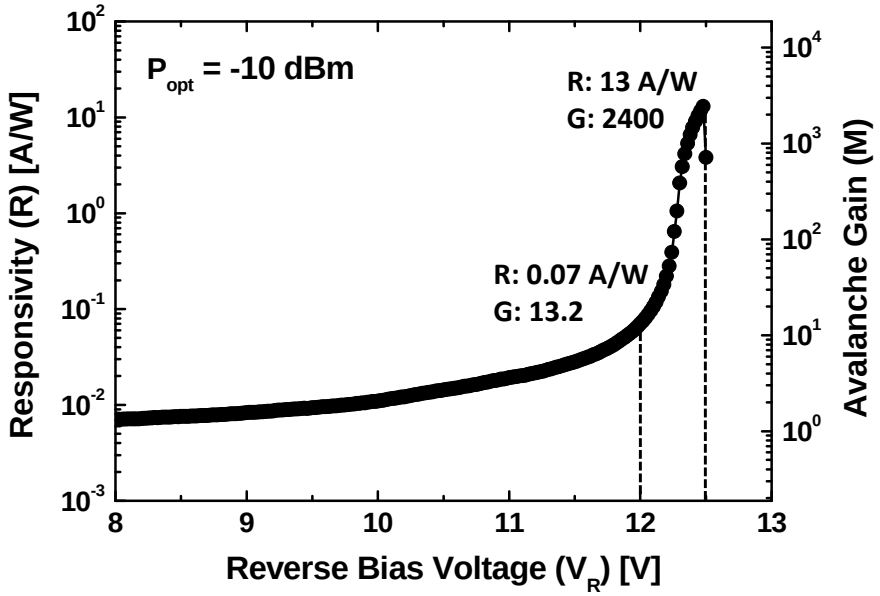
$$R = \frac{I_{ph}}{P_{opt}} \ [\mathrm{A/W}] \tag{2.2}$$

$$M(V) = \frac{I_{ph}(V)}{I_{ph}(V_0)} = \frac{I_{illumination}(V) - I_{dark}(V)}{I_{illumination}(V_0) - I_{dark}(V_0)} \tag{2.3}$$

where $I_{illumination}$ and I_{dark} represent the photogenerated current under optical illumination and the dark current, respectively. V_0 is the reference voltage at which no avalanche gain is observed. For the investigation, we used V_0 of 1 V. Fig. 2-3(b) shows the calculated responsivity and avalanche gain of the fabricated APD. The maximum responsivity and avalanche gain of the APD are about 13 A/W and 2400, respectively. The optimal V_R for the best BER performance of OEIC receiver is about 12.0 V, the reason will be discussed in chapter 4. At this V_R point, responsivity and avalanche gain are about 70 mA/W and 13.2, respectively.



(a)



(b)

Fig. 2-3. (a) Current-voltage characteristics and (b) DC responsivity and avalanche gain of the fabricated APD. Incident optical power (P_{opt}) is −10 dBm.

2-2-2. Photodetection Frequency Response

Fig. 2-4 shows the measured photodetection frequency responses of the fabricated APD with different reverse bias voltages of from 10.5 V to 12.0 V in steps of 0.5 V at P_{opt} of −10 dBm. With increasing V_R, the measured photodetection response magnitude is enhanced due to the increased avalanche gain. The 3-dB photodetection bandwidth is nearly the same to 5 GHz for V_R range from 10.5 V to 12.0 V.

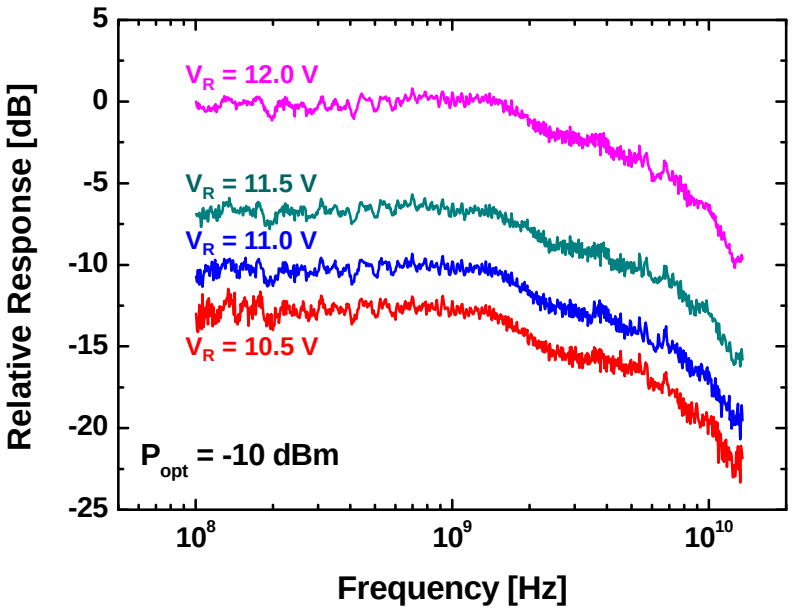


Fig. 2-4. Measured photodetection frequency responses of the fabricated APD with different reverse bias voltages (V_R).

2-3. Signal-to-Noise Ratio (SNR) Characteristics

It is an important task to investigate SNR characteristics of APD because APD provides much enhanced noises as well as signals. Fig. 2-5 shows the experimental setup for measuring APD signal and noise characteristics. For signal measurement, 850-nm light from a laser diode is modulated at 1 GHz by an external electro-optic modulator. 1-GHz modulation frequency is used because APD has flat frequency response at this frequency region, and the measurement does not suffer from electrical cable loss. The 850-nm modulated light is transmitted through MMF, and injected into the APD using a lensed fiber, and the APD output signal is measured using a spectrum analyzer having 50-Ω load.

For noise measurement, the noise power spectral density at 1 GHz is measured using the spectrum analyzer with un-modulated light. Since the resulting noise level is less than the sensitivity of the spectrum analyzer, APD output signal is amplified with a commercial low-noise amplifier (LNA) having 26-dB gain and 3-dB noise figure at 1 GHz. APD noise power spectral density is determined by calibrating these results with LNA gain and noise figure. Since dominant APD noises are thermal and shot noises, which are white noises [38], the total APD noise power can be obtained by multiplying the above results at 1 GHz

with an equivalent noise bandwidth of the APD. The noise bandwidth is equal to the 1.55 times the signal bandwidth. Then, the measured APD signal and noise power are converted into peak-to-peak signal current and root mean square (rms) noise current, respectively. For this, the influence of APD output impedance can be ignored since it is much larger than 50-Ω load provided by the spectrum analyzer.

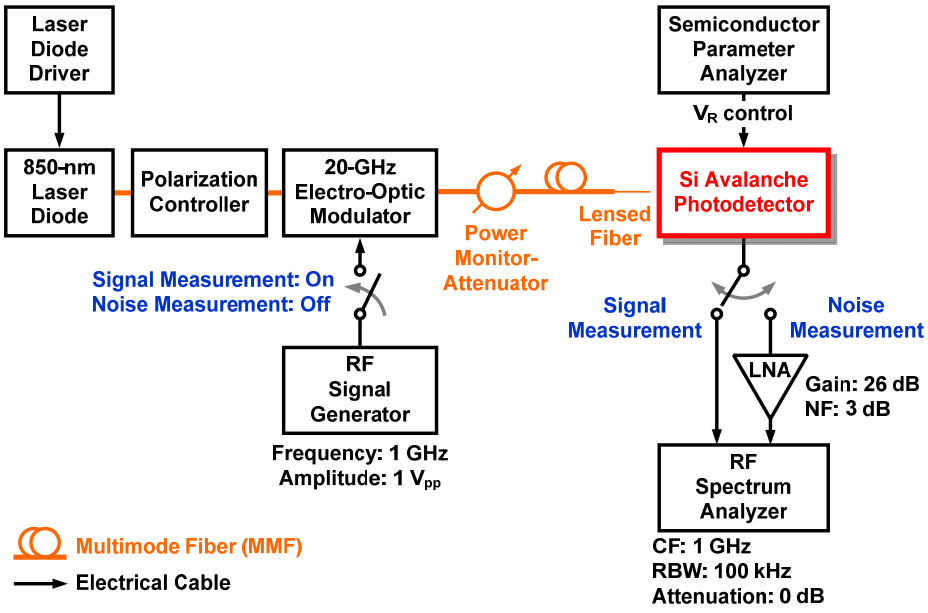
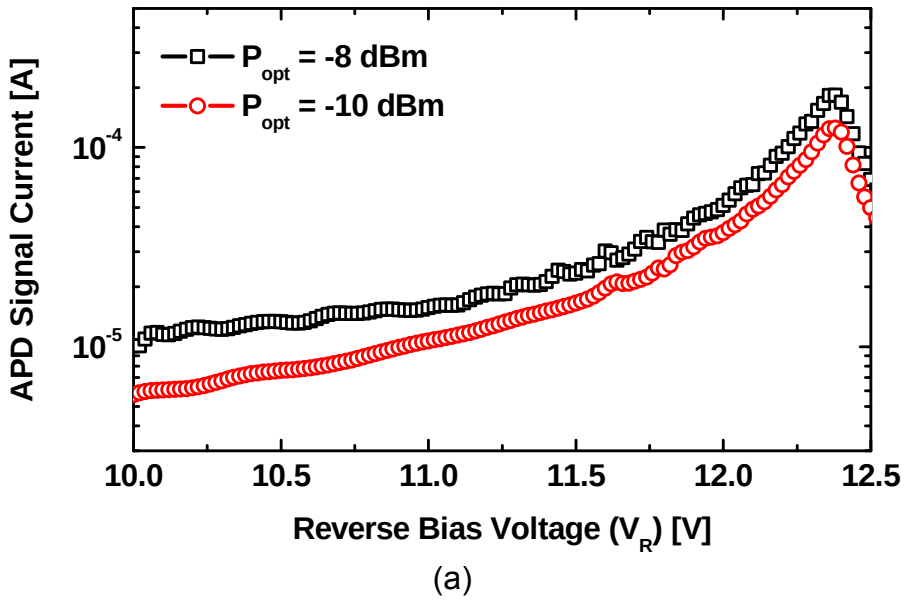
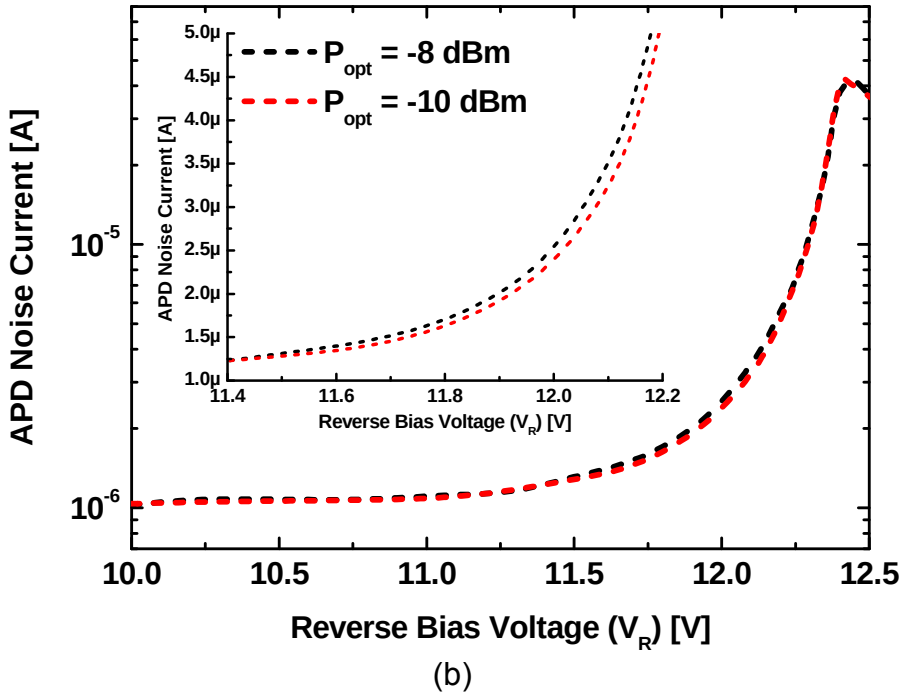


Fig. 2-5. Experimental setups for APD signal and noise measurements.

Fig. 2-6(a) and (b) show the measured APD signal and noise characteristics as a function of V_R, respectively. The measurement is done with two different optical powers of −8 and −10 dBm. With increasing V_R, the APD signal current increases due to avalanche gain, reaching the maximum at V_R of about 12.4 V as shown in Fig. 2-6(a). As expected, APD signal current is larger for larger P_{opt}. The APD noise current also increases with increasing V_R because of increasing avalanche noise. The APD noise current is slightly larger for larger P_{opt} as shown in the inset of Fig. 2-6(b). Both noise currents are nearly the same for V_R below about 11.5 V since the thermal noise is dominant for APD in the range. With increasing V_R, the shot noise is more pronounced, and consequently, larger P_{opt} produces larger noise current.



(a)



(b)

Fig. 2-6. Measured (a) signal and (b) noise characteristics of the fabricated APD as a function of reverse bias voltage (V_R). Incident optical power (P_{opt}) is −8 and −10 dBm.

With the measured APD signal and noise characteristics, APD SNR (SNR_{APD}) can be calculated as the following equation:

$$\mathrm{SNR}_{\mathrm{APD}}(\mathrm{V_R}) = \frac{I_{\mathrm{s,pp,APD}}(\mathrm{V_R})}{\sqrt{\overline{I^2_{\mathrm{n,rms,APD}}}(\mathrm{V_R})}} \tag{2.4}$$

where $I_{\mathrm{s,pp,APD}}$ and $I_{\mathrm{n,rms,APD}}$ represent peak-to-peak signal current and rms noise current of APD, respectively, both of which depend on V_R. Fig. 2-7 shows the calculated SNR_{APD} as a function of V_R at P_{opt} of −8 and −10 dBm, respectively. The SNR_{APD} is the highest for V_R of about 11.9 V, which is less than V_R of 12.4 V that gives the maximum APD signal current shown in Fig. 2-6(a). For V_R below 11.9 V, the SNR_{APD} is degraded because APD does not have sufficient avalanche gain. For V_R above 11.9 V, the SNR_{APD} is dramatically degraded due to too much avalanche noises.

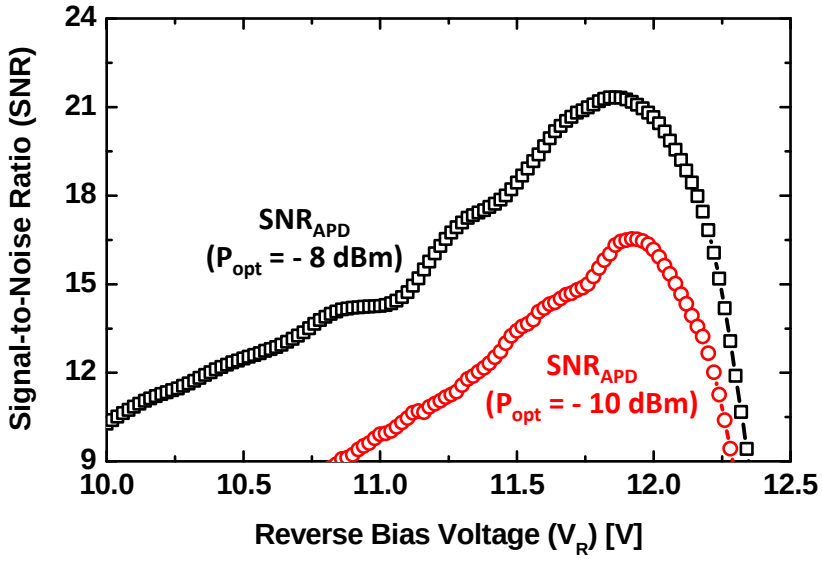


Fig. 2-7. Calculated SNR_{APD} as a function of reverse bias voltage (V_R). Incident optical power (P_{opt}) is −8 and −10 dBm.

2-4. Equivalent Circuit Model

Fig. 2-8 shows a simplified APD equivalent circuit model which is composed of parasitic components and signal (i_{ph}) and noise (i_n) current sources. A first-order RC low-pass filter is used to include the transit time effect of the photogenerated carriers. In Fig. 2-8, R_j and C_j represent junction resistance and capacitance in the P^+/N-well depletion region. R_s and C_p represent parasitic resistance in N-well region and capacitance between P^+ and N-well electrodes, respectively. The model parameters are extracted from the measured two-port S-parameter

characteristics. The extracted model parameters and values are listed in Table. 2-1. The further details for parameter extraction process and equivalent circuit model can be found in [39].

For C_j, the value can be easily derived using $C_j = \varepsilon_s A / W_D$ where ε_s is the semiconductor permittivity, A is the cross-sectional area, and W_D is the depletion width. In the APD, P^+/N-well depletion width is about 0.3 μm, and therefore, the estimated junction capacitance is about 35 fF which is well matched with the extracted value. Fig. 2-9 shows the measured photodetection frequency response at V_R of 12.0 V as well as the simulation result using the equivalent circuit model. As shown in Fig. 2-9, measured and simulated results are well matched.

The circuit model is further established by adding APD noise current source as shown in Fig. 2-8. The APD noise characteristic can be modeled as Gaussian distribution in the case of silicon APD having small excess noise factors [38]. Fig. 2-10 shows the simulated 6-Gb/s eye diagrams and power spectra of APD output currents at different reverse bias voltages. This simulation is done with Spectre circuit simulator in Cadence, and the APD noise current is added using Verilog-A. As shown in Fig. 2-10, signal amplitude and magnitude are increased with the increasing V_R. However, both eye diagram and power spectrum are degraded due to the increased avalanche noise.

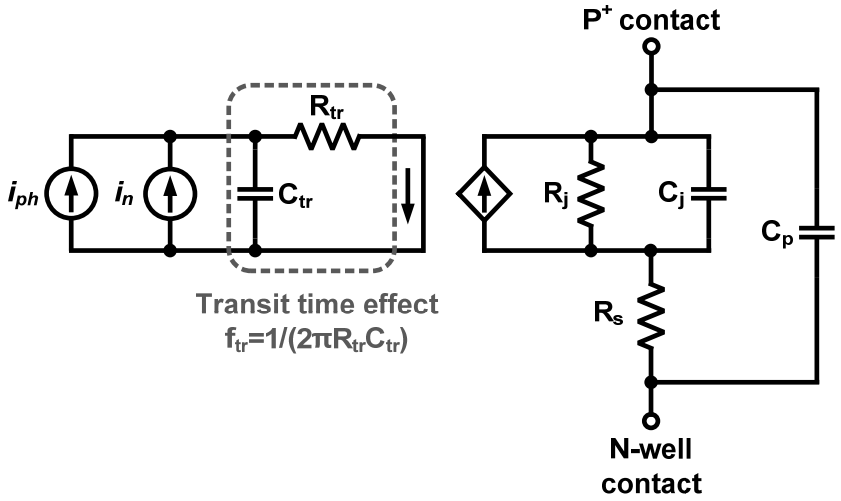


Fig. 2-8. Equivalent circuit model of APD including transit time effect and noise current source.

Table 2-1
Extracted model parameters of APD

Junction resistance (R_j)	70 kΩ
Junction capacitance (C_j)	35 fF
Series resistance (R_s)	72 Ω
Parasitic capacitance (C_p)	13 fF
Transit time bandwidth (f_{tr})	5 GHz

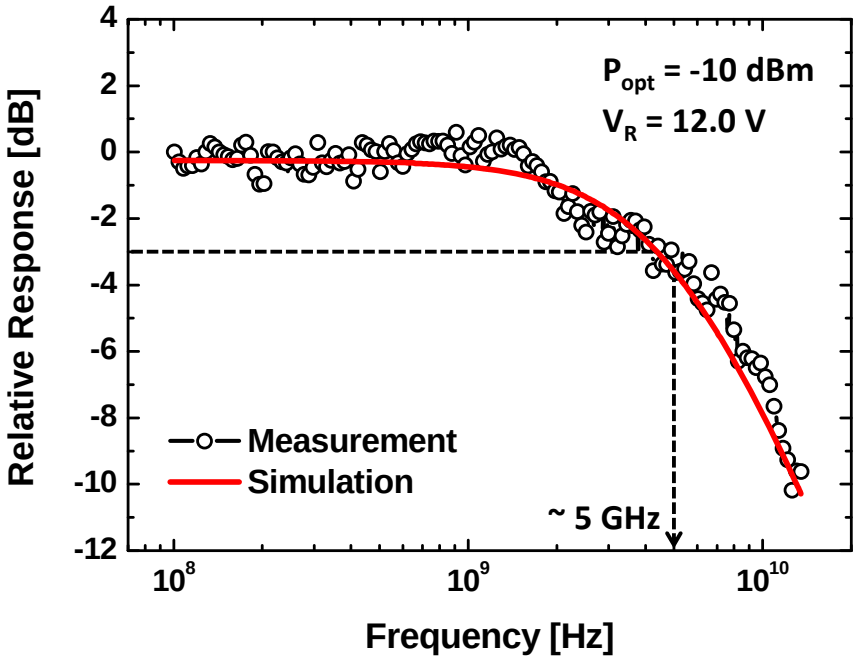


Fig. 2-9. Measured and simulated photodetection frequency responses of APD at V_R of 12.0 V.

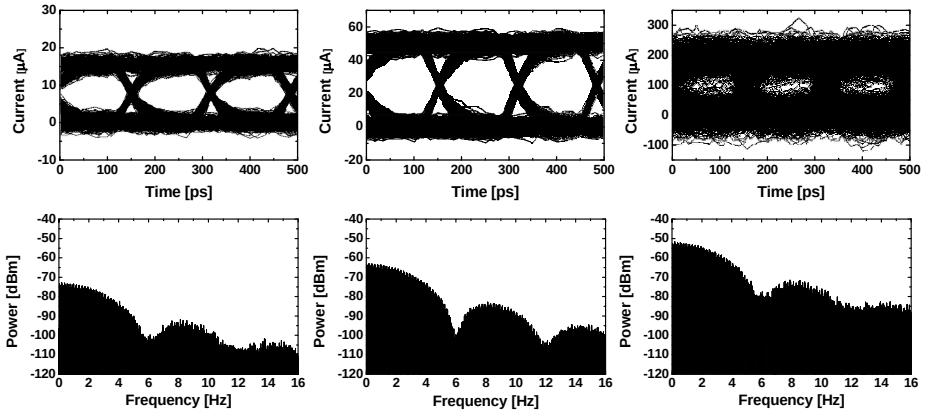


Fig. 2-10. Simulated 6-Gb/s eye diagrams and power spectra of the APD output currents at different reverse bias voltages of (a) 11.0 V, (b) 12.0 V, and (c) 12.4 V, respectively.

2-5. Summary

An APD fabricated with standard silicon technology is investigated. It is realized by a vertical P^+/N-well junction surrounded by shallow trench isolation. The APD has active area of about 10 μm × 10 μm. Firstly, DC and photodetection frequency response characteristics are measured. The fabricated APD provides high responsivity as well as large photodetection bandwidth. Then, SNR characteristics are measured and investigated. Finally, an APD equivalent circuit model including noise current source is developed. It is expected that SNR characteristics and equivalent circuit model of the APD are very useful for OEIC receiver design because they allow circuit design optimization as well as precise design estimation of OEIC receiver bandwidth.

3. High-Speed 850-nm CMOS OEIC Receiver

3-1. Overall Structure

Fig. 3-1 shows a simplified block diagram of the proposed 850-nm OEIC receiver fabricated with standard 0.13-μm CMOS technology. The OEIC receiver consists of APD with dummy PD, transimpedance amplifier (TIA) with DC-balanced buffer, tunable equalizer, limiting amplifier, and output buffer with 50-Ω loads. The APD is implemented P^+/N-well junction surrounded by shallow trench isolation. The optical window is about 10 μm x 10 μm. The dummy PD is used for achieving input symmetry of the differential TIA. The TIA is designed in shunt-feedback configuration, and the DC-balanced buffer is used for fully differential signaling. The equalizer compensates bandwidth limitation due to the APD and TIA, and its high-frequency boosting gain is tuned with a capacitor array. The limiting amplifier is composed of five-stage amplifier having active feedback and/or negative capacitance. The output buffer is used for driving 50-Ω loads. The following chapters concentrate on illustrating the design procedures of the receiver circuits such as TIA, equalizer, and limiting amplifier, and finally, measurement results will be presented.

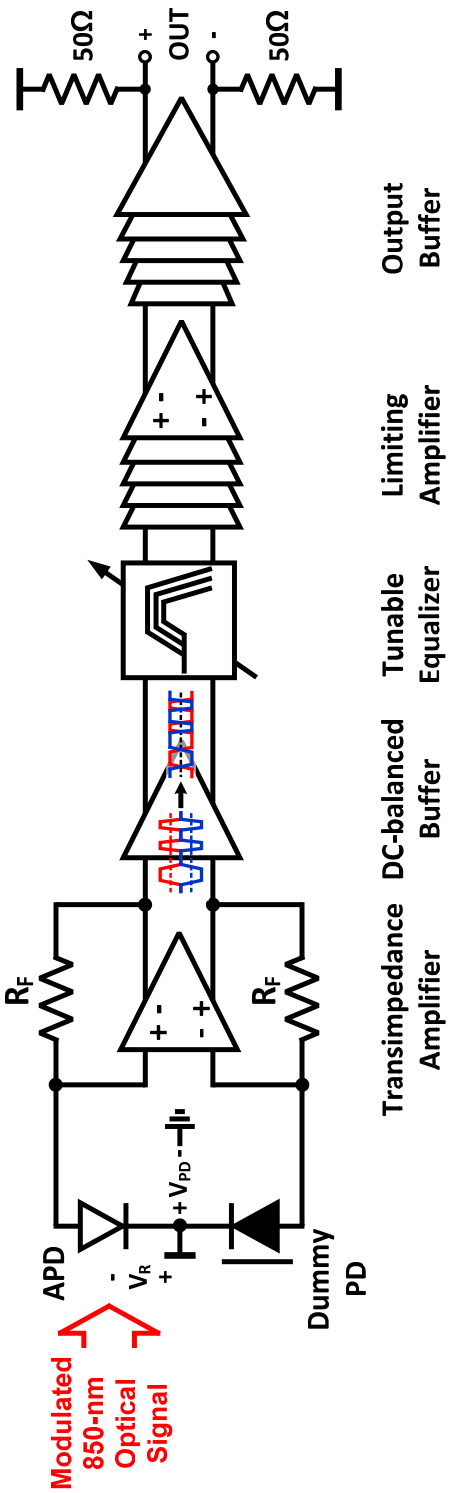


Fig. 3-1. Block diagram of the fabricated CMOS OEIC receiver.

3-2. Circuit Implementation

3-2-1. Transimpedance Amplifier

The photodetector produces a small photocurrent signal proportional to optical signal. The current signal should be converted to the voltage signal with amplification to be handled by the subsequent circuits. For this, some components and/or circuits are needed, and they should be carefully designed because the entire receiver performance is mainly determined by them. The simplest way to convert from current signal to voltage signal is using a resistive load in open-loop configuration as shown in Fig. 3-2(a). With the resistive load (R_L), conversion gain, 3-dB bandwidth, and input-referred noise current can be determined as:

$$\text{Conversion gain} \simeq R_L, \tag{3.1}$$

$$\text{3-dB bandwidth} \simeq \frac{1}{2\pi R_L C_{PD}}, \tag{3.2}$$

$$\text{Input-referred noise current} \simeq \frac{4kT}{R_L} \text{ (neglecting } C_{PD}\text{)}, \tag{3.3}$$

where k and T represent Boltzmann constant and absolute temperature, respectively. C_{PD} represents PD junction capacitance. If R_L is small (~

50 Ω, low impedance), wide dynamic range and large bandwidth can be achieved. However, it has drawbacks of small output voltage signal as well as poor noise performance due to the small R_L. On the other hands, if R_L is high (~ a few kΩ, high impedance), large output voltage signal and good noise performance can be achieved. However, their speed can be limited.

In order to mitigate these trade-offs, a transimpedance configuration is introduced as shown in Fig. 3-2(b). It consists of a voltage amplifier and a resistor in negative-feedback configuration. For transimpedance configuration, conversion gain, 3-dB bandwidth, and input-referred noise current can be determined as:

$$\text{Conversion gain} \simeq -\frac{A}{A+1}\cdot R_F, \tag{3.4}$$

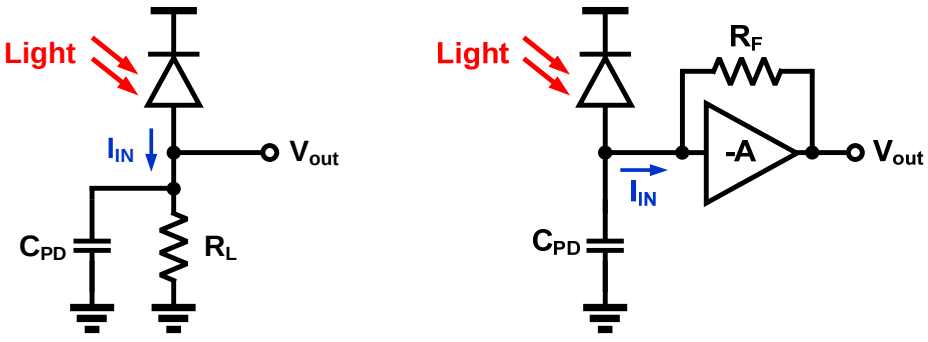
$$\text{3-dB bandwidth} \simeq \frac{A}{2\pi R_F C_D}, \tag{3.5}$$

$$\text{Input-referred noise current} \simeq \frac{4kT}{R_F} + \frac{\overline{V_{n,amp}^2}}{R_F^2} \text{ (neglecting } C_{PD}\text{)}, \tag{3.6}$$

where A and $V_{n,amp}$ represent gain and noise of the voltage amplifier. C_D represents parasitic capacitance due to input transistor of TIA and PD. With large A, transimpedance configuration can achieve large output voltage signal, wide bandwidth, and as well as good noise performance

simultaneously. For this reason, the transimpedance configuration is the most popular for achieving current-to-voltage conversion.

Table 3-1 summarizes trade-offs of low- and high-impedance, and transimpedance configurations [40].



(a) (b)

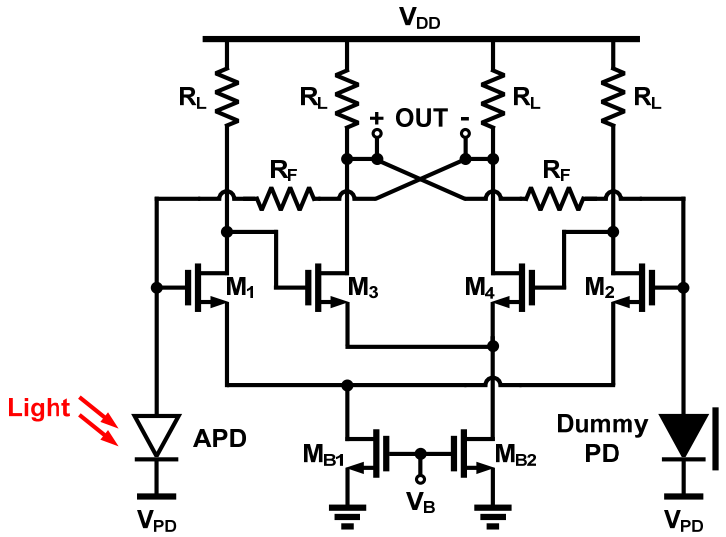
Fig. 3-2. (a) Open-loop and (b) negative-feedback configuration.

Table 3-1
Current-to-voltage conversion topologies [40].

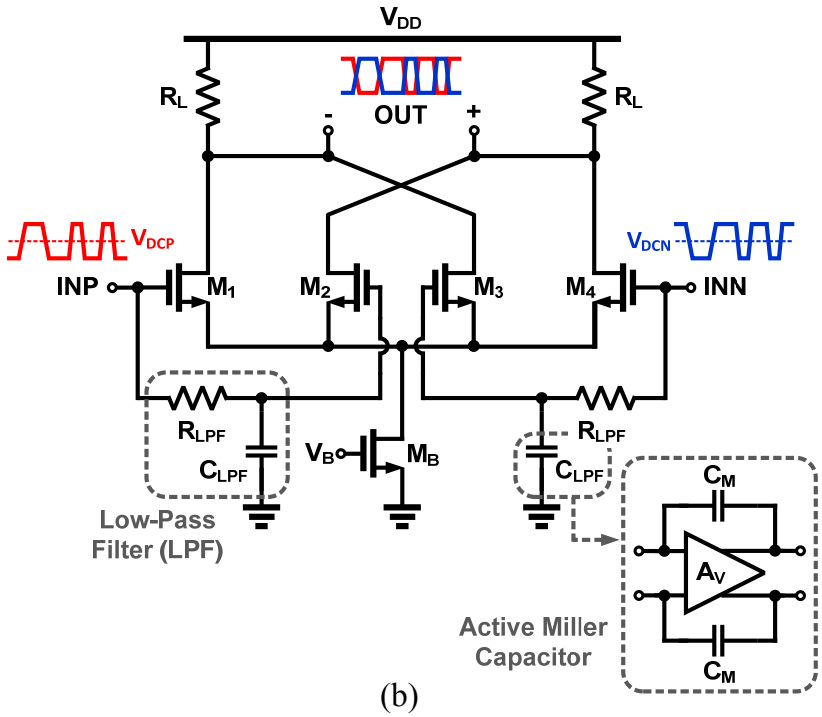
LOW-IMPEDANCE	HIGH-IMPEDANCE	TRANSIMPEDANCE
High bandwidth	Small bandwidth	High bandwidth
Low sensitivity	High sensitivity	High sensitivity (Dependent on R_F)
High noise	Low noise	Medium noise

In this work, shunt-feedback TIA configuration is used for current-to-voltage conversion as shown in Fig. 3-3(a). It is composed of two-stage voltage amplifier and feedback resistance (R_F) of 4 kΩ. In order to connect PD and TIA without any speed degradation, TIA having low input impedance is desired because PD junction capacitance can generate a dominant pole at the low frequency in frequency response. Fortunately, relatively high input impedance can be allowed in this case because the APD has relatively small junction capacitance of about 35 fF. As a result, the TIA can achieve low-noise characteristics [41] as well as high-speed operation while maintaining high transimpedance gain without using any passive inductors [42] or such input stage as common-gate [43] or regulated cascade [44], [45].

Because the optical signal is detected by single APD, differential TIA does not produce completely differential output signals. To solve these problems, a DC-balanced buffer is used as shown in Fig. 3-3(b). It is composed of f_T-doubler amplifier and low-pass filters. With this circuit, fully-differential signals can be achieved at the buffer output. The chip area of the capacitor in the low-pass filter can be shrunk by using an active Miller capacitor [46]. The values for R_{LPF}, C_M, and A_V used in this design are 20 kΩ, 2.4 pF, and 2.5, respectively. The resulting low cut-off frequency is about 1 MHz.



(a)



(b)

Fig. 3-3. Schematic diagrams of (a) transimpedance amplifier and (b) DC-balanced buffer with active Miller capacitor.

3-2-2. Equalizer

Continuous-time linear equalizer circuits having high-pass filter characteristics are widely used to compensate high-frequency loss and enhance bandwidth. In this work, an equalizer circuit is also used to compensate bandwidth limitation due to the APD and TIA. The equalizer circuit is composed of five-stage of an identical filter, and the individual filter is designed in a differential structure with capacitive degeneration [47] and negative capacitance [48] as shown in Fig. 3-4. The frequency response of the filter can be estimated by pole-zero analysis. The transfer function of the filter with capacitive degeneration can be derived as:

$$H(s) \cong \frac{g_m R_{\mathrm{L}}}{1+\frac{g_{\mathrm{m}} R_{\mathrm{S}}}{2}} \cdot \frac{1+\frac{s}{\omega_{\mathrm{z1}}}}{\left(1+\frac{s}{\omega_{\mathrm{p1}}}\right)\cdot\left(1+\frac{s}{\omega_{\mathrm{p2}}}\right)}, \tag{3.7}$$

where $\omega_{\mathrm{z1}} = 1/(R_{\mathrm{S}}C_{\mathrm{S}})$, $\omega_{\mathrm{p1}} = (1+g_{\mathrm{m}}R_{\mathrm{S}}/2)/R_{\mathrm{S}}C_{\mathrm{S}}$, $\omega_{\mathrm{p2}} = 1/(R_{\mathrm{L}}C_{\mathrm{L}})$, and g_{m} is the transconductance of $\mathrm{M}_{1,2}$. Its transfer function has high-pass filter characteristics as the solid line in Fig. 3-5. However, it is difficult to achieve high-frequency boosting without DC gain degradation [48]. To overcome above problem, a negative capacitance is added into the filter,

and its equivalent output impedance (Z_{NC}) can be described as:

$$Z_{NC} \cong -\frac{1}{sC_{NC}} \cdot \frac{g_{mNC} + s(C_{gsNC} + 2C_{NC})}{g_{mNC}}, \tag{3.8}$$

where g_{mNC} and C_{gsNC} represent transconductance and gate-source capacitance of $M_{3,4}$, respectively. As shown in Eq. (3.8), there are one pole (ω_{pNC}) and one zero (ω_{zNC}), and their location can be expressed as:

$$\omega_{pNC} \cong \frac{g_{mNC}}{C_{gsNC} + 2C_{NC} - g_{mNC}R_L C_{NC}}, \tag{3.9}$$

$$\omega_{zNC} \cong \frac{g_{mNC}}{C_{gsNC} + 2C_{NC}}. \tag{3.10}$$

The dashed-line in Fig. 3-5 shows the transfer function of the filter with capacitive degeneration and negative capacitance. It can be observed that high-frequency gain can be further boosted without any DC gain degradation. In addition, its boosting gain and frequency can be changed by adjusting poles and zeros position. In this work, a 3-bit capacitor array is used in source capacitor to change the boosting gain of the filter. The equivalent source capacitance (C_s) can be discretely controlled from zero to 210 fF in steps of 30 fF.

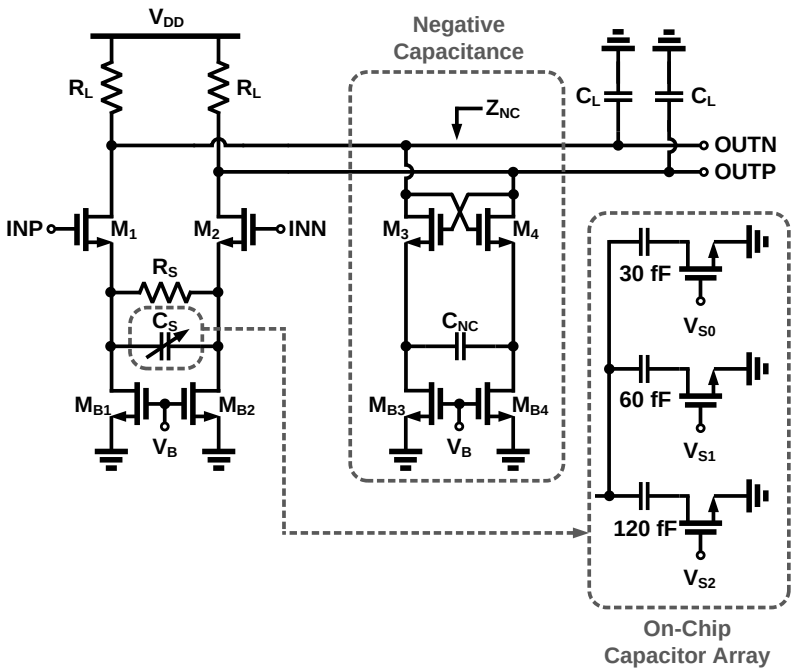


Fig. 3-4. Schematic diagram of tunable equalizer.

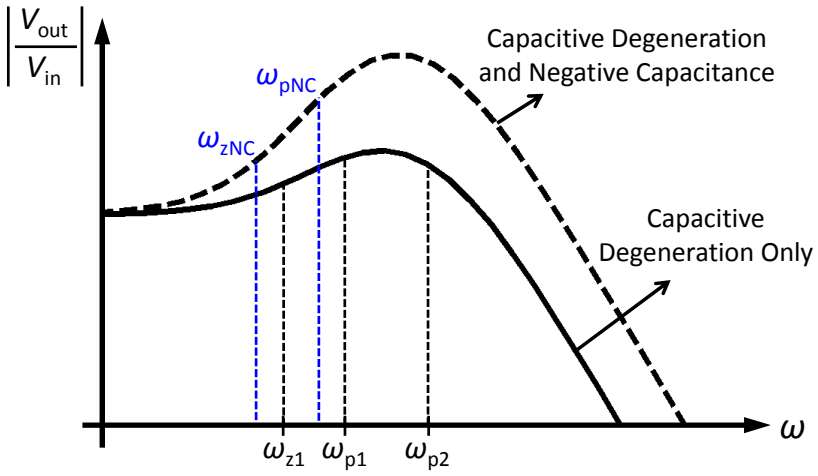


Fig. 3-5. Transfer functions of equalizer having capacitive degeneration and/or negative capacitance.

3-2-3. Limiting Amplifier

The main purpose of a limiting amplifier is to provide high voltage gain for reliable operation of the subsequent circuit or testing instrument without any performance degradation due to inter-symbol interference (ISI) penalty. Therefore, limiting amplifier should be designed to achieve high voltage gain as well as large bandwidth simultaneously. For this, most limiting amplifiers are designed in the open-loop configuration with cascaded gain stages, and various broadband circuit techniques are used for the individual gain stage [49]–[54]. Table 3-2 summarizes broadband circuit techniques and their drawbacks [55].

In order to achieve data rate up to 10 Gb/s and beyond, the inductive peaking technique is typically used [42], [49]. However, this technique has drawbacks of the large chip area for passive inductors and high supply voltage for active inductors. Another approach is using the active feedback technique [49], [52]. It can effectively increase gain-bandwidth product beyond the cut-off frequency effectively and to take up a small chip area compared to using passive inductors [49].

Table 3-2
Summary of broadband circuit techniques and drawbacks [55].

	TECHNIQUE	DRAWBACKS
Inductive peaking (Passive Inductors)	Resonates out load capacitance	Large chip area
Inductive Peaking (Active Inductors)	Use transistors as passive inductors	Voltage headroom
Capacitive Degeneration	Adds pole-zero pair	DC gain reduction
Negative Miller Capacitance	Compensates input capacitance	Capacitance matching
Cherry-Hooper Amplifier	Shunt feedback	Voltage headroom
Active Feedback	Signal feedback w/o resistive loading	Power consumption
Reverse Scaling	Stage sizing	Power consumption & input capacitance
Negative Capacitance	Compensates load capacitance	Gain peaking and ringing

For the cascaded limiting amplifier, the number of stages should be carefully determined by using the following estimation. Assuming that a limiting amplifier consists of *n*-identical cascaded gain stages, and each gain cell has m^{th}-order Butterworth frequency response, overall bandwidth (BW_{total}) of the cascaded limiting amplifier can be calculated as [52]

$$BW_{total} = BW_{cell} \cdot \sqrt[2m]{\sqrt[n]{2} - 1}, \tag{3.11}$$

where BW_{cell} represents the bandwidth of the individual gain cell. From above equation, the required gain-bandwidth product (GBW_{cell}) of the individual gain cell can be determined as:

$$GBW_{cell} = \frac{BW_{total}}{\sqrt[2m]{\sqrt[n]{2} - 1}} \cdot \sqrt[n]{A_{total}}, \tag{3.12}$$

where A_{total} is the overall voltage gain of the cascaded limiting amplifier.

Fig. 3-6 shows the calculated GBW_{cell} with different order of gain stages (*m*) as a function of the number of stages (*n*) for achieving A_{total} and BW_{total} of 40 dB and 10 GHz, respectively, which are design target. In this calculation, bandwidth degradation effects due to Miller effect

and device parasitic capacitance are included. As shown in Fig. 3-6, the GBW_{cell} decreases with increasing n. However, this approach has drawbacks of large power consumption as well as poor noise performance due to the insufficient gain per each cell. Thus, the cascaded limiting amplifier is typically implemented with no more than five gain stages. Another approach is using the individual gain cell having second- or third-order characteristics. However, the gain cell having high-order response can increase circuit complexity which requires careful design.

To achieve design target, for given 0.13-μm CMOS technology with f_T of about 90 GHz, the limiting amplifier is designed in five-stage gain stage, and the each gain cell has second-order characteristics.

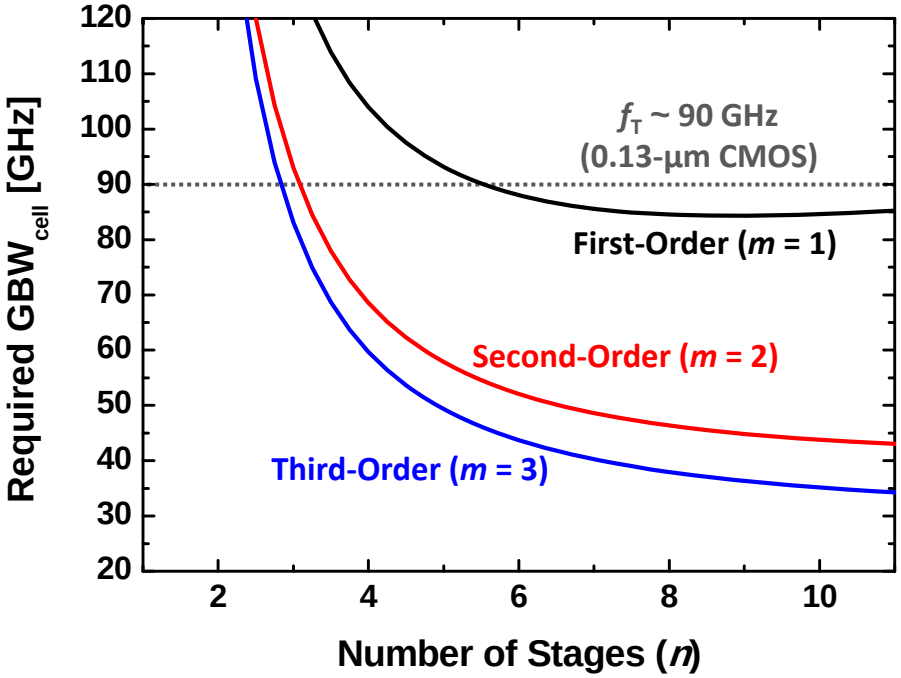


Fig. 3-6. Required gain-bandwidth product (GBW_{cell}) of the gain cell with different order (m) as a function of the number of stages (n).

Fig. 3-7(a) shows a block diagram of the designed limiting amplifier. It consists of two types of gain cells and an offset cancellation network. The odd gain cell is composed of a two-stage differential amplifier with active feedback as shown in Fig. 3-7(b). Its transfer function is given by

$$H(s) \cong \frac{(g_m R_L)^2}{\left(1+\frac{s}{\omega_p}\right)^2 + (g_m R_L)\cdot(g_{mf} R_L)}, \qquad (3.13)$$

where g_m and g_{mf} represent transconductance of $M_{1\sim4}$ and $M_{5,6}$ and $\omega_p = 1/(R_L C_L)$. R_L and C_L are load resistance and capacitance, respectively. For even gain cells, the negative capacitance is added as shown in Fig. 3-7(c) to compensate the limited bandwidth of the odd gain cell. The negative capacitance can cancel out load parasitic capacitance [53], [54]. By interleaving two types of gain cells, broadband flat response can be achieved. However, due to high voltage gain (~ 40 dB) of the designed limiting amplifier, small DC offset at the input node can cause large voltage offset at the output node. To eliminate these problems, the offset cancellation network is used, and it is composed of on-chip resistors and external capacitors of about 20 kΩ and 10 nF, respectively.

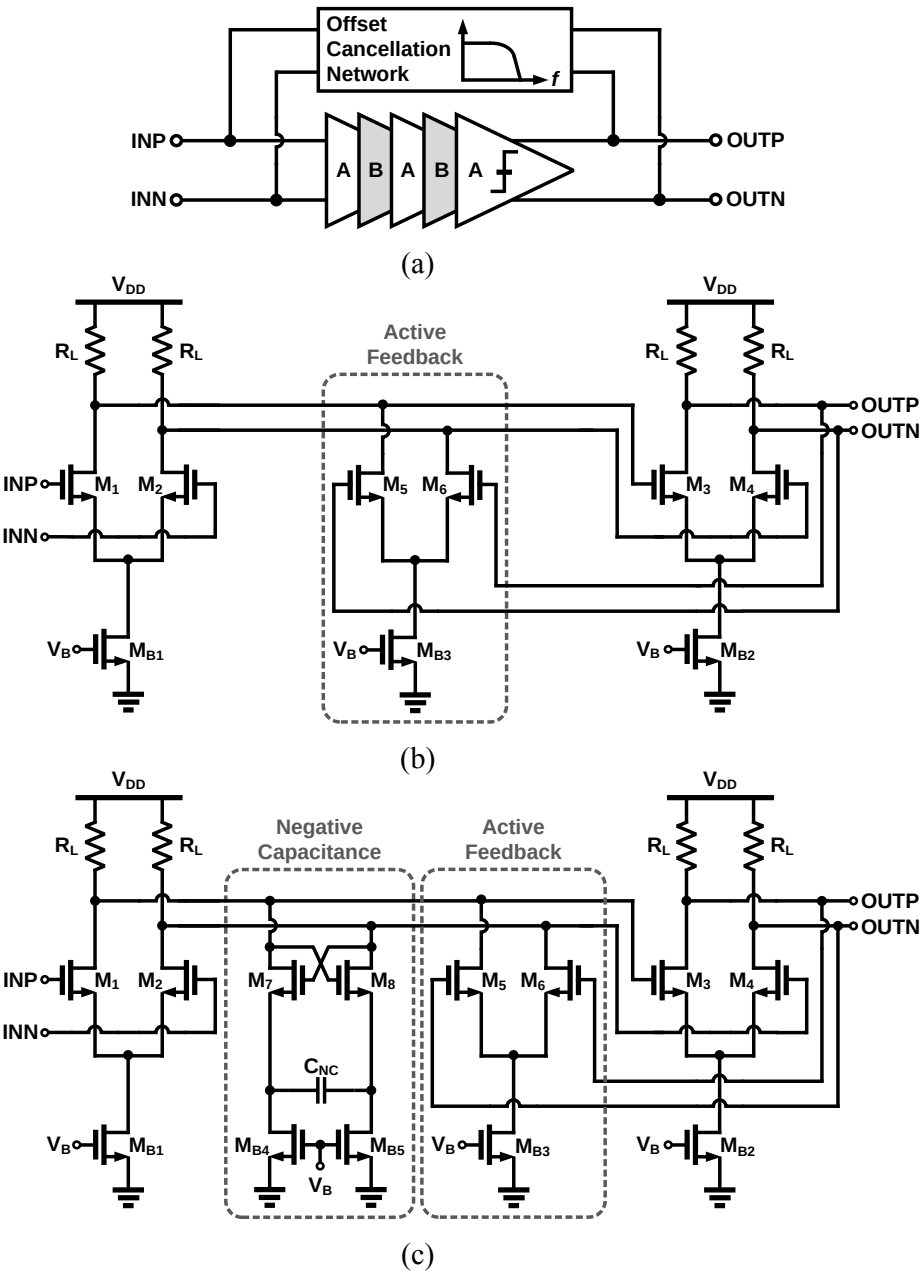


Fig. 3-7. (a) Block diagram of limiting amplifier and schematic diagrams of individual gain cell (b) with active feedback (c) with active feedback and negative capacitance.

3-2-4. Post-Layout Simulation Results

Fig. 3-8 shows post-layout simulated eye diagrams at different output nodes with 10-Gb/s input signals. For this simulation, the equivalent circuit model of APD is used. As shown in Fig. 3-8(a) and (b), eye diagrams are distorted and closed due to bandwidth limitation of APD and TIA with DC-balanced buffer. However, it is compensated by the equalizer, and consequently, clean eye diagram can be achieved at the equalizer output. Finally, these signals are further amplified by the limiting amplifier as shown in Fig. 3-8(d).

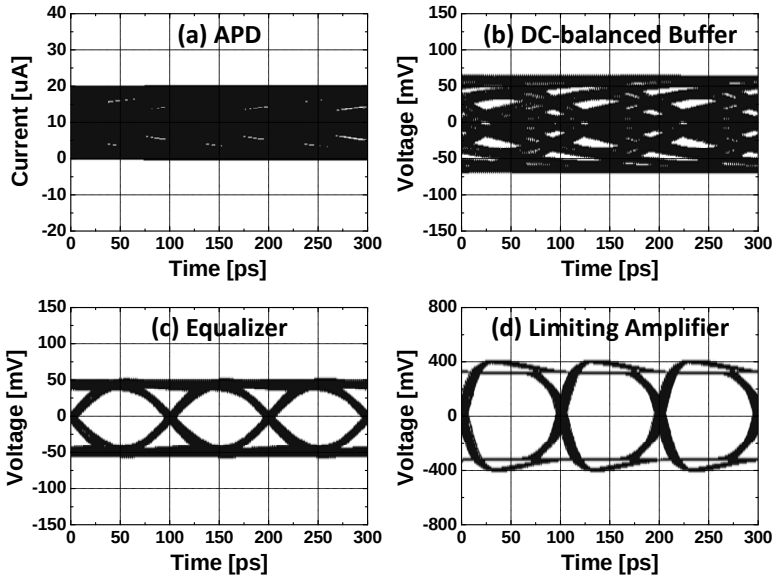


Fig. 3-8. Post-layout simulation results of 10-Gb/s eye diagrams at the output of (a) APD, (b) DC-balanced buffer, (c) equalizer, and (d) limiting amplifier.

3-3. Experimental Results

Fig. 3-9 shows the chip photograph of the fabricated CMOS OEIC receiver. The chip area is about 1.0 mm × 0.26 mm. The power consumption excluding output buffer is about 66.8 mW with 1.2-V supply voltage. Fig. 3-10 shows the measurement setup for photodetection frequency response and broadband optical data detection. All experiments for the OEIC receiver characterization are done with on-wafer probing setup. An 850-nm laser diode is used as an optical source and its output light is modulated by an external electro-optic modulator using a 2^7-1 pseudo random bit sequence (PRBS) pattern. The modulated optical signals are transmitted through MMF and injected into the OEIC receiver using a lensed fiber. A power monitor-attenuator is used to control the incident optical power. An S-parameter network analyzer is used to measure photodetection frequency response. The applied bias voltage of APD (V_{PD}) is experimentally optimized to 10.5 V by monitoring BER performance of the fabricated OEIC receiver.

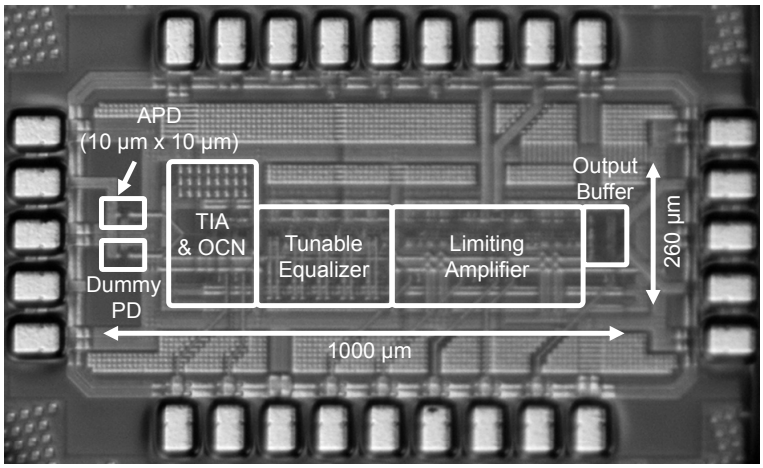


Fig. 3-9. Chip photograph of the fabricated CMOS OEIC receiver.

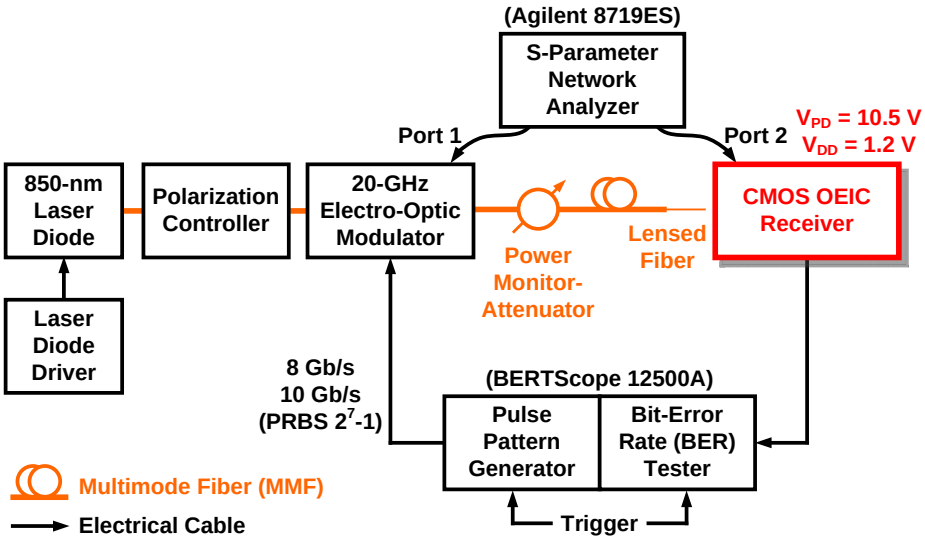


Fig. 3-10. Measurement setup.

Fig. 3-11 shows the measured BER performance as a function of V_{PD} with 10-Gb/s optical data with P_{opt} of −4 dBm. At V_{PD} of 10.5 V, 10-Gb/s optical data is successfully detected with BER less than 10^{-12}. However, the BER performance is degraded for V_{PD} below 10.5 V due to insufficient APD output signal, and the BER also degraded for V_{PD} above 10.5 V due to increased avalanche noises. Fig. 3-12 shows the measured photodetection frequency response of the fabricated OEIC receiver. For this measurement, V_{PD}, C_s, and P_{opt} are set to 10.5 V, 210 fF, and −4 dBm, respectively. The measured transimpedance gain and 3-dB bandwidth are about 100 dBΩ and 6 GHz, respectively. Fig. 3-13 shows the measured BER performance as a function of P_{opt} for 8-Gb/s and 10-Gb/s optical data transmission. The optical sensitivities for BER less than 10^{-12} are −6 and −4 dBm for 8 Gb/s and 10 Gb/s, respectively. Fig. 3-14 shows the measured eye diagrams for differential signals when 8-Gb/s and 10-Gb/s optical data are successfully detected with P_{opt} of −6 dBm and −4 dBm, respectively.

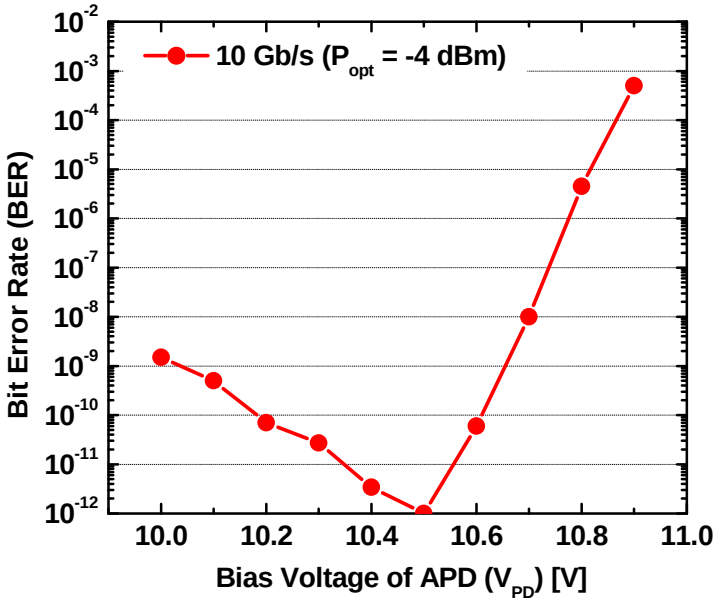


Fig. 3-11. Measured BER performance as a function of applied bias voltage of APD (V_{PD}).

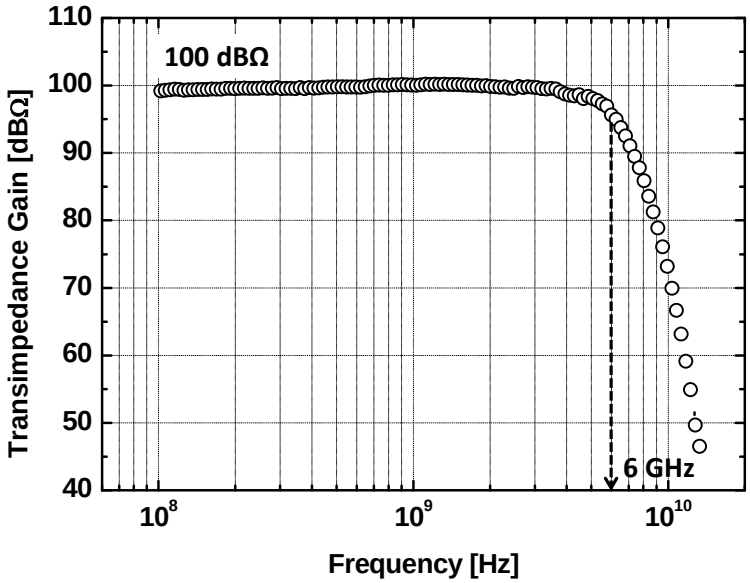


Fig. 3-12. Measured photodetection frequency response of the fabricated CMOS OEIC receiver.

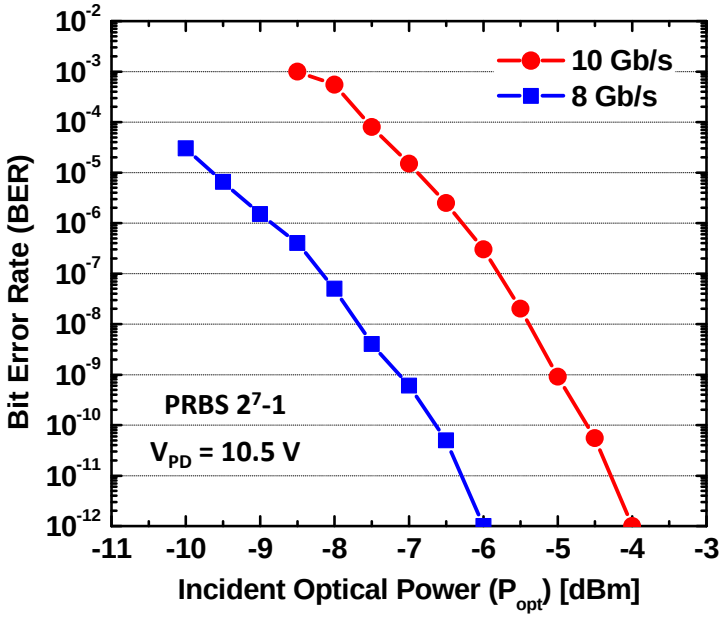


Fig. 3-13. Measured BER performance as a function of incident optical power (P_{opt}).

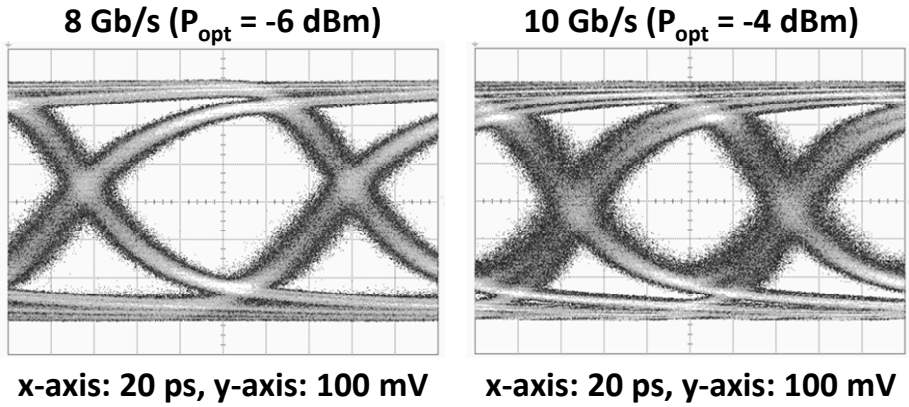


Fig. 3-14. Measured eye diagrams of 8 Gb/s and 10 Gb/s.

3-4. Summary

A 10-Gb/s OEIC receiver is realized with standard 0.13-μm CMOS technology for 850-nm optical interconnect applications. It consists of on-chip APD and electronic circuits including TIA, equalizer, and limiting amplifier. With the fabricated CMOS OEIC receiver, we successfully demonstrate 10-Gb/s optical data transmission with BER less than 10^{-12} at the incident optical power of −4 dBm. It is expected that the CMOS OEIC receiver has a great potential for application in cost-effective 850-nm optical interconnect systems. Table 3-3 summarizes chip design and demonstration results of the fabricated CMOS OEIC receiver. Table 3-4 shows the performance comparison with previously reported Si OEIC receivers.

Table 3-3

Performance summary of 10-Gb/s 850-nm CMOS OEIC receiver.

DESIGN RESULTS	
Technology	0.13-μm CMOS
Receiver Structure	APD+TIA+EQ+LA
Photodetector	P^+/N-well APD (10 μm × 10 μm)
Overall Transimpedance Gain	100 dBΩ
3-dB Bandwidth	6 GHz
Power Consumption (excluding output buffer)	66.8 mW at 1.2-V supply
Chip Area	1.0 mm × 0.26 mm
DEMONSTRATION RESULTS	
Maximum Data Rate	10 Gb/s
Sensitivity	−4 dBm
BER (PRBS)	10^{-12} (2^7-1)
Optimum APD Bias Voltage (V_{PD})	10.5 V
Power Efficiency	6.68 mW/Gb/s

Table 3-4
Performance comparison with Si OEIC receivers.

.

	[22] 05' JSSC	**[28] 10' TCAS1**	**[29] 10' JSSC**	**[30] 11' JSSC**	**This work (Chap. 3)**
Receiver Structure	N-well/P-sub PD+TIA+EQ	SML+TIA +EQ+LA	SML+TIA +EQ+LA	Meshed SML+TIA+LA (9 passive inductors)	**APD+TIA +EQ+LA**
Technology	0.18-µm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.18-µm CMOS	**0.13-µm CMOS**
Maximum Data Rate	3 Gb/s	5 Gb/s	8.5 Gb/s	10 Gb/s	**10 Gb/s**
Sensitivity	-19 dBm	-3 dBm	-3.2 dBm	-6 dBm	**-4 dBm**
BER (PRBS)	10^{-11} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-11} (2^{7}-1)	**10^{-12} (2^{7}-1)**
Supply Voltage	1.8 V	3.3 V (PD/TIA) 1.8 V (Other circuits)	1.5 V	1.8 V (Circuit) 14.2 V (PD)	**1.2 V (Circuit) 10.5 V (PD)**
Power Consumption	34 mW	183 mW	47 mW	118 mW	**66.8 mW**
Power Efficiency	11.3 mW/Gbps	36.6 mW/Gbps	5.53 mW/Gbps	11.8 mW/Gbps	**6.68 mW/Gbps**
Chip Area	N/A	0.72 mm^2	0.1 mm^2	0.76 mm^2	**0.26 mm^2**

4. High-Speed 850-nm SiGe BiCMOS OEIC Receiver

4-1. CMOS vs. SiGe BiCMOS Technology

The OEIC receiver can be realized with SiGe BiCMOS technology which can integrate SiGe heterojunction bipolar transistors (HBTs) with CMOS technologies on a single substrate. Typically, SiGe HBTs with Ge doping for the base can provide faster switching speed and larger current gain than CMOS transistors [56]. Therefore, OEIC receiver fabricated SiGe BiCMOS technology can achieve simple structure as well as high-speed operation. Fig. 4-1 shows the cut-off frequencies (f_T) with different CMOS and SiGe BiCMOS technologies [57].

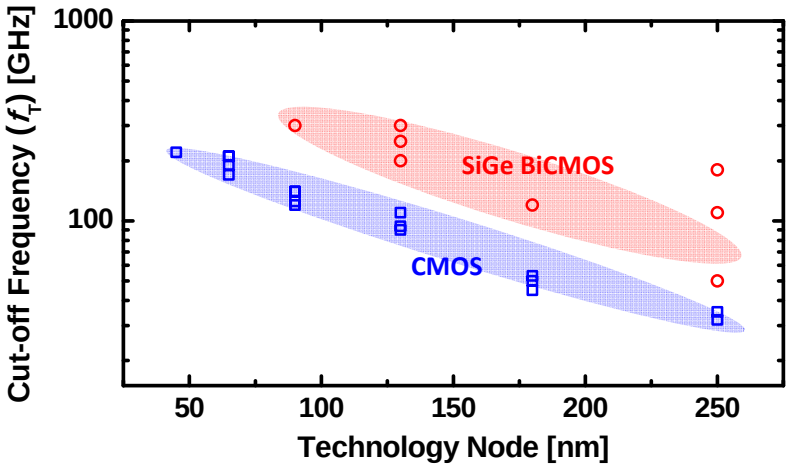


Fig. 4-1. Cut-off frequency (f_T) of standard Si technology [57].

4-2. Overall Structure

Fig. 4-2(a) shows a simplified block diagram of the proposed 850-nm OEIC receiver fabricated with IHP's standard 0.25-μm SiGe BiCMOS technology [58]. The OEIC receiver is composed of APD with dummy PD and BiCMOS electronic circuits including TIA with DC-balanced buffer, tunable equalizer, limiting amplifier, and output buffer with 50-Ω loads. The APD is realized P^+/N-well junction using CMOS processing only. This junction is surrounded by shallow trench isolation. The APD has optical window is about 10 μm × 10 μm. The dummy PD having the same structure as the main APD is used to provide identical capacitance for differential TIA inputs. For receiver circuit design, SiGe HBTs having high-frequency performance are used for differential input pair to achieve high gain and large bandwidth, and NMOS transistors having high input impedance are used for current mirror to minimize current mismatch. In particular, the following chapters focus on SNR characteristics of APD and OEIC receiver for optimal design of OEIC receiver.

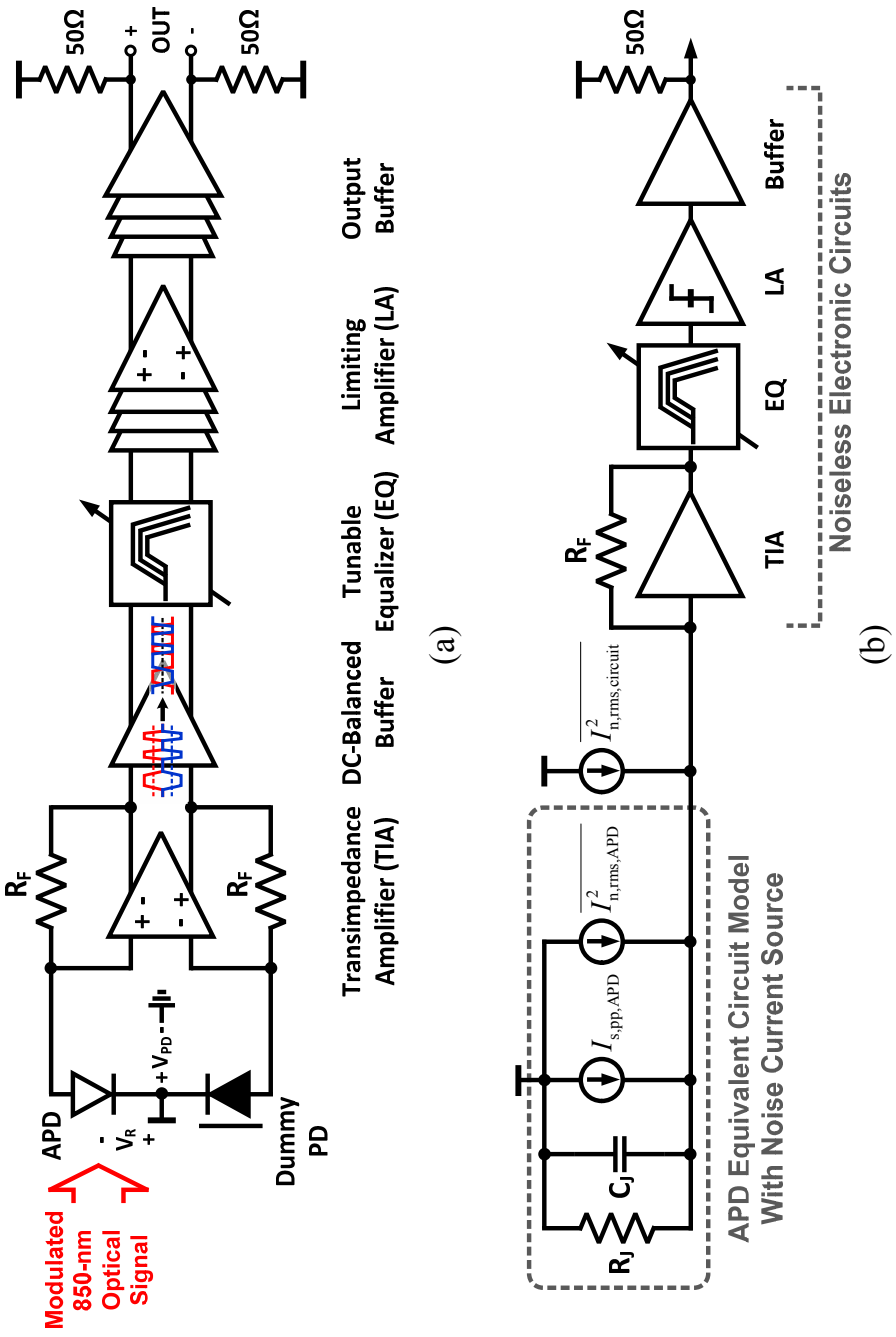


Fig. 4-2. Simplified block diagram of (a) the proposed OEIC receiver (b) OEIC receiver for signal-to-noise ratio investigation.

4-3. Signal-to-Noise Ratio Estimation

Fig. 4-2(b) shows a block diagram of the OEIC receiver for SNR investigation. An APD equivalent circuit model [39] including a noise current source is shown, and the electronic circuit noise is modeled with an input-referred noise current source ($I_{n,rms,circuit}$). The APD transit time effect is included in both current sources of $I_{s,pp,APD}$ and $I_{n,rms,APD}$. In a similar way of chapter 2-3, the OEIC receiver SNR (SNR_{OEIC}) can be calculated by adding the $I_{n,rms,circuit}$ into the Eq. (2.4).

$$SNR_{OEIC}(V_R) = \frac{I_{s,pp,APD}(V_R)}{\sqrt{\overline{I^2_{n,rms,APD}}(V_R) + \overline{I^2_{n,rms,circuit}}}}. \quad (4.1)$$

As can be seen, SNR_{OEIC} is also affected by the reverse bias voltage. With the measured $I_{s,pp,APD}$ and $I_{n,rms,APD}$ presented in chapter 2-3, numerical value of the SNR_{OEIC} can be estimated with different $I_{n,rms,circuit}$ of 1, 2, and 3 μA_{rms}.

The resulting SNR_{OEIC} is shown in Fig. 4-3 for both P_{opt} of −8 and −10 dBm. With increasing $I_{n,rms,circuit}$, SNR_{OEIC} is continuously degraded, and V_R range for satisfying the specific SNR is decreased. For example, SNR of about 14 is required for achieving BER of 10^{-12} which is

design target. As shown in Fig. 4-3(b), for P_{opt} of −10 dBm, SNR_{OEIC} is hard to achieve the target BER performance for all case of $I_{n,rms,circuit}$. For P_{opt} of −8 dBm, there are a few V_R points to satisfy SNR of about 14 with $I_{n,rms,circuit}$ of 2 and 3 μA_{rms} as shown in Fig. 4-3(a). To achieve BER less than 10^{-12} for wide range of V_R, the $I_{n,rms,circuit}$ should be minimized to less than 1 μA_{rms}, and electronic circuit configurations should be carefully determined.

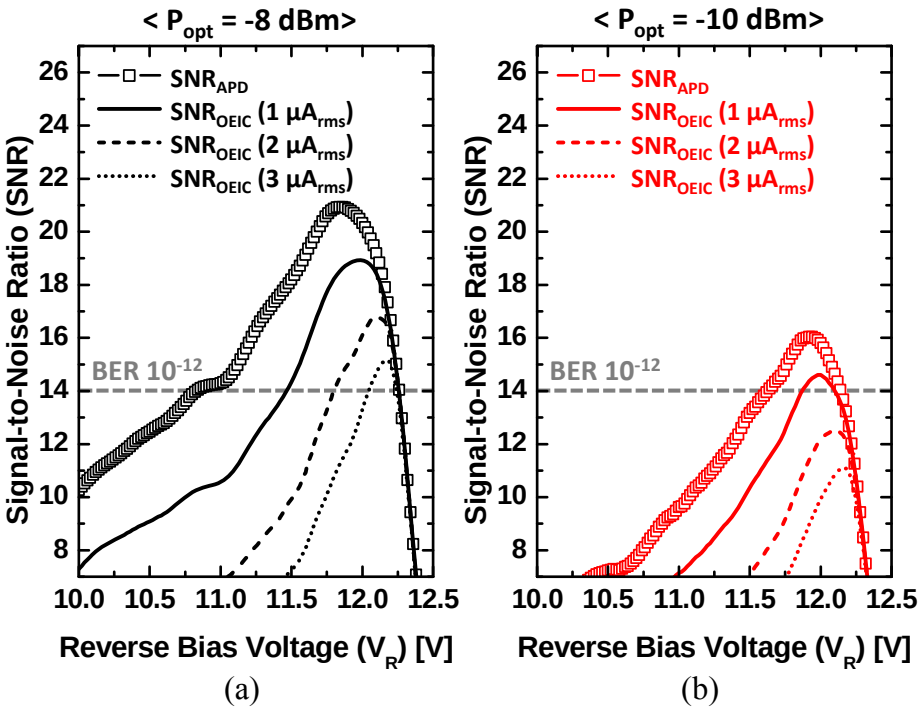


Fig. 4-3. Estimated SNR_{APD} and SNR_{OEIC} as a function of reverse bias voltage (V_R) at incident optical power (P_{opt}) of (a) −8 and (b) −10 dBm, respectively.

4-4. Circuit Implementation

4-4-1. Transimpedance Amplifier

The $I_{\text{n,rms,circuit}}$ can be expressed as

$$\overline{I_{\text{n,rms,circuit}}^2} \simeq \overline{I_{\text{n,rms,TIA}}^2} + \frac{\overline{V_{\text{n,rms,other}}^2}}{T_{\text{z,TIA}}^2}, \tag{4.2}$$

where $T_{\text{z,TIA}}$ and $I_{\text{n,rms,TIA}}$ are transimpedance gain and input-referred rms noise current of TIA, respectively. $V_{\text{n,rms,other}}$ is rms noise voltage at TIA output due to equalizer and limiting amplifier. To minimize $I_{\text{n,rms,circuit}}$ less than 1 μA_{rms}, TIA should be carefully designed and optimized more than other circuits because $I_{\text{n,rms,circuit}}$ is mainly affected by the $I_{\text{n,rms,TIA}}$, and $V_{\text{n,rms,other}}$ contribution to the $I_{\text{n,rms,circuit}}$ is determined by $T_{\text{z,TIA}}$.

The TIA is designed in shunt-feedback configuration as shown in Fig. 4-4 since it can provide higher transimpedance gain as well as lower noise characteristics than any other TIA configurations [41]. The TIA is composed of a core amplifier and a feedback resistance (R_F). Assuming the core amplifier has transfer function of $A(s) = A_0 / (1 + s/\omega_0)$, transfer function of the shunt-feedback TIA can be expressed as a second-order

system [47].

$$H(s) = -\frac{A_0 R_F}{A_0 + 1} \cdot \frac{\omega_n^2}{s^2 + 2\varsigma\omega_n s + \omega_n^2}, \tag{4.3}$$

where

$$\omega_n^2 = \frac{(A_0 + 1)\omega_0}{R_F C_D}, \tag{4.4}$$

$$\varsigma = \frac{1}{2} \cdot \frac{R_F C_D \omega_0 + 1}{\sqrt{(A_0 + 1)\omega_0 R_F C_D}}, \tag{4.5}$$

where A_0 and ω_0 represent DC gain and pole frequency of the core amplifier, and C_D represents parasitic capacitance due to the TIA input transistors and photodetector. For designing TIA without any ringing in time domain, damping factor (ζ) of 0.707 is desired, and it means that TIA has critically-damped behavior.

As s $\rightarrow$ 0, mid-band transimpedance gain of the TIA at low frequency is derived as Eq. (4.6). The 3-dB bandwidth of the TIA can be derived as Eq. (4.7) with the following assumptions. The core amplifier has larger bandwidth than closed-loop TIA bandwidth, that is, TIA has critically-damped response. Lastly, input-referred noise current

of the TIA having CMOS- and BJT-based core amplifier can be derived as Eq. (4.8) and (4.9), respectively.

$$\text{Transimpedance gain} \simeq -\frac{A_0}{A_0+1}\cdot \mathrm{R_F}, \tag{4.6}$$

$$\text{3-dB bandwidth} \simeq \frac{1}{2\pi}\cdot\frac{\sqrt{2}A_0}{R_F C_\mathrm{D}}, \tag{4.7}$$

$$\text{Input-referred noise current}$$
$$\simeq \frac{4kT}{R_\mathrm{F}}+\frac{4kT\Gamma}{g_m}\left(\frac{1}{R_\mathrm{F}^2}+\left(2\pi C_\mathrm{D} f\right)^2\right), \tag{4.8}$$

$$\simeq \frac{4kT}{R_\mathrm{F}}+\frac{2qI_C}{g_m^2}\left(\frac{1}{R_\mathrm{F}^2}+\left(2\pi C_\mathrm{D} f\right)^2\right), \tag{4.9}$$

where Γ is channel noise factor in MOS transistor, q and I_C represent the electronic charge and collector current in BJT, respectively. C_D represents parasitic capacitance due to the TIA input transistors and photodetector. As can be seen, the shunt-feedback TIA design parameters are directly related with $\mathrm{R_F}$. Fig. 4-5 shows simulation results of transimpedance gain and input-referred noise current as a function of $\mathrm{R_F}$. As expected, with increasing $\mathrm{R_F}$, transimpedance gain is gradually increased, while input-referred noise current is gradually decreased. Fig. 4-5 also shows the simulated 3-dB bandwidth at the

TIA output, for this simulation, the simplified APD equivalent circuit model is used. With increasing R_F, the 3-dB bandwidth is decreased because the bandwidth is limited by APD transit time effect as well as dominant pole due to C_D and R_F. As a result, in our design, R_F of 3 kΩ is used to achieve low-noise characteristics as well as large bandwidth simultaneously.

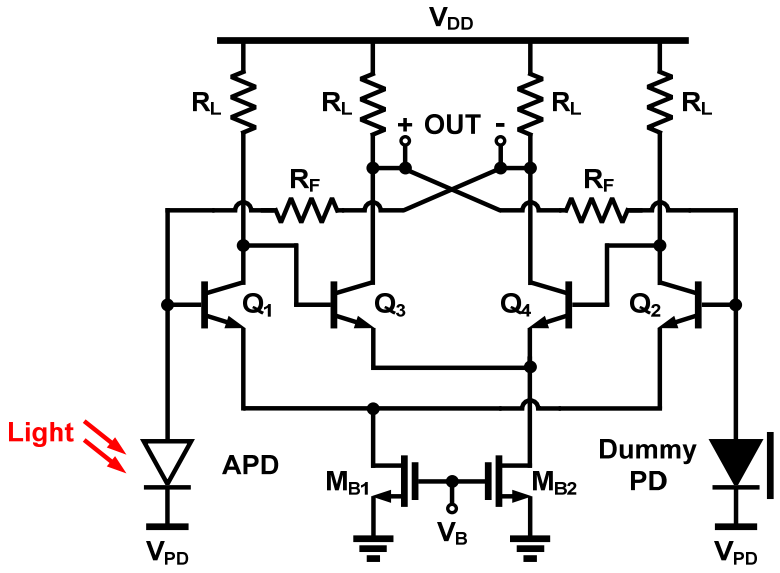


Fig. 4-4. Schematic diagram of transimpedance amplifier.

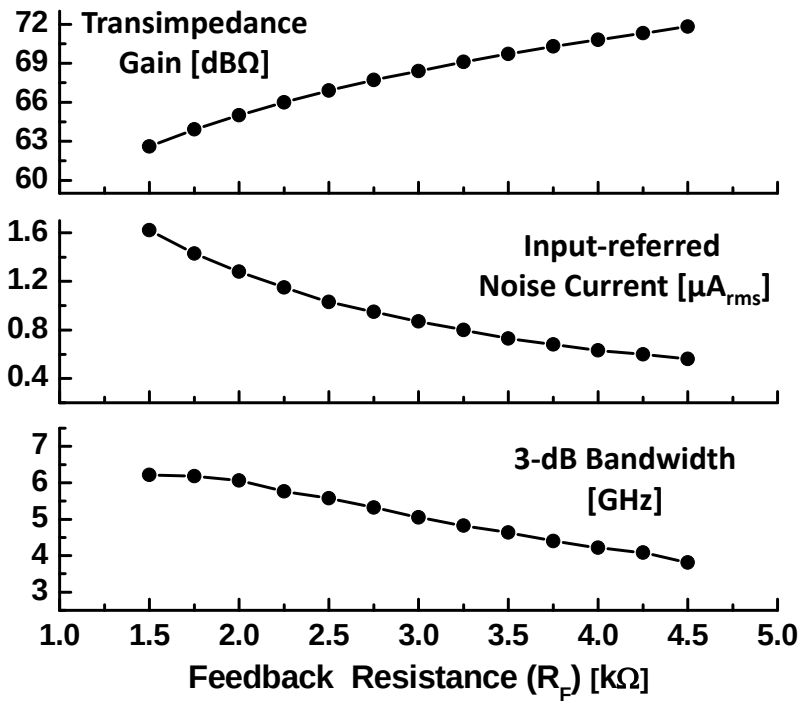


Fig. 4-5. Simulation results of transimpedance amplifier.

Fig. 4-6 shows a schematic diagram of the DC-balanced buffer. It is composed of f_T-doubler amplifier and two low-pass filters. NMOS transistors having high input impedance are used for input differential pair to achieve signal conversion without any DC voltage changes. With the DC-balanced buffer, pseudo-differential signal is converted to fully-differential signal. The low cut-off frequency of the buffer is set to 1 MHz to prevent any DC droop problem. Fig. 4-7 shows the post-layout simulated frequency response at the DC-balanced buffer output. The transimpedance gain and 3-dB bandwidth are about 68.4 dBΩ and 5.2 GHz, respectively. However, the bandwidth is insufficient design target for 12.5-Gb/s operation because there is high-frequency loss of about 10.8 dB at 8.7 GHz. As a result, 12.5-Gb/s eye diagram for differential signals is distorted and closed due to the bandwidth limitation of the APD and TIA with the buffer as shown in the inset of Fig. 4-7. To compensate high-frequency loss and achieve the clean eye diagram, an equalizer having high-pass filter characteristic should be required, and it will be discussed in next chapter.

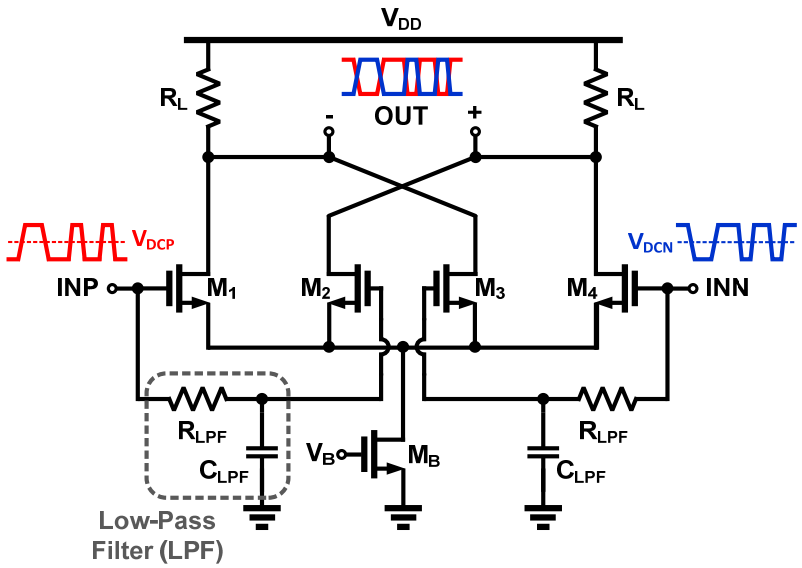


Fig. 4-6. Schematic diagram of DC-balanced buffer.

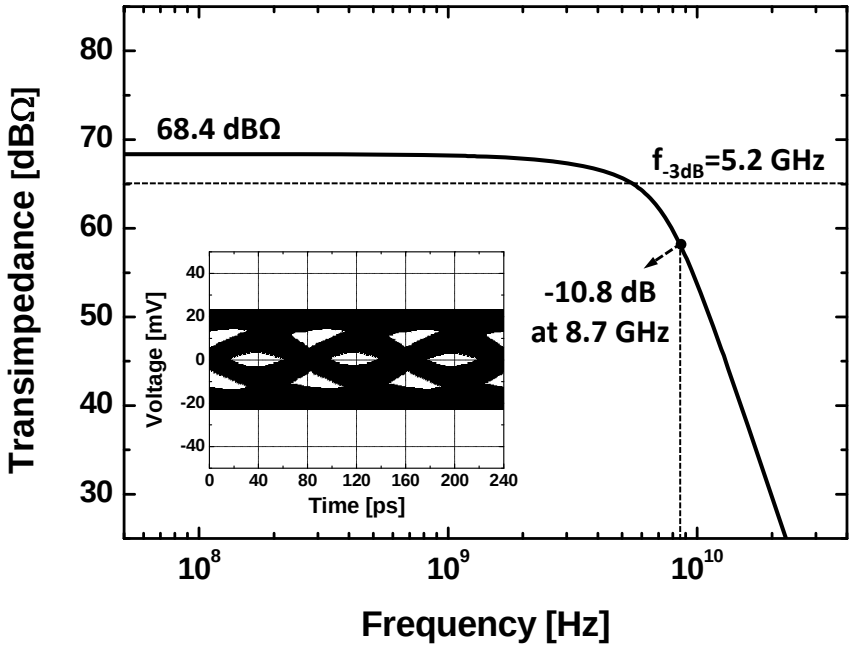


Fig. 4-7. Post-layout simulated frequency response and eye diagram with 12.5-Gb/s input data at the DC-balanced buffer output.

4-4-2. Equalizer

Fig. 4-8 shows a schematic diagram of the equalizer. It is composed of a differential configuration with emitter degeneration. In order to achieve the 10.8-dB boosting gain, one-stage equalizer filter is enough since SiGe HBTs provide high-frequency operation as well as large current gain. A capacitor array in emitter capacitor composed of metal-insulator-metal capacitors and on-chip NMOS switches is used to control boosting gain. The gate voltage of NMOS switches is externally controlled. The equivalent emitter capacitance (C_E) can be discretely controlled from nominally zero to 750 fF. Fig. 4-9 shows the post-layout simulated frequency responses at the equalizer output. It can be observed that the receiver bandwidth can be changed from 7.5 GHz to 8.8 GHz by varying C_E. The inset of Fig. 4-9 also shows the post-layout simulated 12.5-Gb/s eye diagram for differential signals at the equalizer output with C_E of 300 fF. As can be seen, clean eye diagram can be achieved without any ringing.

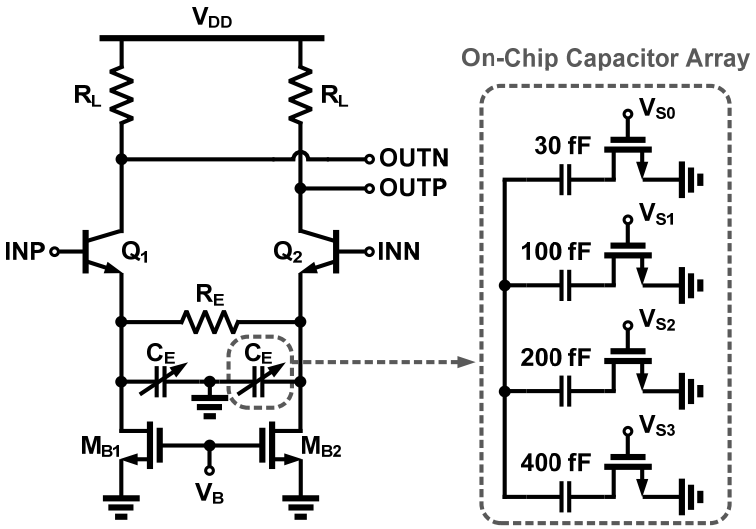


Fig. 4-8. Schematic diagram of equalizer with capacitor array.

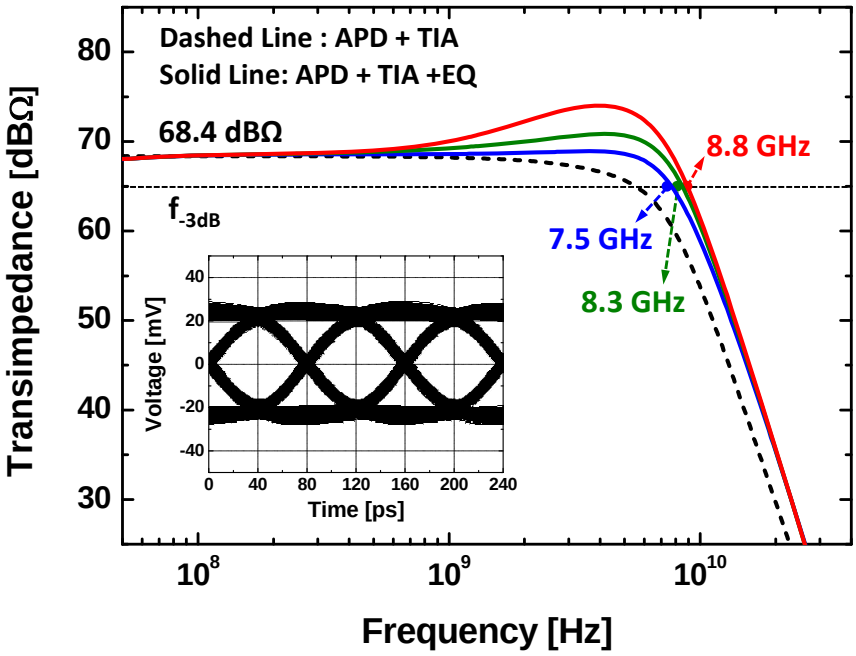


Fig. 4-9. Post-layout simulated frequency responses and eye diagram with 12.5-Gb/s input data at the equalizer output.

4-4-3. Limiting Amplifier

Fig. 4-10 shows a schematic diagram of the limiting amplifier. It is composed of four-stage gain stage, and individual gain cell consists of differential amplifier with resistive and capacitive degeneration. To compensate DC offset, on-chip low-pass filters are implemented with a feedback network made up of resistors and MOS capacitors. Fig. 4-11 shows the post-layout simulated frequency response of the limiting amplifier. The simulated mid-band gain and 3-dB bandwidth are about 41.8 dB and 12.2-GHz, respectively. The inset of Fig. 4-11 shows the post-layout simulated eye diagram for differential signals, and the limited signal can be achieved at the limiting amplifier output.

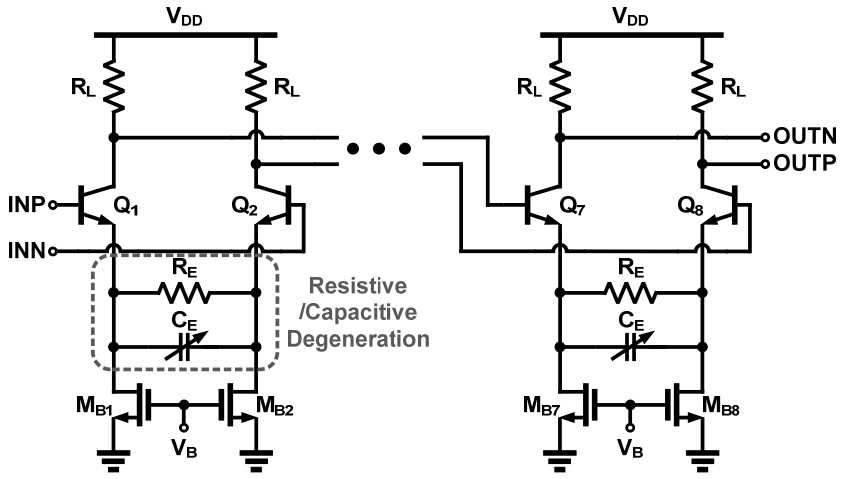


Fig. 4-10. Schematic diagram of limiting amplifier with resistive and capacitive degeneration.

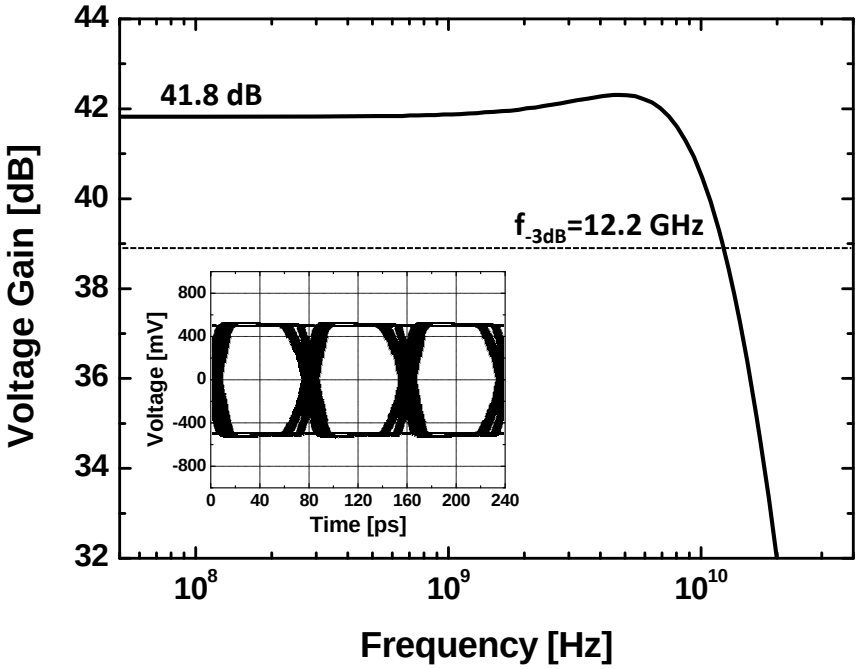


Fig. 4-11. Post-layout simulated frequency response and eye diagram with 12.5-Gb/s input data at the limiting amplifier output.

4-5. Experimental Results

Fig. 4-12 shows the chip photograph of the fabricated BiCMOS OEIC receiver. The chip area is about 1.0 mm × 0.28 mm. The power consumption excluding output buffer is about 59 mW with 2.5-V supply voltage. Fig. 4-13 shows the measurement setup for the fabricated OEIC receiver characterization, and all experiments are done on-wafer probing. The BER performance of the OEIC receiver is measured by using PRBS of the length 2^{31}-1. The PRBS data are used to modulate optical signals using an 850-nm laser diode and an external electro-optic modulator. The modulated optical signals are injected into the fabricated BiCMOS OEIC receiver using a lensed fiber after MMF. A power monitor-attenuator is used to control the incident optical power. An S-parameter network analyzer is used to measure photodetection frequency response of the OEIC receiver with prior cable calibration. Similar to the CMOS OEIC receiver in chapter 3, the BER performance of the OEIC receiver is affected by the applied bias voltage for APD (V_{PD}) which is about 2.2 V larger than V_R due to the TIA structure. In the case of the BiCMOS OEIC receiver, the best BER performance can be achieve at V_R of about 12.0 V, and the details of this dependence and analysis will be discussed in the following chapter.

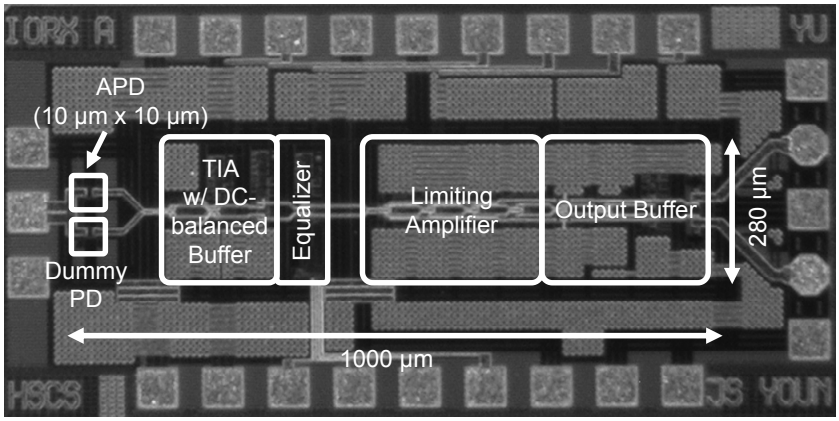


Fig. 4-12. Chip photograph of the fabricated BiCMOS OEIC receiver.

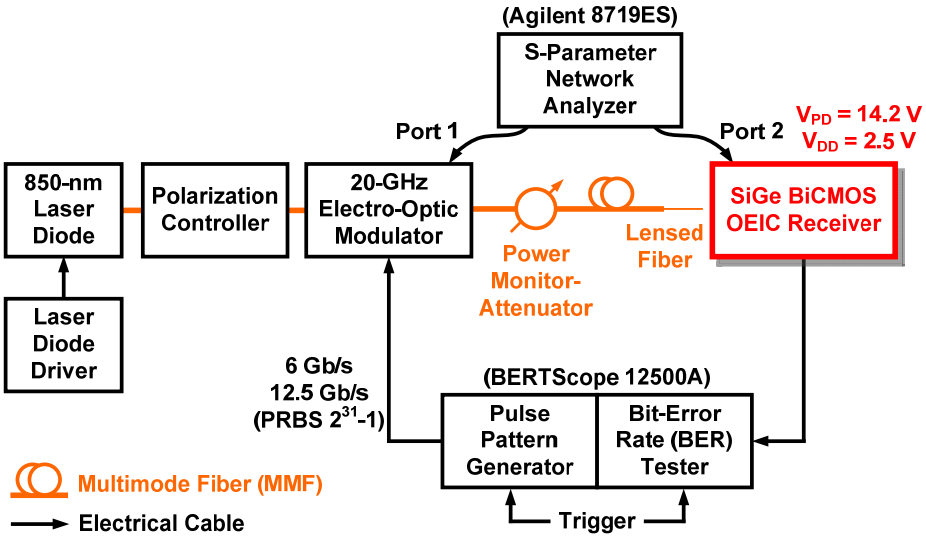


Fig. 4-13. Measurement setup.

Fig. 4-14 shows the measured photodetection frequency response at P_{opt} of −7 dBm. The measured transimpedance gain and 3-dB bandwidth of the fabricated OEIC receiver are about 110 dBΩ and 8.4 GHz, respectively. Fig. 4-15 shows the measured BER performance as a function of the incident optical power for 6-Gb/s and 12.5-Gb/s optical data transmission. The measured optical sensitivities for BER less than 10^{-12} are −9 and −7 dBm for 6 Gb/s and 12.5 Gb/s, respectively. Fig. 4-16 shows the measured eye diagrams for differential signals when 6-Gb/s and 12.5-Gb/s optical data are successfully detected with P_{opt} of −9 dBm and −7 dBm, respectively.

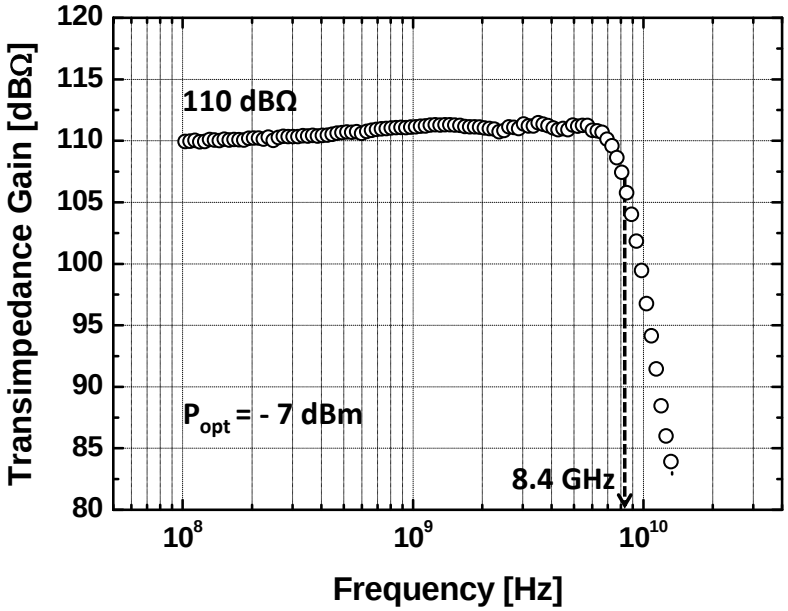


Fig. 4-14. Measured photodetection frequency response of the fabricated BiCMOS OEIC receiver.

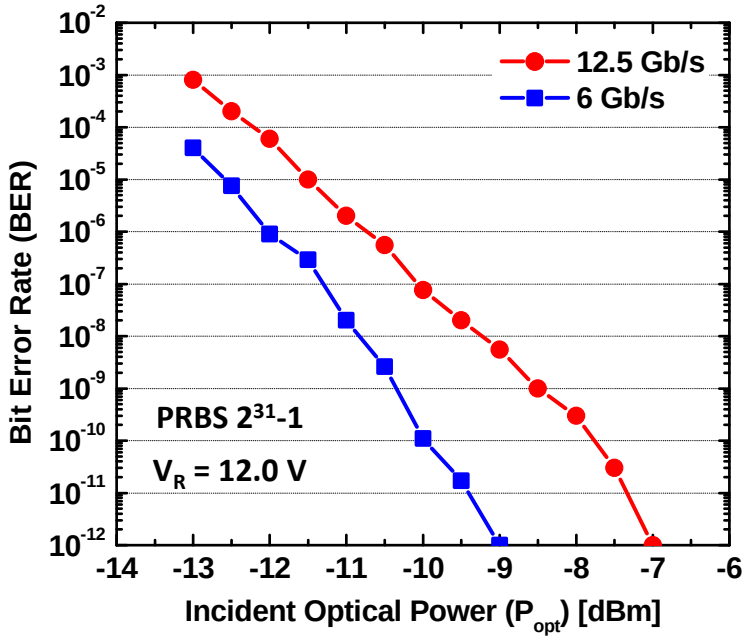


Fig. 4-15. Measured BER performance as a function of incident optical power (P_{opt}).

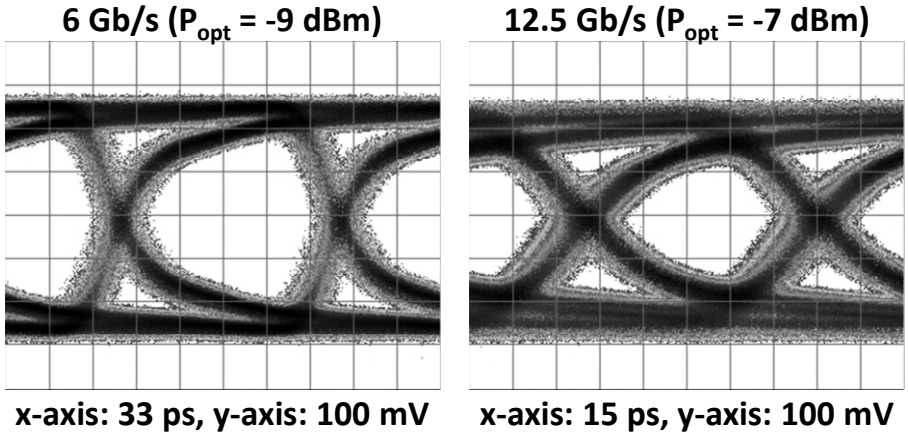


Fig. 4-16. Measured eye diagrams for differential signals of 6 Gb/s and 12.5 Gb/s.

4-6. Signal-to-Noise Ratio Verification

$I_{n,rms,circuit}$ of the fabricated receiver circuit is measured to estimate SNR_{OEIC}. For measuring $I_{n,rms,circuit}$, a receiver circuit without on-chip APD fabricated within the same run as the OEIC receiver is used. For noise measurement, the input node is left open, and one of two differential outputs is terminated with 50-Ω load, and the other is connected to the spectrum analyzer [59]. The noise frequency characteristics of the receiver circuit are measured from 100 MHz to 10 GHz with no equalization, and the effect of electrical cable loss is calibrated. The output noise power is converted into output noise voltage, and then, the output noise voltage is referred to the input node by dividing the resulting output noise voltage with the measured signal frequency response of the receiver circuit. Fig. 4-17 shows the resulting input-referred noise current density ($i_{n,circuit}$) as well as the measured signal frequency response. The $I_{n,rms,circuit}$ can be determined as below equation [60]:

$$\overline{I_{n,rms,circuit}^2} = \left[\int_{100\,MHz}^{BW_s} \overline{i_{n,circuit}^2} df \right] \cdot \frac{BW_n}{BW_s}, \tag{4.10}$$

where BW_s and BW_n represent signal and equivalent noise bandwidth of the receiver circuit, respectively. The resulting $I_{n,rms,circuit}$ of the receiver

circuits is about 0.83 μA_{rms}. Fig. 4-17 also shows the measurement results agree well with the simulation results.

Using the Eq. (2.4) and Eq. (4.1), numerical values for SNR_{APD} and SNR_{OEIC} can be determined. For this calculation, the measured $I_{s,pp,APD}$ and $I_{n,rms,APD}$ presented in chapter 2-3 are used. In addition, the measured $I_{n,rms,circuit}$ of 0.83 μA_{rms} is used. Fig. 4-18 shows the resulting SNR_{APD} and SNR_{OEIC} with different bias voltages. As mentioned in chapter 2-3, SNR_{APD} is the highest for V_R of about 11.9 V. It is different to the maximum-signal bias condition of 12.4 V. The short-dashed lines in Fig. 4-18 show the estimated SNR_{OEIC}, and the optimal V_R for SNR_{OEIC} is slightly higher than that for SNR_{APD} since APD needs to provide slightly larger gain due to the receiver circuit noise. For V_R below 12.0 V, SNR_{OEIC} is degraded because APD has insufficient signal current. For V_R above 12.0 V, SNR_{OEIC} is degraded due to the increased APD noise.

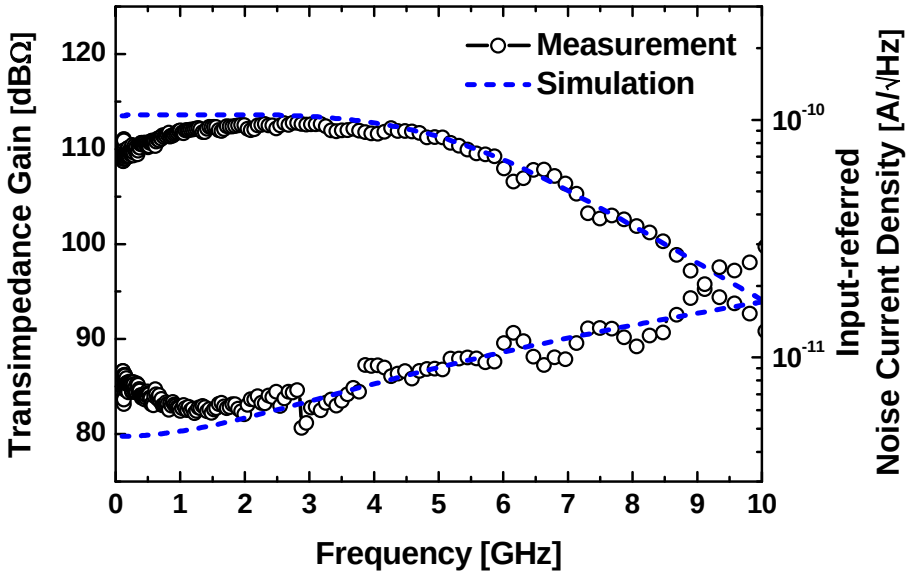


Fig. 4-17. Measured and simulated signal and noise frequency characteristics of the receiver circuit with no equalization.

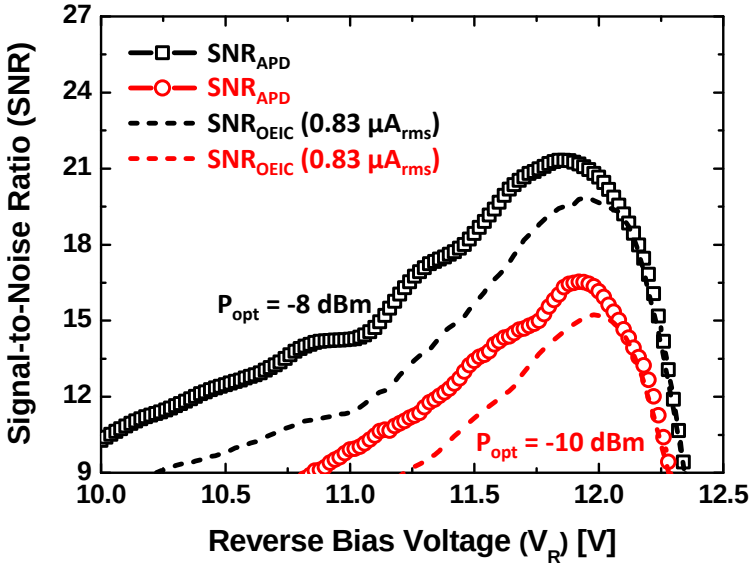


Fig. 4-18. Estimated SNR_{APD} and SNR_{OEIC} as a function of reverse bias voltage (V_R) at incident optical power (P_{opt}) of −8 and −10 dBm, respectively.

To verify the accuracy of the estimated SNR_{OEIC}, BER performance of the OEIC receiver is measured with different V_R, and the results are compared with the BER derived from SNR_{OEIC}. For this measurement, equalizer boosting gain is minimized to alleviate any noise boosting and over equalization. In addition, the data rate is set below the OEIC receiver bandwidth to alleviate any BER degradation due to ISI effect. Fig. 4-19 shows the measured BER performance when 6-Gb/s broadband optical data are detected at P_{opt} of −8 and −10 dBm, respectively. The short-dashed lines in Fig. 4-19 show the estimated BER derived with the following equation:

$$\mathrm{BER} = \frac{1}{2} \cdot erfc\left(\frac{\alpha \cdot \mathrm{SNR}_{\mathrm{OEIC}}}{2\sqrt{2}} \right). \tag{4.11}$$

In Eq. (4.11), α represents signal penalties due to fiber dispersion, transmitter bandwidth, and experimental loss [55]. In this case, α is estimated to be 0.88 for both cases by fitting measured data to Eq. (4.11) with the minimum squared error function in MATLAB. As shown in Fig. 4-19, for P_{opt} of −10 dBm, the best BER performance can be achieved at V_R of about 12.0 V, corresponding to V_R having the highest SNR_{OEIC}. For P_{opt} of −8 dBm, the measured BER is equal to or less than 10^{-12} for V_R of from 11.6 V to 12.2 V.

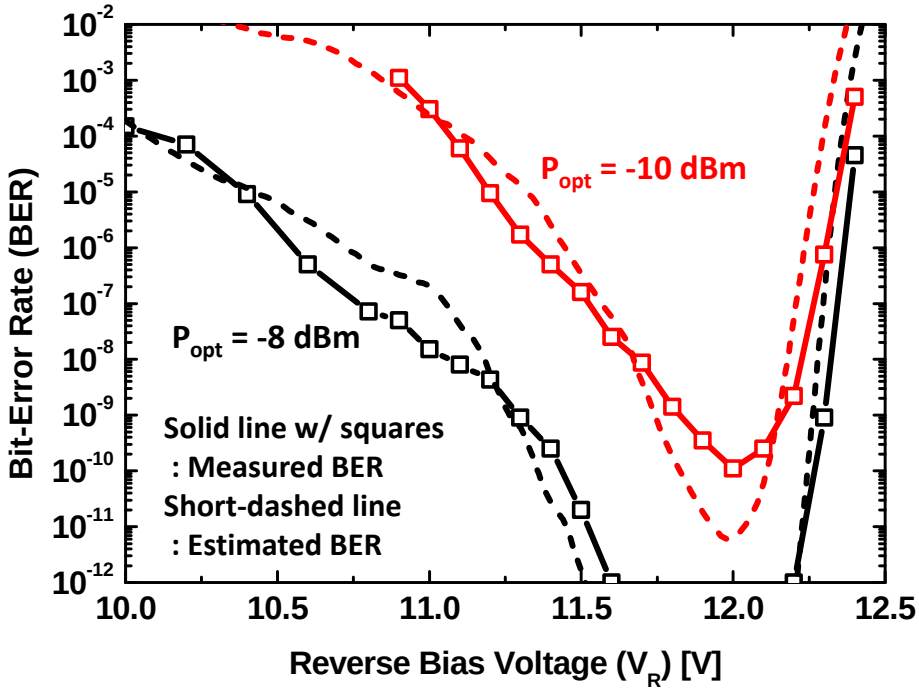


Fig. 4-19. Measured and estimated BER as a function of reverse bias voltage (V_R) at incident optical power (P_{opt}) of −8 and −10 dBm, respectively.

4-7. Summary

A 12.5-Gb/s OEIC receiver is realized with standard 0.25-μm SiGe BiCMOS technology for 850-nm optical interconnect applications. It consists of on-chip APD and BiCMOS circuits such as TIA, equalizer, and limiting amplifier. With the fabricated BiCMOS OEIC receiver, 12.5-Gb/s optical data transmission is successfully demonstrated with BER less than 10^{-12} at P_{opt} of −7 dBm. In addition, SNR characteristics of the OEIC receiver is investigated and verified. It is expected that the fabricated SiGe BiCMOS OEIC receiver shows the feasibility of cost-effective and high-speed 850-nm optical interconnect systems. Furthermore, this approach could be extended for 1.5-μm applications with the possibility of realizing of Ge PDs with SiGe BiCMOS technology. Table 4-1 summarizes chip design and demonstration results of the fabricated BiCMOS OEIC receiver. Table 4-2 compares performances with previously reported Si OEIC receiver.

Table 4-1
Performance summary of 12.5-Gb/s 850-nm BiCMOS OEIC receiver.

DESIGN RESULTS	
Technology	0.25-μm SiGe BiCMOS (f_T = 120 GHz)
Receiver Structure	APD+TIA+EQ+LA
Photodetector	P^+/N-well APD (10 μm × 10 μm)
Overall Transimpedance Gain	110 dBΩ
3-dB Bandwidth	8.4 GHz
Power Consumption (excluding output buffer)	59 mW at 2.5-V supply
Chip Area	1.0 mm × 0.28 mm
DEMONSTRATION RESULTS	
Maximum Data Rate	12.5-Gb/s
Sensitivity	−7 dBm
BER (PRBS)	10^{-12} (2^{31}-1)
Optimum APD Bias Voltage (V_{PD})	14.2 V (V_R = 12.0 V)
Power Efficiency	4.72 mW/Gb/s

Table 4-2
Performance comparison with Si OEIC receivers.

.

	[22] 05' JSSC	**[28] 10' TCAS1**	**[29] 10' JSSC**	**[30] 11' JSSC**	**This work (Chap. 4)**
Receiver Structure	N-well/P-sub PD+TIA+EQ	SML+TIA +EQ+LA	SML+TIA +EQ+LA	Meshed SML+TIA+LA (9 passive inductors)	**APD+TIA +EQ+LA**
Technology	0.18-μm CMOS	0.18-μm CMOS	0.13-μm CMOS	0.18-μm CMOS	**0.25-μm SiGe BiCMOS (f_T = 120 GHz)**
Maximum Data Rate	3 Gb/s	5 Gb/s	8.5 Gb/s	10 Gb/s	**12.5 Gb/s**
Sensitivity	-19 dBm	-3 dBm	-3.2 dBm	-6 dBm	**-7 dBm**
BER (PRBS)	10^{-11} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-11} (2^{7}-1)	**10^{-12} (2^{31}-1)**
Supply Voltage	1.8 V	3.3 V (PD/TIA) 1.8 V (Other circuits)	1.5 V	1.8 V (Circuit) 14.2 V (PD)	**2.5 V (Circuit) 14.2 V (PD)**
Power Consumption	34 mW	183 mW	47 mW	118 mW	**59 mW**
Power Efficiency	11.3 mW/Gbps	36.6 mW/Gbps	5.53 mW/Gbps	11.8 mW/Gbps	**4.72 mW/Gbps**
Chip Area	N/A	0.72 mm^2	0.1 mm^2	0.76 mm^2	**0.28 mm^2**

5. Power-Efficient 850-nm CMOS OEIC Receiver

5-1. CML- and CMOS-type TIA

For shunt-feedback TIA design, a core amplifier can be implemented in current-mode logic (CML) or CMOS-inverter logic configurations. Typically, CML-type TIA is preferred than CMOS-type TIA for high-speed operation. However, CML-type TIA dissipates larger power than CMOS-type TIA due to the large static currents. As CMOS technology scales down to deep sub-micron, the CMOS-type TIA is gaining popularity because it can provide high-speed operation with low-power consumption while maintaining high transimpedance gain [61], [62].

To evaluate performance of two types of TIAs, power consumption and 3-dB bandwidth are compared for achieving the same transimpedance gain with different CMOS technology nodes. Fig. 5-1 shows schematic diagrams of CML- and CMOS-type TIAs. The CML-type TIA is composed of a two-stage differential amplifier, a feedback resistance (R_F), and PD capacitance (C_{PD}). The CMOS-type TIA is composed of an inverter as a core amplifier, R_F, and C_{PD}. For both simulations, R_F and C_{PD} of 3 kΩ and 35 fF are used.

By varying transistor width, power consumption and 3-dB bandwidth

are simulated for two types of TIAs to achieve the same transimpedance gain of about 68 dBΩ. In addition, for CML-type TIA simulation, voltage swing and total power consumption are also set to the same values by changing load resistance (R_L) and tail current (I_{SS}), and the design parameters are listed in Table 5-1.

With simulation results, the power efficiency can be evaluated by dividing the power consumption with 3-dB bandwidth. Fig. 5-2 shows the resulting power efficiency for both types of the TIAs with different CMOS technology nodes. Although CML-type TIA has better power efficiency than CMOS-type TIA for above 0.13-μm CMOS process, power efficiency of CMOS-type TIA is rapidly improved in deep sub-micron technology. In 65-nm CMOS technology, the CMOS-type TIA achieves about five times better power efficiency than CML-type TIA.

Table 5-1
Design parameters and supply voltages

CMOS Tech.	**65 nm**	**90 nm**	**0.13 μm**	**0.18 μm**	**0.25 μm**
V_{DD}	1 V	1.2 V	1.2 V	1.8 V	2.5 V
R_L	300 Ω	350 Ω	350 Ω	550 Ω	750 Ω
I_{SS}	2 mA	1.7 mA	1.7 mA	1.1 mA	0.8 mA

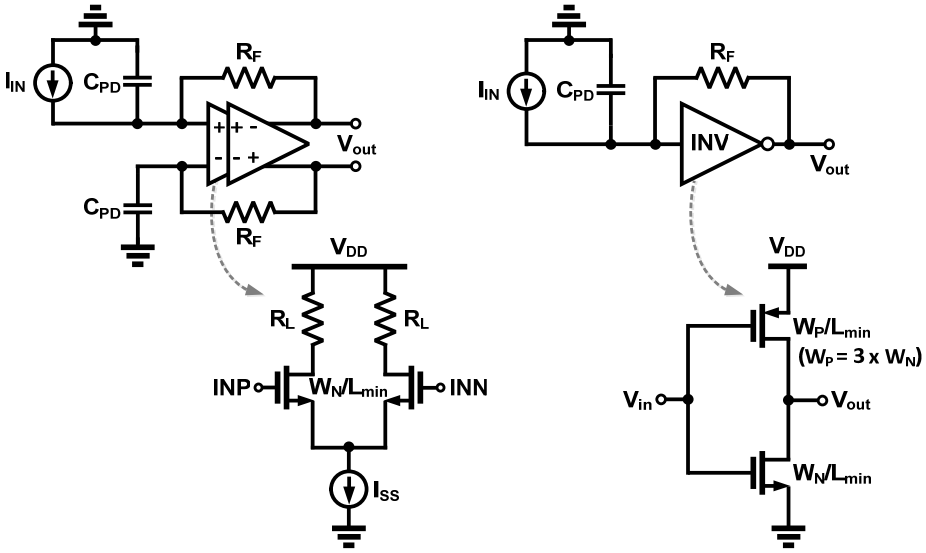


Fig. 5-1. Schematic diagrams of (a) CML- and (b) CMOS-type TIA.

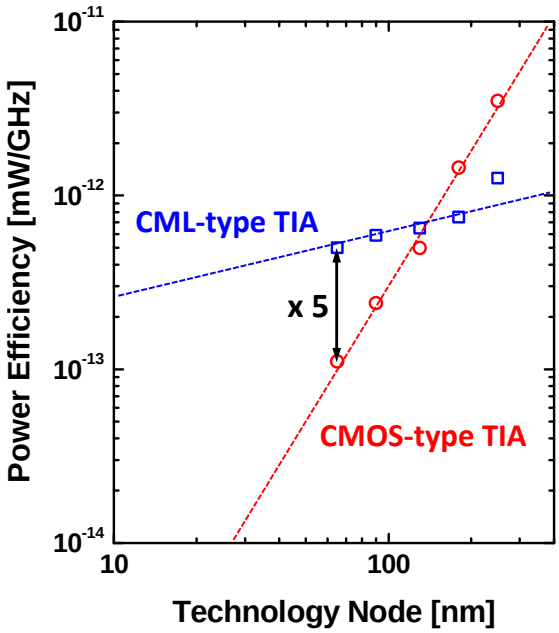


Fig. 5-2. Power efficiency comparison between CML- and CMOS-type TIAs with different CMOS technology nodes.

5-2. Overall Structure

Fig. 5-3 shows a simplified block diagram of the proposed 850-nm OEIC receiver. It is fabricated with standard 65-nm CMOS technology. The OEIC receiver is composed of APD and CMOS electronic circuits. The APD is realized P^+/N-well junction surrounded by shallow trench isolation, and its optical window is about 10 μm x 10 μm. The TIA is designed in single-ended configuration, and an on-chip low-dropout regulator provides 1-V supply to the TIA to alleviate supply noise. The single-ended signal at TIA output is converted to fully-differential signal by single-to-differential amplifier. The equalizer is used to compensate bandwidth limitation due to the APD and TIA, and the post amplifier provides additional gain and wide bandwidth. The limiter is used to satisfy input sensitivity of testing equipment and drive the output buffer. The output buffer is used for driving 50-Ω loads. In addition, the monitoring circuits using asynchronously under-sampled histogram [63] are added to observe on-chip signal amplitude and quality. The following chapter focuses on low-power circuit design and signal monitoring.

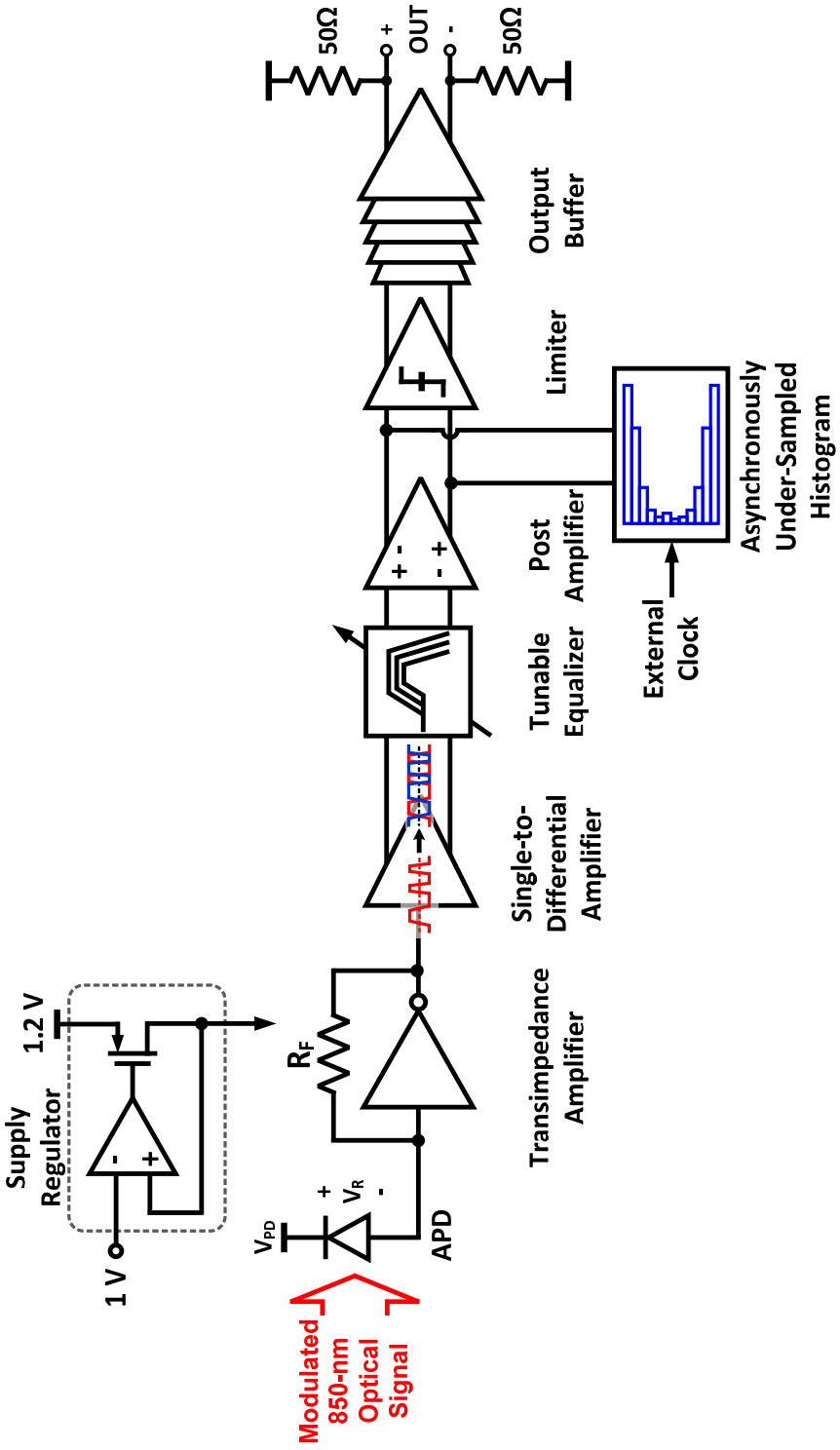


Fig. 5-3. Block diagram of the fabricated CMOS OEIC receiver.

5-3. Circuit Implementation

5-3-1. Inverter-Based Transimpedance Amplifier

In this work, TIA is designed in CMOS inverter-based configuration to achieve large bandwidth as well as low-power consumption. Fig. 5-4 shows a schematic diagram of inverter-based TIA, common-source amplifier, and additional circuits. The inverter-based TIA is composed of an inverter and a feedback resistance (R_F) of 3 kΩ.

In order to optimize inverter-based TIA performance, various design parameters such as transimpedance gain, 3-dB bandwidth, and power consumption are evaluated by changing NMOS and PMOS transistor width. The PMOS transistor width (W_{P1}) is three times larger than the NMOS transistor width (W_{N1}) to set common-mode voltage of $V_{DD}/2$. As expected, TIA power consumption increases with increasing transistor width. Fig. 5-5 shows the simulated transimpedance gain and 3-dB bandwidth of the TIA as a function of transistor width. The transimpedance gain of inverter-based TIA can be expressed as:

$$\text{Transimpedance Gain} \simeq -\frac{A_0}{A_0+1}\cdot R_F, \qquad (5.1)$$

where

$$A_0 \simeq -\left(g_{mn} + g_{mp}\right)\cdot\left(r_{on} \| r_{op}\right), \tag{5.2}$$

where g_{mn} and g_{mp} are NMOS and PMOS transconductance, and r_{on} and r_{op} are output resistance of NMOS and PMOS. As shown in Fig. 5-5, with increasing the W_{N1}, the transimpedance gain is gradually increased due to the increased A_0. The 3-dB bandwidth is maximized with W_{N1} of about 4 μm. For W_{N1} below 4 μm, the bandwidth is decreased due to insufficient intrinsic gain of the inverter. For W_{N1} above 4 μm, the bandwidth is also decreased due to the increased parasitic capacitance. In this work, W_{N1} of 6 μm is used to achieve high transimpedance gain as well as large bandwidth with low-power consumption. After the TIA, the common-source amplifier is used as a level shifter with additional gain, and degeneration technique is used to enhance bandwidth.

The 1-V supply voltage for the TIA and the additional circuits is provided by on-chip low-dropout regulator to achieve supply noise immunity. In addition, an error amplifier and a transistor M_{N3} are used to eliminate DC offset due to photodetector dark currents, amplifier offset, and DC component of the received signal [64]. The voltage difference between (+) node and (−) node of the error amplifier is integrated, and the output voltage of error amplifier controls the amount

of current flowing through M_{N3}. With these circuits, input voltage of the inverter-based TIA is always kept to $V_{DD}/2$.

Fig. 5-6 shows post-layout simulated frequency response and input-referred noise current at the amplifier output (V_{out}). The transimpedance gain is about 69 dBΩ. The 3-dB bandwidth with and without APD transit time effect are about 2.5 and 3.6 GHz, respectively. The simulated input-referred noise current density is about 4.2 pA/sqrt(Hz), and the calculated input-referred rms noise current is about 0.3 μA_{rms}.

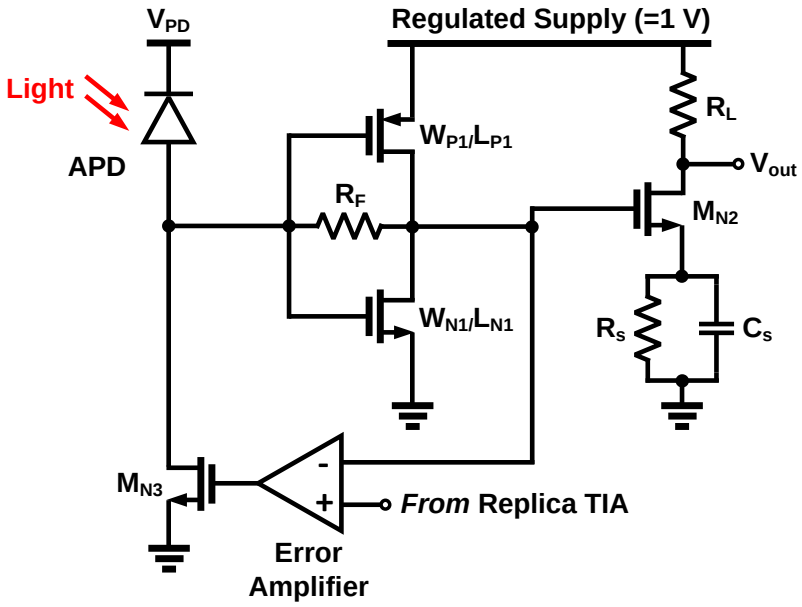


Fig. 5-4. Schematic diagrams of inverter-based TIA, common-source amplifier with degeneration, and additional circuits.

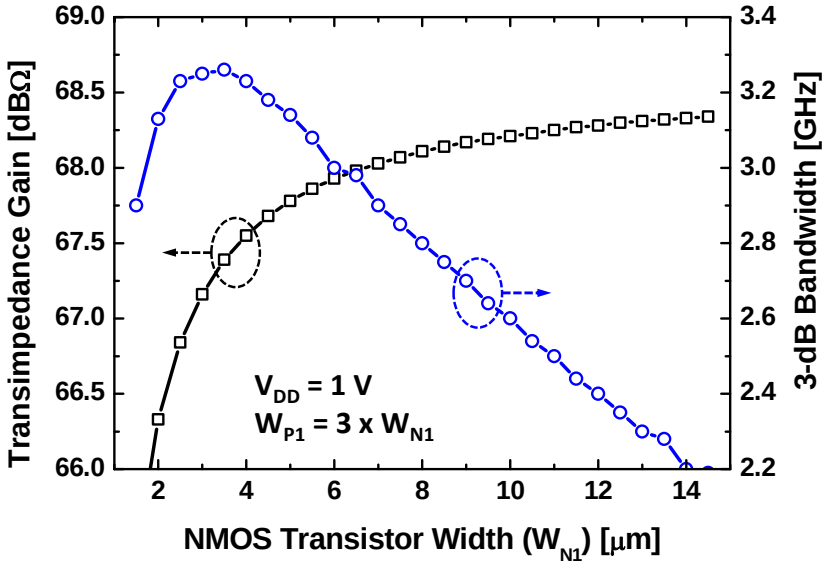


Fig. 5-5. Simulated transimpedance gain and 3-dB bandwidth of the inverter-based TIA with different transistor sizes.

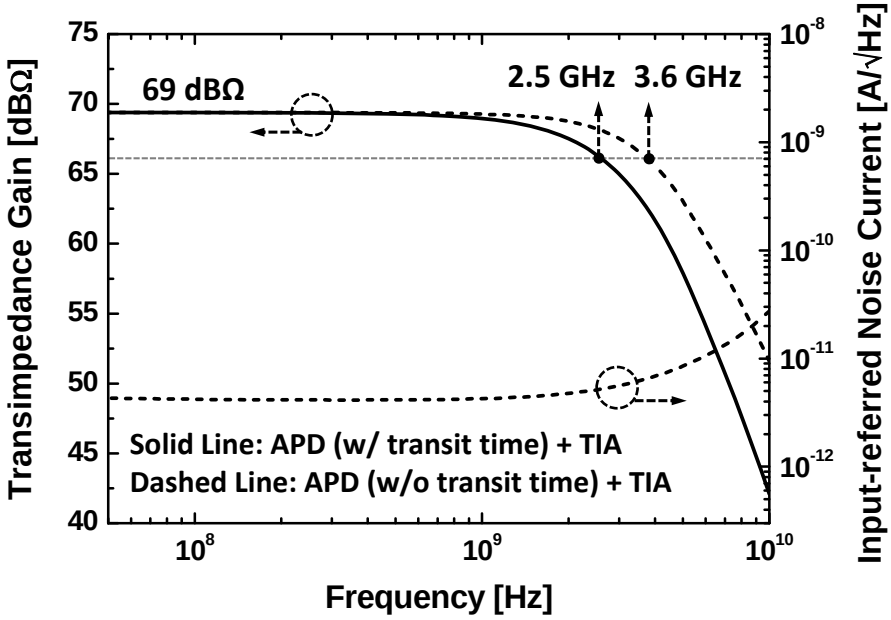


Fig. 5-6. Post-layout simulated frequency responses and input-referred noise current at the common-source amplifier output.

5-3-2. Equalizer and Post Amplifier

An equalizer circuit having high-pass filter characteristics is used to compensate the limited bandwidth due to APD and TIA. The equalizer consists of two-stage filter, and the each filter is designed in differential configuration with capacitive degeneration and negative capacitance as shown in Fig. 5-7. The value of C_{NC} in negative capacitance can be controlled by a capacitor array from nominally zero to about 44 fF. Fig. 5-8 shows a schematic diagram of post amplifier composed of two-stage differential amplifier with active feedback. It is used to provide additional gain to satisfy input sensitivity of the subsequent clock and data recovery circuit.

Fig. 5-9(a) shows the post-layout simulated frequency response at the equalizer output. With the equalizer, the 3-dB bandwidth is further enhanced up to 4.35 GHz without any frequency peaking, and therefore, the clean eye diagram can be achieved at the equalizer differential output as shown in Fig. 5-9(b). Fig. 5-9(a) shows the post-layout simulated frequency response at the post amplifier output, and overall transimpedance gain at the post amplifier output is about 83 dBΩ.

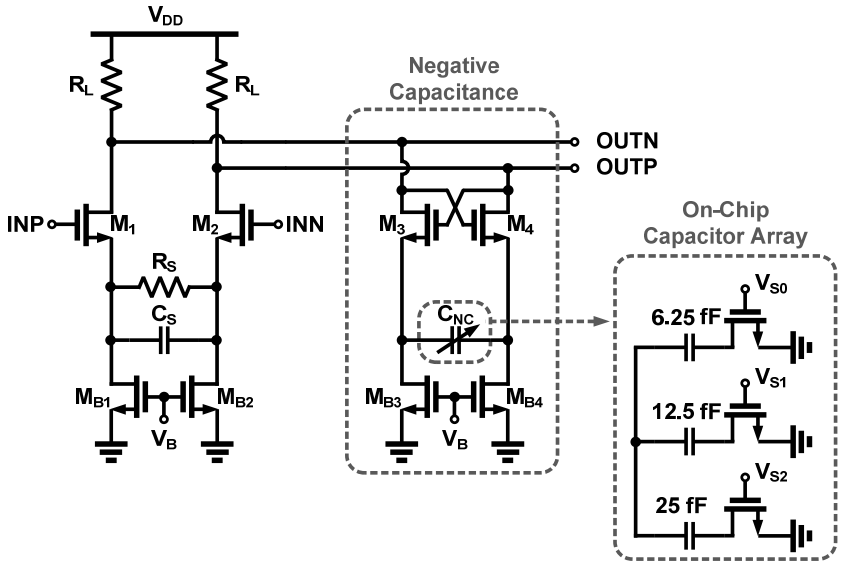


Fig. 5-7. Schematic diagram of equalizer with capacitor array.

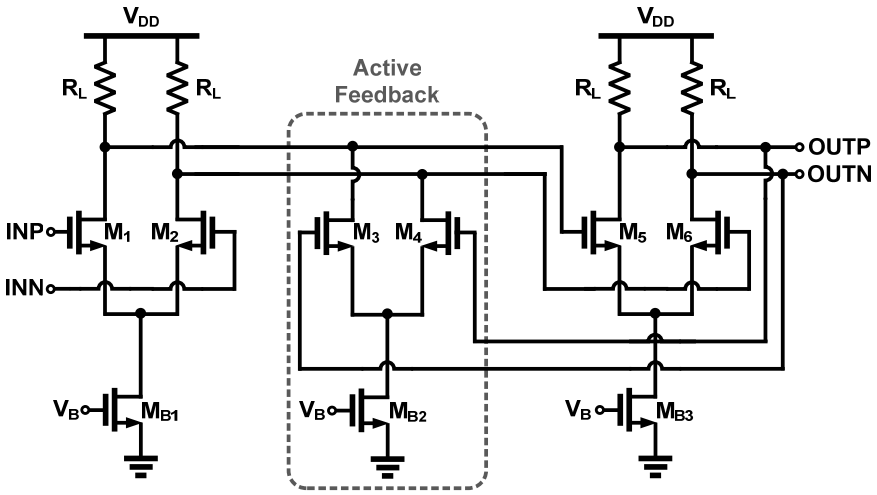


Fig. 5-8. Schematic diagram of post amplifier with active feedback.

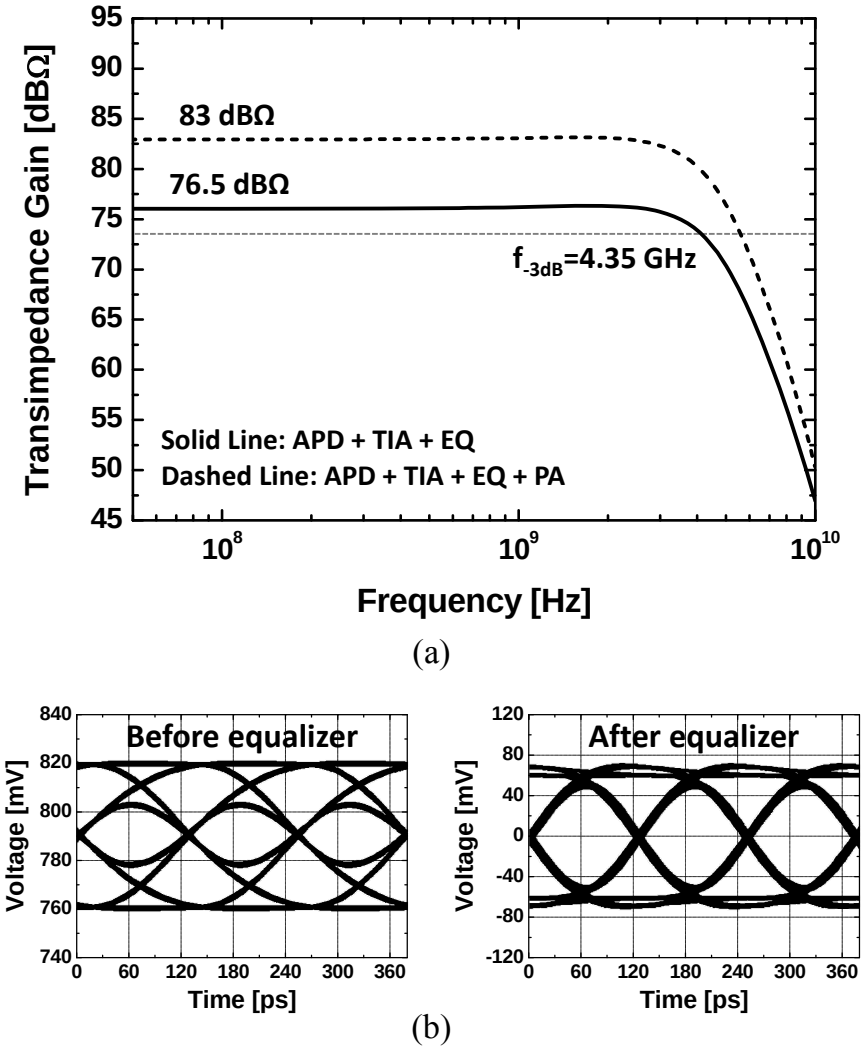


Fig. 5-9. Post-layout simulated (a) frequency responses at the output of equalizer (EQ) and post amplifier (PA) and (b) eye diagrams for differential signals before and after equalization.

5-3-3. On-Chip Signal Amplitude Monitoring Circuits

Fig. 5-10 shows a block diagram of asynchronously under-sampled histogram for monitoring the on-chip signal amplitude. It consists of an input buffer, four track-and-hold (T/H) circuits, a comparator, two digital-to-analog converters (DACs), and a four-phase clock generator. The input buffer is used to prevent clock feed-through problem from T/H circuits composed of pass-gate logic. The comparator is designed in four-input differentially strong arm latch [65], and it compares input PRBS signal with DAC reference voltages. The 4-bit DAC provides 16-level reference voltages from 0.8 V to 1.2 V with about 25-mV resolution. The clock generator provides four-phase clocks from an external clock. In order to extract histogram and control DAC reference voltages, the field-programmable gate array (FPGA) board is used.

Fig. 5-11(a) illustrates an asynchronously under-sampled histogram process. Firstly, the input signal is compared with different DAC reference voltages from V_{REF1} to V_{REFN}. If the V_{REF} is lower than input signal, the comparator output is high for all sampling points. However, with increasing V_{REF}, the comparator generates high or low because the case that V_{REF} is higher than input signal is gradually occurred. If the V_{REF} is completely higher than input signal, the comparator output is low for all sampling points. Fig. 5-11(b) shows the comparator outputs

for different DAC reference voltages. From these processes, cumulative distribution function can be obtained, and probability density function (PDF) can be calculated by differentiation as shown in Fig. 5-11(c). From the measured PDF histogram, on-chip signal amplitude can be estimated. The further details of circuit description and flowchart for histogram extraction can be found in [63].

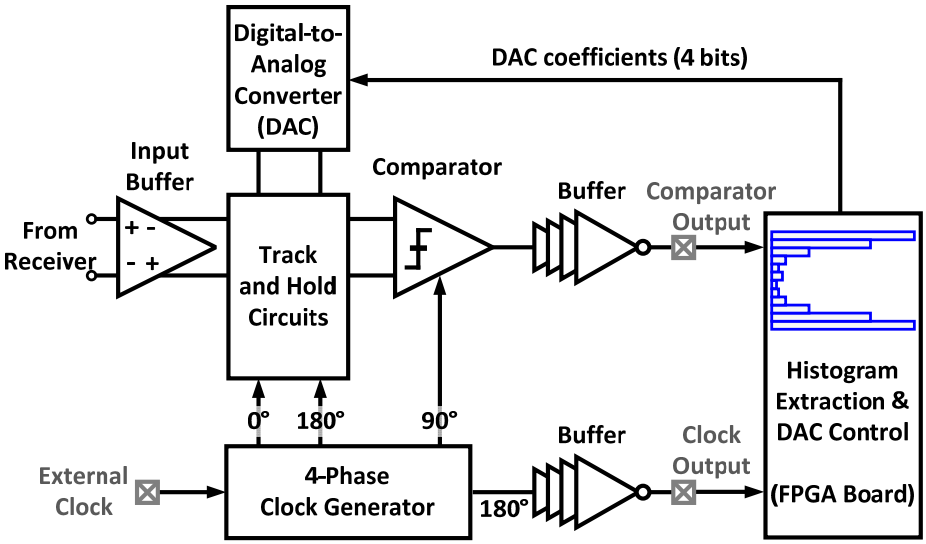
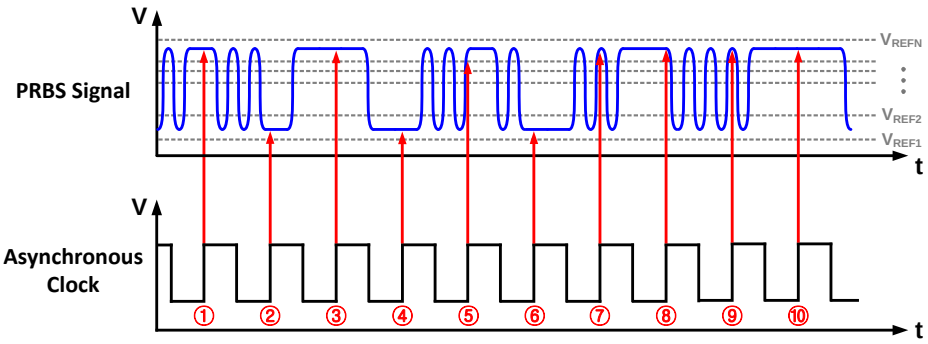


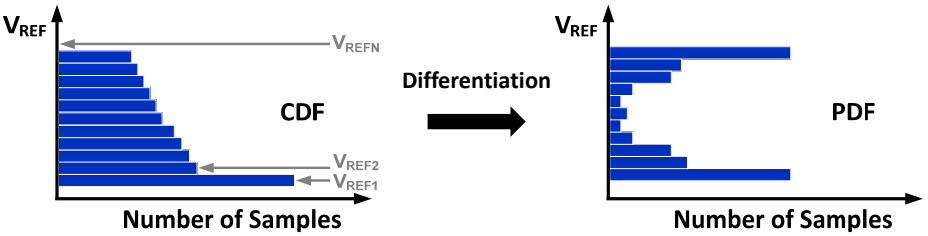
Fig. 5-10. Block diagram of asynchronously under-sampled histogram.



(a)

L : 0 H: 1	Comparator Output									
	①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩
V_{REFN}	L	L	L	L	L	L	L	L	L	L
⋮					⋮					
V_{REF2}	H	L	H	L	H	L	H	H	H	H
V_{REF1}	H	H	H	H	H	H	H	H	H	H

(b)



(c)

Fig. 5-11. (a) Asynchronous undersampling process (b) comparator output signal with different DAC reference voltages, and (c) obtained cumulative distribution function (CDF) and probability density function (PDF) histograms.

5-4. Experimental Results

Fig. 5-12 shows the chip photograph of the fabricated CMOS OEIC receiver. The chip area of receiver and monitoring circuit is about 0.58 mm × 0.36 mm. The power consumption excluding limiter and output buffer is about 5 mW with 1.2-V supply voltage. Fig. 5-13 shows the measurement setup for the OEIC receiver characterization, and all experiments are done on-wafer probing. An 850-nm laser diode and an external electro-optic modulator are used to generate the modulated optical signals. The modulated optical signals are transmitted through MMF and injected into the OEIC receiver using a lensed fiber. 2^{31}-1 PRBS signal generated by pulse pattern generator is used to measure BER performance. The reverse bias voltage (V_{PD}) of 10.2 V is applied to the N-well contact of APD for achieving optimal BER performance of the fabricated OEIC receiver. To observe on-chip signal amplitude and obtain histograms, the clock and comparator outputs are delivered to FPGA board, and DAC is also controlled by the FPGA board.

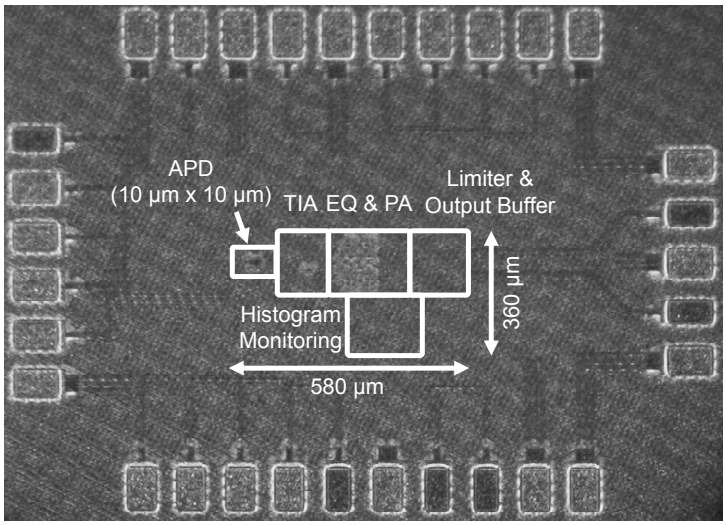


Fig. 5-12. Chip photograph of the fabricated CMOS OEIC receiver.

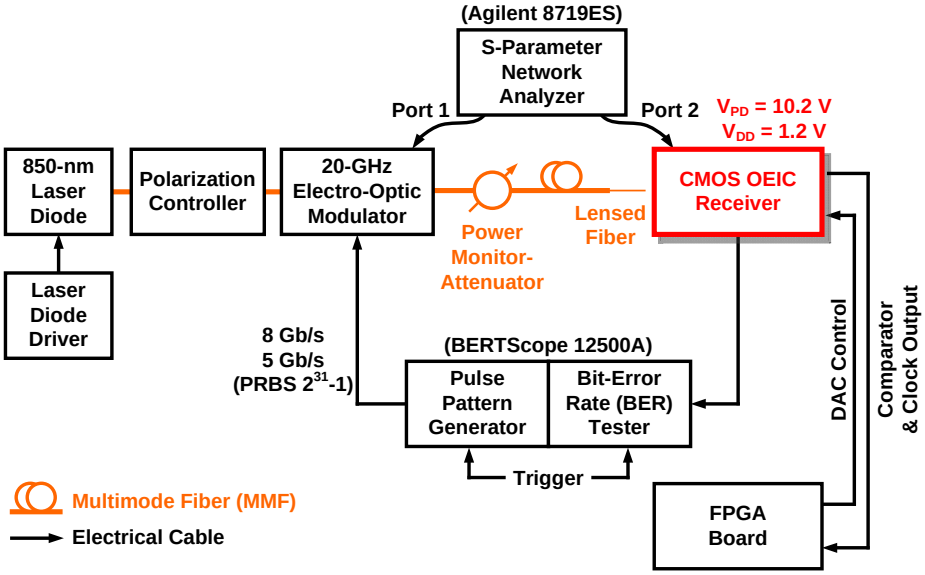


Fig. 5-13. Measurement Setup.

Fig. 5-14 shows the measured photodetection frequency response. The measured overall transimpedance gain and 3-dB bandwidth of the fabricated OEIC receiver are about 95 dBΩ and 3.3 GHz, respectively. Fig. 5-15 shows the measured BER performance versus P_{opt} for 5-Gb/s and 8-Gb/s optical data transmission. The measured optical sensitivities for BER less than 10^{-12} are −7 dBm and −4.5 dBm for 5 Gb/s and 8 Gb/s, respectively. Fig. 5-16 shows the measured eye diagrams for differential signals and histograms for 5-Gb/s and 8-Gb/s optical data with P_{opt} of −7 dBm and −4.5 dBm, respectively. From the measured PDF histogram, it can be observed that on-chip single-ended signal amplitude is about 275 mV_{pp} for both cases. In addition, the largest peak value of the histogram is decreased with increasing data rate due to the increased ISI effect.

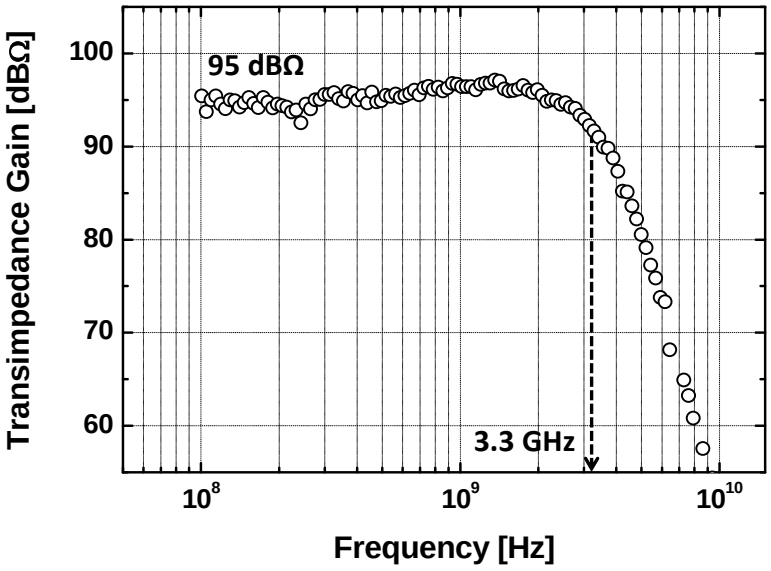


Fig. 5-14. Measured photodetection frequency response of the fabricated CMOS OEIC receiver.

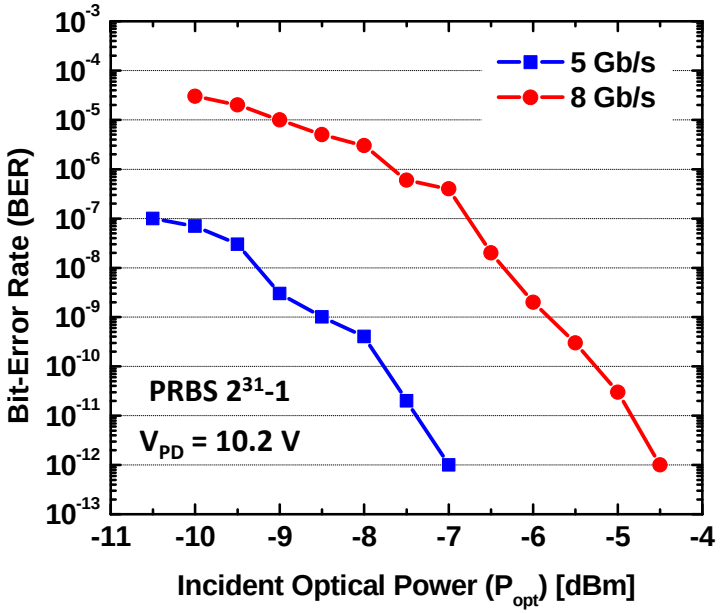


Fig. 5-15. Measured BER performance as a function of incident optical power (P_{opt}).

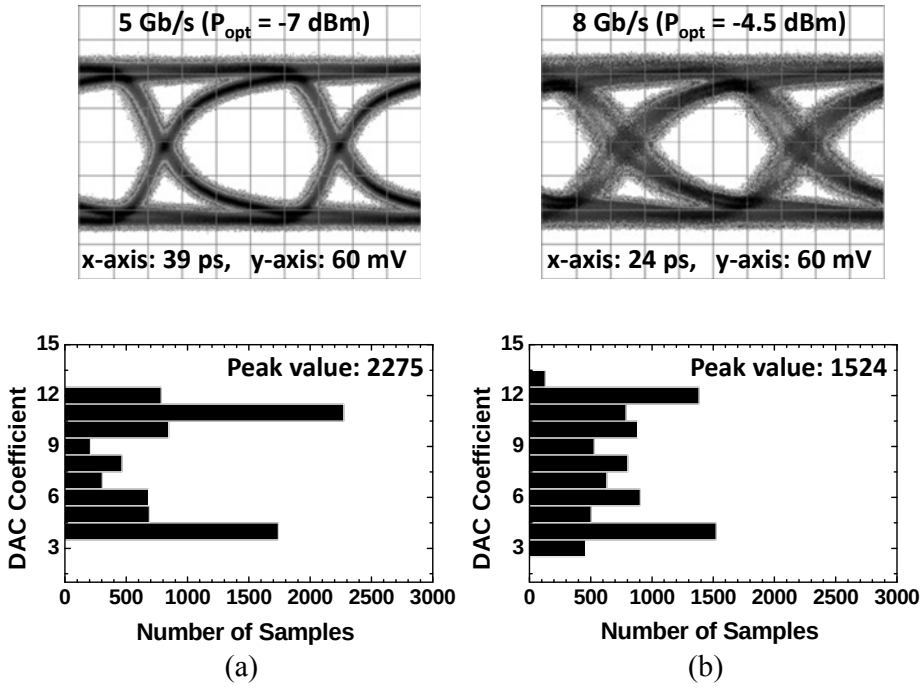


Fig. 5-16. Measured eye diagrams for differential signals and histograms of (a) 5 Gb/s and (b) 8 Gb/s at incident optical power (P_{opt}) of −7 and −4.5 dBm, respectively.

5-5. Summary

A power-efficient OEIC receiver is realized with standard 65-nm CMOS technology. The OEIC receiver is composed of on-chip APD, inverter-based TIA, equalizer, post amplifier, limiter and output buffer. To improve power efficiency of the OEIC receiver, TIA is designed in inverter-based configuration, and its performance is further improved with optimizing transistor size. With the fabricated CMOS OEIC receiver, 8-Gb/s optical data transmission is successfully demonstrated with BER less than 10^{-12} at incident optical power of −4.5 dBm. In addition, on-chip signal can be observed with asynchronously under-sampled histogram. From this, on-chip signal amplitude and quality can be evaluated. It is expected that the CMOS OEIC receiver is promising solution for cost-effective and power-efficient 850-nm optical interconnect applications. Table 5-2 summarizes chip design and demonstration results of the fabricated CMOS OEIC receiver. Table 5-3 shows the performance comparison with previously reported Si OEIC receivers.

Table 5-2
Performance summary of 8-Gb/s 850-nm CMOS OEIC receiver.

DESIGN RESULTS	
Technology	65-nm CMOS
Receiver Structure	APD+TIA+EQ+LA +Monitoring Circuits
Photodetector	P^+/N-well APD (10 μm × 10 μm)
Overall Transimpedance Gain	95 dBΩ
3-dB Bandwidth	3.3 GHz
Power Consumption (w/o limiter and output buffer)	5 mW at 1.2-V supply
Chip Area	0.58 mm × 0.36 mm
DEMONSTRATION RESULTS	
Maximum Data Rate	8 Gb/s
Sensitivity	−4.5 dBm
BER (PRBS)	10^{-12} (2^{31}-1)
Optimum APD Bias Voltage (V_{PD})	10.2 V
Power Efficiency	0.63 mW/Gb/s

Table 5-3
Performance comparison with Si OEIC receivers.

.

	[22] 05' JSSC	**[28] 10' TCAS1**	**[29] 10' JSSC**	**[30] 11' JSSC**	**This work (Chap. 5)**
Receiver Structure	N-well/P-sub PD+TIA+EQ	SML+TIA +EQ+LA	SML+TIA +EQ+LA	Meshed SML+TIA+LA (9 passive inductors)	**APD+TIA +EQ+PA**
Technology	0.18-µm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.18-µm CMOS	**65-nm CMOS**
Maximum Data Rate	3 Gb/s	5 Gb/s	8.5 Gb/s	10 Gb/s	**8 Gb/s**
Sensitivity	-19 dBm	-3 dBm	-3.2 dBm	-6 dBm	**-4.5 dBm**
BER (PRBS)	10^{-11} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-11} (2^{7}-1)	**10^{-12} (2^{31}-1)**
Supply Voltage	1.8 V	3.3 V (PD/TIA) 1.8 V (Other circuits)	1.5 V	1.8 V (Circuit) 14.2 V (PD)	**1.2 V (Circuit) 10.2 V (PD)**
Power Consumption	34 mW	183 mW	47 mW	118 mW	**5 mW**
Power Efficiency	11.3 mW/Gbps	36.6 mW/Gbps	5.53 mW/Gbps	11.8 mW/Gbps	**0.63 mW/Gbps**
Chip Area	N/A	0.72 mm^2	0.1 mm^2	0.76 mm^2	**0.2 mm^2**

6. Conclusions and Discussions

6-1. Conclusions

In this dissertation, high-speed and power-efficient OEIC receivers are realized in standard CMOS/BiCMOS technology for 850-nm short-distance optical interconnect applications. In these OEIC receivers, silicon APD is monolithically integrated with electronic circuits such as TIA, equalizer, and limiting amplifier, and etc.

To develop high-performance Si OEIC receivers, both characteristics of APD and electronic circuits are investigated. Firstly, DC, photodetection frequency response, and SNR characteristics of APD are investigated, and an APD equivalent circuit model is also developed. The APD characteristics and model can provide useful information for circuit design optimization. Secondly, various circuit topologies of TIA, equalizer, and limiting amplifier are compared and investigated. With these, electronic circuits are carefully designed, and consequently, high-speed, low-noise and power-efficient circuits can be realized. Finally, SNR characteristics of entire OEIC receiver are investigated, and this result is verified by BER measurement.

Table 6-1
Performance summary of the fabricated Si OEIC receivers.

.

	This work (Chap. 3)	**This work (Chap. 4)**	**This work (Chap. 5)**
Receiver Structure	APD+TIA +EQ+LA	APD+TIA +EQ+LA	APD+TIA +EQ+PA
Technology	0.13-μm CMOS	0.25-μm SiGe BiCMOS (f_T = 120 GHz)	65-nm CMOS
Maximum Data Rate	10 Gb/s	12.5 Gb/s	8 Gb/s
Sensitivity	-4 dBm	-7 dBm	-4.5 dBm
BER (PRBS)	10^{-12} (2^7-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{31}-1)
Supply Voltage	1.2 V (Circuit) 10.5 V (PD)	2.5 V (Circuit) 14.2 V (PD)	1.2 V (Circuit) 10.2 V (PD)
Power Consumption	66.8 mW	59 mW	5 mW
Power Efficiency	6.68 mW/Gb/s	4.72 mW/Gb/s	0.63 mW/Gb/s
Chip Area	0.26 mm^2	0.28 mm^2	0.2 mm^2

Table 6-1 summarizes the performance of the fabricated 850-nm Si OEIC receivers. These OEIC receivers are composed of APD, TIA, EQ, and LA (or PA), and it is realized with small chip area. As can be seen, the measured sensitivities are about −4 dBm at maximum data rate. The BiCMOS receiver has better sensitivity because its receiver bandwidth is enough to detect 12.5-Gb/s optical data. In other word, it is expected that above 12.5-Gb/s optical data can be detected with sensitivity of about −4 dBm. However, it didn't measure due to equipment limitation.

Table 6-2

Performance comparison with Si OEIC receivers.

.

	[22] 05' JSSC	[28] 10' TCAS1	[29] 10' JSSC	[30] 11' JSSC	This work (Chap. 3)	This work (Chap. 4)	This work (Chap. 5)
Receiver Structure	N-well/P-sub PD+TIA+EQ	SML+TIA +EQ+LA	SML+TIA +EQ+LA	Meshed SML+TIA+LA (9 passive inductors)	**APD+TIA +EQ+LA**	**APD+TIA +EQ+LA**	**APD+TIA +EQ+PA**
Technology	0.18-µm CMOS	0.18-µm CMOS	0.13-µm CMOS	0.18-µm CMOS	**0.13-µm CMOS**	**0.25-µm SiGe BiCMOS (f_T = 120 GHz)**	**65-nm CMOS**
Maximum Data Rate	3 Gb/s	5 Gb/s	8.5 Gb/s	10 Gb/s	**10 Gb/s**	**12.5 Gb/s**	**8 Gb/s**
Sensitivity	-19 dBm	-3 dBm	-3.2 dBm	-6 dBm	**-4 dBm**	**-7 dBm**	**-4.5 dBm**
BER (PRBS)	10^{-11} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-12} (2^{31}-1)	10^{-11} (2^{7}-1)	**10^{-12} (2^{7}-1)**	**10^{-12} (2^{31}-1)**	**10^{-12} (2^{31}-1)**
Supply Voltage	1.8 V	3.3 V (PD/TIA) 1.8 V (Other circuits)	1.5 V	1.8 V (Circuit) 14.2 V (PD)	**1.2 V (Circuit) 10.5 V (PD)**	**2.5 V (Circuit) 14.2 V (PD)**	**1.2 V (Circuit) 10.2 V (PD)**
Power Consumption	34 mW	183 mW	47 mW	118 mW	**66.8 mW**	**59 mW**	**5 mW**
Power Efficiency	11.3 mW/Gbps	36.6 mW/Gbps	5.53 mW/Gbps	11.8 mW/Gbps	**6.68 mW/Gbps**	**4.72 mW/Gbps**	**0.63 mW/Gbps**
Chip Area	N/A	0.72 mm^2	0.1 mm^2	0.76 mm^2	**0.26 mm^2**	**0.28 mm^2**	**0.2 mm^2**

Table 6-2 compares recently reported 850-nm Si OEIC receivers fabricated with standard CMOS/BiCMOS technology. These OEIC receivers achieve 10-Gb/s and 12.5-Gb/s operation with better sensitivity, smaller power consumption than previously reported results. Fig. 6-1 shows the power efficiency comparison of 850-nm Si OEIC receivers. As can be seen, the OEIC receiver achieves the best power-efficiency among Si OEIC receivers reported until now. It is expected that the fabricated OEIC receivers can play an important role for cost-effective, high-speed and power-efficient 850-nm optical interconnect systems.

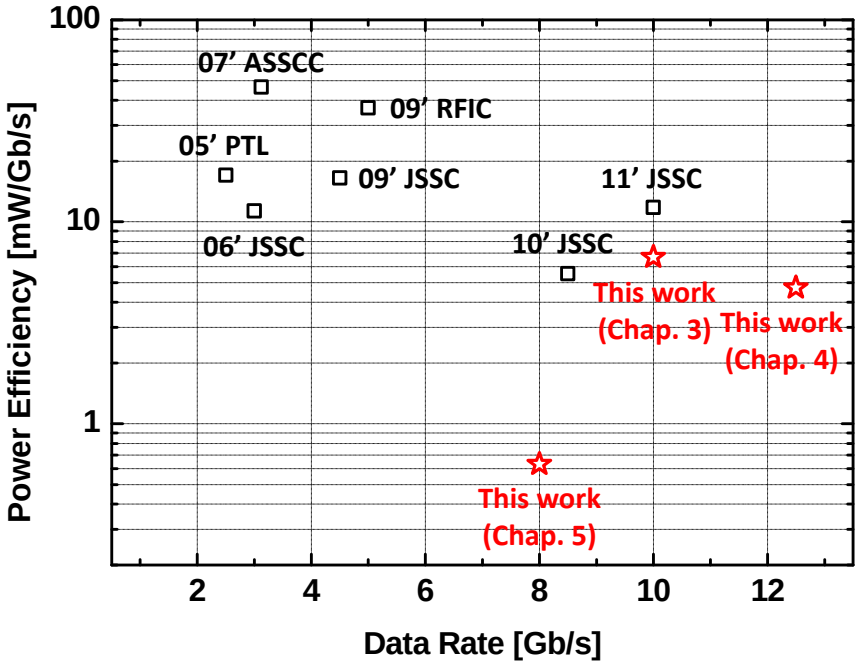


Fig. 6-1. Power efficiency comparison of recently reported 850-nm OEIC receivers fabricated with standard CMOS/BiCMOS technology.

6-2. Discussions

6-2-1. Compensation of APD Performance Variation

Due to process and temperature variation, APD characteristics such avalanche gain, noise and bandwidth can be changed, and it can affect receiver performance degradation. In order to compensate these variations, some circuits are required and integrated in OEIC receiver. Among them, the bandwidth variation can be easily compensated using tunable equalizer circuits, and they are included in the fabricated OEIC receivers.

The most intuitive way to compensate APD gain and noise variation is controlling APD bias voltage with monitoring circuits. For this purpose, the histogram monitoring circuits are included in the OEIC receiver discussed in chapter 5. With these, signal amplitude variation is detected, however, noise effects didn't included in histogram since APD noise characteristic is random. Although APD noise effects can be included in histogram with increasing DAC resolution and number of sample, it increases hardware complexity and costs. It is expected that APD gain and noise variations can be detected by using on-chip BER tester, and furthermore, APD bias adaptation can be also achieved by using on-chip DC-DC converter [66].

6-2-2. Comparison of Various Types of TIA Structures

In this section, the most widely used TIA structures are compared. Fig. 6-2 illustrates three types of TIA configurations: shunt-feedback, common-gate, and regulated cascode TIA.

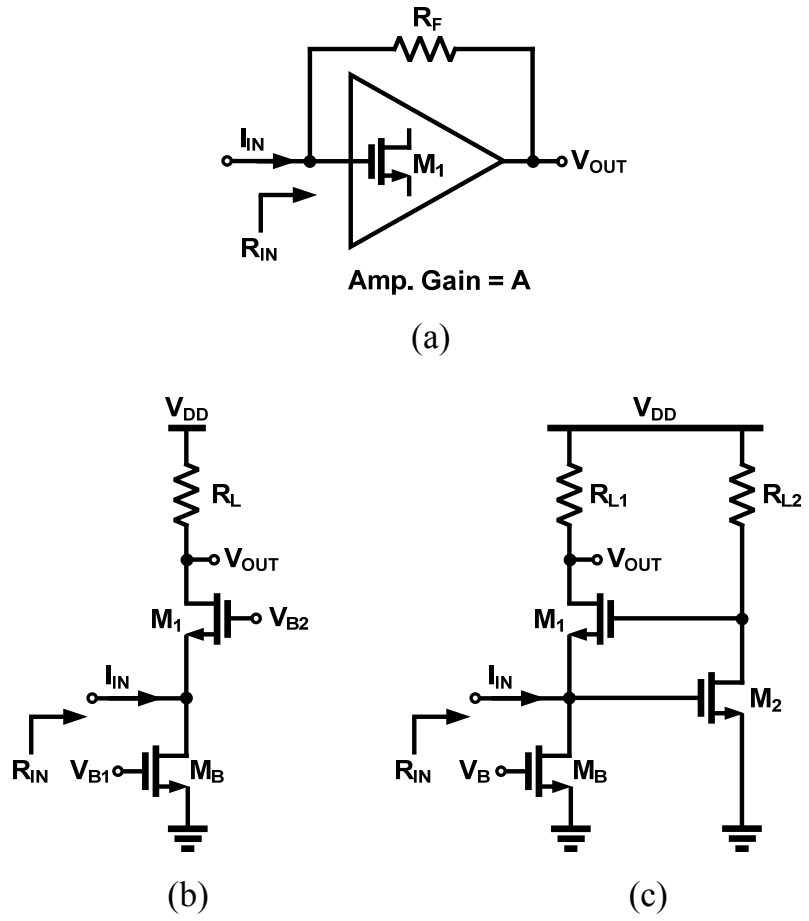


Fig. 6-2. Schematic diagrams of TIA structures (a) shunt-feedback (b) common-gate, and (c) regulated cascode.

Table 6-3
Performance summary of three types of TIA structures.

TIA Structure	**Input Impedance**	**Dominant Noise source**
Shunt Feedback	$R_F/(1+A)$	Input transistor (M_1) of core amplifier
Common-gate	$1/g_{m1}$	Common-gate transistor (M_1)
Regulated Cascode (RGC)	$1/[g_{m1}\times(1+g_{m2}R_{L2})]$	Transistor (M_2)

Table 6-3 summarizes input impedance and dominant noise source for these TIA structures, and equation (6.1)–(6.3) show input-referred noise currents generated by the dominant noise source, respectively.

$$\overline{i_{n,M1,\text{Shunt-FB}}^2}(f) \cong 4kT\Gamma g_{d0,m1}\cdot\frac{1}{g_{m1}^2}\cdot\left(\frac{1}{R_F^2}+\omega^2 C_T^2\right), \qquad (6.1)$$

$$\overline{i_{n,M1,\text{Common-gate}}^2}(f) \cong 4kT\Gamma g_{d0,m1}\cdot\frac{1}{g_{m1}^2}\cdot\left(\omega^2 C_T^2\right), \qquad (6.2)$$

$$\overline{i_{n,M2,\text{RGC}}^2}(f) \cong 4kT\Gamma g_{d0,m2}\cdot\frac{1}{\left(g_{mB}+1/R_B\right)^2}\cdot\left(\omega^2 C_T^2\right), \qquad (6.3)$$

where k is Boltzmann's constant, T is the absolute temperature, Γ is the channel noise factor in MOSFET, g_{d0} is the zero-bias drain conductance, g_m is the transconductance, and C_T is total parasitic capacitance due to transistors and photodetector.

The shunt-feedback TIA having simple structure can provide better noise performance than other TIA configurations [41], however, its bandwidth can be limited due to large input impedance. In order to overcome the bandwidth limitation, the common-gate TIA and regulated cascode TIA having lower input impedance have been investigated, and their noise performance can be comparable to the shunt-feedback TIA by determining g_m, load resistance, and bias currents appropriately [44], [67]. However, their noise characteristics can be deteriorated due to additional transistors and components. In addition, they can suffer from voltage headroom. It is expected that the optimized common-gate and regulated cascode TIAs without voltage headroom problem can provide performance improvement for APD-based OEIC receiver.

Bibliography

[1] H. Cho, P. Kapur, and K. C. Sarawat, “Power comparison between high-speed electrical and optical interconnect for interchip communication,” *J. Lightw. Technol.*, vol. 22, no. 9, pp. 2021–2033, Sep. 2004.

[2] E. Mohammed, A. Alduino, T. Thomas, H. Braunisch, D. Lu, J. Heck, A. Liu, I. Young, B. Barnett, G. Vandentop, and R. Mooney, “Optical interconnect system integration for ultra-short-reach applications,” *Intel Technol. J.*, vol. 8, no. 2, pp. 115–127, May 2004.

[3] D. M. Kuchta, Y. H. Kwark, C. Schuster, C. Baks, C. Haymes, J. Schuab, P. Pepeljugoski, L. Shan, R. John, D. Kucharski, D. Rogers, M. Ritter, J. Jewell, L. A. Graham, K. Schrödinger, A. Schild, and H.-M. Rein, “120-Gb/s VCSEL-based parallel-optical interconnect and custom 120-Gb/s testing station,” *J. Lightw. Technol.* vol. 22, no. 9, pp. 2200–2212, Sep. 2004.

[4] T. Takemoto, H. Yamashita, T. Yazaki, N. Chujo, Y. Lee, and Y. Matsuoka, “A 4 × 25-to-28Gb/s 4.9mW/Gb/s –9.7dBm high-sensitivity optical receiver based on 65nm CMOS for board-to-board interconnects,” *ISSCC Dig. Tech. Papers*, pp. 118–119, Feb. 2013.

[5] N. Chujo, T. Yazaki, T. Takai, D. Kawamura, Y. Matsuoka, Y. Lee, T. Sugawara, H. Yamashita, T. Takemoto, Y. Ishigami, K. Yamazaki, Y. Sunaga, and N. Matsushima, “A 25-Gb/s × 4-Ch, 8 × 8 mm^2, 2.8-mm thick compact optical transceiver module for on-board optical interconnect,” *OFC/NFOEC,* JW2A, Mar. 2013.

[6] J. W. Goodman, F. J. Leonberger, S.-Y. Kung, and R. A. Athale, “Optical interconnections for VLSI systems,” *Proc. IEEE*, vol. 72, no. 7, pp. 850–866, Jul. 1984.

[7] D. A. B. Miller, “Rationale and challenges for optical interconnects to electronic chips,” *Proc. IEEE*, vol. 88, no. 6, pp. 728–749, Jun. 2000.

[8] D. A. B. Miller, “Device requirements for optical interconnects to silicon chips,” *Proc. IEEE*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.

[9] I. A. Young, E. Mohammed, J. T. S. Liao, A. M. Kern, S. Palermo, B. A. Block, M. R. Reshotko, and P. L. D. Chang, “Optical I/O technology for tera-scale computing,” *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 235–248, Jan. 2010.

[10] http://engineering.ucsb.edu/bowers/presentation.php, M. Paniccia, “First electrically pumped hybrid silicon laser.ppt,” Oct. 2006.

[11] N. Bamiedakis, J. Beals, R. V. Penty, I. H. White, J. V. DeGroot, and T. V. Clapp, “Cost-effective multimode polymer waveguides for high-speed on-board optical interconnect,” *IEEE J. Quantum Electron.*, vol. 45, no. 4, pp. 415–424, Apr. 2009.

[12] C. Gunn, “CMOS photonics for high-speed interconnects” *IEEE Micro.,* vol. 26, no. 2, pp. 58–66, Mar./Apr. 2006.

[13] M. Hochberg, N. C. Harris, R. Ding, Y. Zhang, A. Novack, Z. Xuan, and T. Baehr-Jones, “Silicon photonics: The next fabless semiconductor industry,” *IEEE Solid-State Circuits Mag.*, vol. 5, no. 1, pp. 48–58, Mar. 2013.

[14] S. Assefa, F. Xia, and Y. A. Vlasov, “Reinventing germanium avalanche photodetector for nanophotonic on-chip optical interconnects,” *Nature*, vol. 464, no. 7285, pp. 80–84, Mar. 2010.

[15] http://web.eecs.utk.edu/~dongarra/ccgsc2006/Slides/, “Talk2: David Scott.ppt”.

[16] L. Schares, J. A. Kash, F. E. Doany, C. L. Schow, C. Schuster, D. M. Kuchta, P. K. Pepeljugoski, J. M. Trewhella, C. W. Baks, R. A. John, L. Shan, Y. H. Kwark, R. A. Budd, P. Chiniwalla, F. R. Libsch, J. Rosner, C. K. Tsang, C. S. Patel, J. D. Schaub, R. Dangel, F. Horst, B. J. Offrein, D. Kucharski, D. Guckenberger, S. Hegde, H. Nyikal, C.-K. Lin, A. Tandon, G. R. Trott, M. Nystrom, D. P. Bour, M. R. T. Tan, and D. W. Dolfi, "Terabus: Terabit/second-class card-level optical interconnect technologies," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 5, pp. 1032–1044, Sep./Oct. 2006.

[17] A. C. Carusone, H. Yasotharan, and T. Kao, "CMOS technology scaling considerations for multi-gbps optical receivers with integrated photodetectors," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, Aug. 2011.

[18] Y. Dong and K. W. Martin, "A high-speed fully-integrated POF receiver with large-area photo detectors in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2080–2092, Sep. 2012.

[19] T.-K. Woodward and A. V. Krishnamoorthy, "1-Gb/s integrated optical detectors and receivers in commercial CMOS technologies," *IEEE J. Sel. Topics Quantum Electron.*, vol. 5, no. 2, pp. 146–156, Mar./Apr. 1999.

[20] A. Nemecek, G. Zach, R. Swoboda, K. Oberhauser, and H. Zimmermann, "Integrated BiCMOS p-i-n photodetectors with high bandwidth and high responsivity," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1469–1475, Nov./Dec. 2006.

[21] B. Yang, J. D. Schaub, S. M. Csutak, D. L. Rogers, and J. C. Campbell, "10-Gb/s all-silicon optical receiver," *IEEE Photon. Technol. Lett.*, vol. 15, no. 5, pp. 745–747, May 2003.

[22] S. Radovanovic, A.-J. Annema, and B. Nauta, "A 3-Gb/s optical detector in standard CMOS for 850-nm optical communication,"

IEEE J. Solid-State Circuits, vol. 40, no. 8, pp. 1706–1717, Aug. 2005.

[23] M.-J. Lee and W.-Y. Choi, "Performance comparison of two types of silicon avalanche photodetectors based on N-well/P-substrate and P^+/N-well junctions fabricated with standard CMOS technology," *J. Opt. Society Korea*, vol. 15, no. 1, pp. 1–3, Mar. 2011.

[24] C. Rooman, D. Coppee, and M. Kuijk, "Asynchronous 250-Mb/s optical receivers with integrated detector in standard CMOS technology for optocoupler application," *IEEE J. Solid-State Circuits*, vol. 35, no. 7, pp. 953–958, Jul. 2000.

[25] M. Jutzi, M. Grözing, E. Gaugler, W. Mazioschek, and M. Berroth, "2-Gb/s CMOS optical integrated receiver with a spatially modulated photodetector," *IEEE Photon. Technol. Lett.*, vol. 17, no. 6, pp. 1268–1270, Jun. 2005.

[26] W.-Z. Chen, S.-H. Huang, G.-W. Wu, C.-C. Liu, Y.-T. Huang, C.-F. Chiu, W.-H. Chang, and Y.-Z. Juang, "A 3.125 Gbps CMOS fully integrated optical receiver with adaptive analog equalizer," in *Proc. Asian Solid-State Circuits Conf.*, pp. 396–399, Nov. 2007.

[27] F. Tavernier, M. Steyaert, "High-speed optical receives with integrated photodiode in 130 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2856–2867, Oct. 2009.

[28] T. S. Kao, F. A. Musa, and A. C. Carusone, "A 5-Gbit/s CMOS optical receiver with integrated spatially modulated light detector and equalization," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 11, pp. 2844–2857, Nov. 2010.

[29] D. Lee, J. Han, G. Han, and S. M. Park, "An 8.5-Gb/s fully integrated CMOS optoelectronic receiver using slope-detection

adaptive equalizer," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2861–2873, Dec. 2010.

[30] S.-H. Huang, W.-Z. Chen, Y.-W. Chang, and Y.-T. Huang, "A 10-Gb/s OEIC with meshed spatially-modulated photo detector in 0.18-μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1158–1169, May 2011.

[31] W.-Z. Chen and S.-H. Huang, "A 2.5 Gbps CMOS fully integrated optical receiver with lateral PIN detector," in *Proc. IEEE Custom Integrated Circuits Conf.*, pp. 293–296, Sep. 2007.

[32] H.-S. Kang, M.-J. Lee, and W.-Y. choi, "Si avalanche photodetectors fabricated in standard complementary metal-oxide-semiconductor process," *Appl. Phys. Lett.*, vol. 90, no. 15, pp. 151118-1–151118-3, Apr. 2007.

[33] J.-S. Youn, H.-S. Kang, M.-J. Lee, K.-Y. Park, and W.-Y. Choi, "High-speed CMOS integrated optical receiver with an avalanche photodetector," *IEEE Photon. Technol. Lett.*, vol. 21, no. 20, pp. 1553–1555, Oct. 2009.

[34] J.-S. Youn, M.-J. Lee, K.-Y. Park, and W.-Y. Choi, "10-Gb/s 850-nm CMOS OEIC receiver with a silicon avalanche photodetector," *IEEE J. Quantum Electron.*, vol. 48, no. 2, pp. 229–236, Feb. 2012.

[35] J.-S. Youn, M.-J. Lee, K.-Y. Park, H. Rücker, and W.-Y. Choi, "An integrated 12.5-Gb/s optoelectronic receiver with a silicon avalanche photodetector in standard SiGe BiCMOS technology," *Opt. Express*, vol. 20, no. 27, pp. 28153–28162, Dec. 2012.

[36] M.-J. Lee, H. Rücker, and W.-Y. Choi, "Effects of guard-ring structures on the performance of silicon avalanche photodetectors fabricated with standard CMOS technology," *IEEE Electron Device Lett.*, vol. 33, no. 1, pp. 80–82, Jan. 2012.

[37] D. S. Kim, S. R. Forrest, G. H. Olsen, M. J. Lange, R. U. Martinelli, and N. J. Di Giuseppe, "Avalanche gain in $InAs_yP_{1-y}$ ($0.1 < y < 0.3$) photodetectors," *IEEE Photon. Technol. Lett.*, vol. 7, no. 8, pp. 911–913, Aug. 1995.

[38] P. P. Webb, R. J. McIntyre, and J. Conradi, "Properties of avalanche photodiodes," *RCA Review*, vol. 35, pp. 234–278, Jun. 1974.

[39] M.-J. Lee, H.-S. Kang, and W.-Y. Choi, "Equivalent circuit model for Si avalanche photodetectors fabricated in standard CMOS process," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1115–1117, Oct. 2008.

[40] C. R. Calvo, "A 2.5 GHz optoelectronic amplifier in 0.18 μm CMOS," *Worcester Polytechnic Institute*, 2003.

[41] E. Säckinger, "The transimpedance limit," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 8, pp. 1848–1856, Aug. 2010.

[42] W.-Z. Chen, Y.-L. Cheng, and D.-S. Lin, "A 1.8-V 10-Gb/s fully integrated CMOS optical receiver analog front-end," *IEEE J. Solid-State Circuits*, vol. 40, no. 6, pp. 1388–1396, Jun. 2005.

[43] C. Toumazou and S. M. Park, "Wideband low noise CMOS transimpedance amplifier for gigahertz operation," *Electron. Lett.*, vol. 32, no. 13, pp. 1194–1196, Jun. 1996.

[44] S. M. Park and H. Yoo, "1.25-Gb/s regulated cascade CMOS transimpedance amplifier for gigabit ethernet application," *IEEE J. Solid-State Circuits*, vol. 39, no. 1, pp. 112–121, Jan. 2004.

[45] C. Kromer, G. Sialm, T. Morf, M. Schmatz, F. Ellinger, D. Erni, and H. Jäckel, "A low-power 20-GHz 52 dBΩ transimpedance amplifier in 80-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 6, pp. 885–894, Jun. 2004.

[46] J. C. Huang, K. S. Lai, and K. Y. J. Hsu, "A fully integrated SiGe optical receiver using differential active miller capacitor for 4.25

Gbit/s fiber channel application," *Jpn. J. Appl. Phys.*, vol. 47, no. 4, pp. 2752–2755, Apr. 2008.

[47] B. Razavi, *Design of Integrated Circuits for Optical Communications*, McGraw-Hill, New York, 2002.

[48] D. Lee, J. Han, G. Han, and S. M. Park, "10-Gb/s 0.0065-mm^2 6-mW analogue adaptive equalizer utilising negative capacitance," *Electron. Lett.*, vol. 45, no. 17, pp. 863–865, Aug. 2009.

[49] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18 μm CMOS technology," *IEEE J. Solid-State Circuits*, vol. 38, no. 12, pp. 2138–2146, Dec. 2003.

[50] E. Säckinger and W. C. Fischer, "A 3-GHz 32-dB CMOS limiting amplifier for SONET OC-48 receiver," *IEEE J. Solid-State Circuits*, vol. 35, no. 12, pp. 1884–1888, Dec. 2000.

[51] H. C. Tsai, J. Y. Yeh, W. H. Tu, T. C. Lee, and C. K. Wang, "A 10GBase-LX4 receiver front end transimpedance amplifier and limiting amplifier," *in Proc. IEEE International Symposium on Circuits and Systems*, vol. 4, pp. 393–396, May 2004.

[52] H.-Y. Huang, J.-C. Chien, and L.-H. Lu, "A 10-Gb/s inductorless CMOS limiting amplifier with third-order interleaving active feedback," *IEEE J. Solid-State Circuits*, vol. 42, no. 5, pp. 1111–1120, May 2007.

[53] K. Yoo, D. Lee, G. Han, S. M. Park, and W. Oh, "A 1.2 V 5.2 mW 40 dB 2.5 Gb/s limiting amplifier in 0.18-μm CMOS using negative impedance compensation," *in IEEE ISSCC Dig. Tech. Papers*, pp. 23–24, Feb. 2007.

[54] J. Han, K. Yoo, D. Lee, K. Park, W. Oh, and S. M. Park, "A low-power gigabit CMOS limiting amplifier using negative impedance compensation and its application," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 20, no. 3, pp. 393–399, Mar. 2012.

[55] P. Muller and Y. Leblebici, *CMOS multichannel single-chip receivers for multi-gigabit optical data communications*, Springer, 2007.

[56] A. H. Pawlikiewicz and D. Hess, "Choosing RF CMOS or SiGe BiCMOS in mixed-signal design," *RF Design*, Mar. 2006.

[57] http://www.ihp-microelectronics.com/en/services/mpw-prototyping/sigec-bicmos-technologies.html "SiGe:C BiCMOS technologies".

[58] B. Heinemann, R. Barth, D. Knoll, H. Rücker, B. Tillack, and W. Winkler, "High-performance BiCMOS technologies without epitaxially-buried subcollectors and deep trenches," *Semicond. Sci. Technol.*, vol. 22, no. 1, pp. 153–157, Jan. 2007.

[59] *Philips Semiconductors Product Specification (SA5212A)*, Philips Semiconductors, Sunnyvale, CA, 1998.

[60] C.-F. Liao and S.-I. Liu, "40 Gb/s transimpedance-AGC amplifier and CDR circuit for broadband data receivers in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 3, pp. 642–655, Mar. 2008.

[61] J. Kim and J. F. Buckwalter, "A 40-Gb/s optical transceiver front-end in 45-nm SOI CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 615–626, Mar. 2012.

[62] F. Y. Liu, D. Patil, J. Lexau, P. Amberg, M. Dayringer, J. Gainsley, H. F. Moghadam, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, E. Alon, and R. Ho, "10-Gbps, 5.3-mW optical transmitter and receiver circuits in 40-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 9, pp. 2049–2067, Sep. 2012.

[63] W.-S. Kim, C.-K. Seong, and W.-Y. Choi, "A 5.4-Gbit/s adaptive continuous-time linear equalizer using asynchronous undersampling histograms," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 9, pp. 553–557, Sep. 2012.

[64] K. Phang and D. A. Johns, “A CMOS optical preamplifier for wireless infrared communications,” *IEEE Trans. Circuits Syst. II*, vol. 46, no. 7, pp. 852–859, Jul. 1999.

[65] J. Kim, B. S. Leibowitz, J. Ren, and C. J. Madden, “Simulation and analysis of random decision errors in clocked comparators,” *IEEE Trans. Circuits Syst. I*, vol. 56, no. 8, pp. 1844–1857, Aug. 2009.

[66] R. Swoboda, J. Knorr, and H. Zimmermann, “A 5-Gb/s OEIC With Voltage-Up-Converter,” *IEEE J. Solid-State Circuits*, vol. 40, no. 7, pp. 1521–1526, Jul. 2005.

[67] L. B. Oliveira, C. M. Leitão, and M. M. Silva, “Noise performance of a regulated cascode transimpedance amplifier for radiation detectors,” *IEEE Trans. Circuits Syst. I*, vol. 59, no. 9, pp. 1841–1848, Sep. 2012.

Abstract (In Korean)

고속 저전력 850-nm Si 광전자 수신기

본 논문은 850-nm 저가 근거리 광연결 응용을 위한 고속 저전력 실리콘 광전자 수신기를 연구하였고, 표준 CMOS 및 SiGe BiCMOS 공정을 이용하여 제작하였다. 제안한 실리콘 광전자 수신기는 실리콘 애벌런치 광검출기와 전기회로가 단일 칩으로 집적되어있다.

제작된 실리콘 애벌런치 광검출기의 DC 및 주파수 응답 특성을 측정하였다. 또한, 신호 대 잡음비 특성을 바이어스를 변화해가며 측정 및 분석하였다. 노이즈 전류원이 포함된 광검출기의 등가 회로 모델을 개발하여 전기회로와 연동된 설계를 하였다.

표준 0.13-μm CMOS 공정을 이용하여 고속 실리콘 광전자 수신기를 제작하였다. 이 수신기에는 애벌런치 광검출기, 전치증폭기, 등화기, 리미팅 증폭기가 집적되어있다. 제작된 광전자 수신기를 이용하여 10-Gb/s 광신호를 성공적으로 전송 (BER < 10^{-12})하였으며, 측정된 광민감도는 -4 dBm이다. 칩 면적은 1 mm x 0.26 mm 이며, 전력 소모는 1.2 V 전원에서 약 66.8 mW이다.

표준 0.25-μm SiGe BiCMOS 공정을 이용하여 고속 실리콘 광전자 수신기를 제작하였다. 이 수신기에는 애벌런치 광검출기 및 다양한

전기회로가 집적되어있다. 수신기의 성능 향상을 위해 애벌런치 광검출기 및 광전자 수신기의 신호 대 잡음비 특성을 연구하였다. 제작된 광전자 수신기를 이용하여 12.5-Gb/s 광신호를 성공적으로 전송 (BER < 10^{-12}) 하였으며, 측정된 광민감도는 -7 dBm이다. 제작된 칩의 면적 및 전력 소모는 각각 1 mm x 0.28 mm 와 59 mW (2.5 V 전원) 이다.

표준 65-nm CMOS 공정을 이용하여 저전력 실리콘 광전자 수신기를 제작하였다. 이 수신기에는 애벌런치 광검출기 및 인버터 기반의 전치증폭기, 등화기, 포스트 증폭기가 단일 칩으로 집적되었다. 전력 효율 향상을 위해서, 전치 증폭기는 인버터 기반으로 설계되었다. 또한, 칩 내부의 신호를 관찰하기 위해서 비동기식 히스토그램 방식이 적용되었다. 제작된 광전자 수신기를 이용하여 8-Gb/s 광신호를 성공적으로 전송 (BER < 10^{-12}) 하였으며, 측정된 광민감도는 -4.5 dBm이다. 제작된 광전자 수신기의 전력 효율은 약 0.63 mW/Gbps 이다.

본 논문에서 제작된 실리콘 광전자 수신기들은 기존에 발표된 850-nm 광전자 수신기들과 성능 비교해 보았을 때, 속도, 광민감도, 전력 효율 측면에서 가장 뛰어난 성능을 보이고 있다. 이는 고속 저전력 850-nm 광연결 응용에 사용 가능할 것으로 예상된다.

핵심 단어: 애벌런치 광검출기, 비동기식 히스토그램, 비트 에러율, CMOS 공정, 선형 등화기, 등가 회로 모델, 리미팅 증폭기, 광연결 응용, 광전자 회로, 전력 효율, 실리콘 포토닉스, SiGe BiCMOS 공정, 신호 대 잡음비, 전치 증폭기.

List of Publications

International Journal Papers

[1] Myung-Jae Lee, **Jin-Sung Youn**, Kang-Yeob Park, and Woo-Young Choi, "A Fully-Integrated 12.5-Gb/s 850-nm CMOS Optical Receiver Based on a Spatially-Modulated Avalanche Photodetector," *submitted to Optics Express*

[2] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "SNR Characteristics of 850-nm OEIC Receiver With a Silicon Avalanche Photodetector," *to be published in Optics Express*

[3] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "An Integrated 12.5-Gb/s Optoelectronic Receiver With a Silicon Avalanche Photodetector in Standard SiGe BiCMOS Technology," *Optics Express,* vol. 20, no. 27, pp.28153-28162, Dec. 2012.

[4] Minsu Ko, **Jin-Sung Youn**, Myung-Jae Lee, Kwang-Chun Choi, Holger Rücker, and Woo-Young Choi, "Silicon Photonics-Wireless Interface IC for 60-GHz Wireless Link," *IEEE Photonics Technology Letters*, vol. 24, no.123, pp.1112-1114, Jul. 2012.

[5] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, and Woo-Young Choi, "10-Gb/s 850-nm CMOS OEIC Receiver With a Silicon Avalanche Photodetector," *IEEE Journal of Quantum Electronics*, vol. 48, no. 2, pp. 229-236, Feb. 2012.

[6] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "A Bandwidth Adjustable Integrated Optical Receiver With an On-Chip Silicon Avalanche Photodetector," *IEICE Electronics Express*, vol. 8, no. 7, pp.404-409, Apr. 2011.

[7] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "7-Gb/s Monolithic Photoreceiver Fabricated With 0.25-μm SiGe BiCMOS Technology," *IEICE Electronics Express*, vol. 7, no. 9, pp.659-665, May 2010.

[8] **Jin-Sung Youn**, Hyo-Soon Kang, Myung-Jae Lee, Kang-Yeob Park, and Woo-Young Choi, "High-Speed CMOS Integrated Optical Receiver With an Avalanche Photodetector," *IEEE Photonics Technology Letters*, vol. 21, no. 20, pp.1553-1555, Oct. 2009.

International Conference Presentations

[1] **Jin-Sung Youn**, Myung-Jae Lee, Wang-Soo Kim, Kang-Yeob Park and Woo-Young Choi, "An 8.7-mW 7-Gb/s CMOS OEIC Receiver," *International SOC Design Conference (Chip Design Contest)*, Nov. 17-19, 2013, Busan, Korea.

[2] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "An Equivalent Circuit With a Noise Source for 850-nm Si Avalanche Photodetector and Optimal Design of Si OEIC Receiver," *The 10th Conference on Lasers and Electro-Optics Pacific Rim (CLEO-PR), and The 18th OptoElectronics and Communications Conference / Photonics in Switching (OECC/PS)*, Jun. 29 – Jul. 4, 2013, Kyoto, Japan.

[3] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "Bit-Error Rate Analysis of Integrated Optoelectronic Receiver," *Photonics Global Conference (PGC)*, Dec. 13-16, 2012, Singapore.

[4] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "A 12.5-Gb/s SiGe BiCMOS Optical Receiver With a Monolithically Integrated 850-nm Avalanche Photodetector," *Optical Fiber Communication Conference and Exposition (OFC) and the National Fiber Optic Engineers Conference (NFOEC),* Mar. 4-8, 2012, Los Angeles Convention Center, USA.

[5] Myung-Jae Lee, **Jin-Sung Youn**, Holger Rücker, and Woo-Young Choi, "A Monolithically Integrated Optical Receiver With a Silicon Avalanche Photodetector for Fiber-Wireless IEEE 802.11 WLAN Applications," *IEEE International Topical Meeting on Microwave Photonics (MWP)*, Oct. 18-21, 2011, Singapore.

[6] **Jin-Sung Youn** and Woo-Young Choi, "6.25-Gb/s Optical Receiver Analog Front-End in a 0.13-μm CMOS Technology," *International SOC Design Conference (Chip Design Contest)*, Nov. 22-23, 2010, Incheon, Korea.

[7] Woo-Young Choi, Myung-Jae Lee, and **Jin-Sung Youn**, "Si Integrated Photoreceivers (Invited Paper)," *IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM)*, Oct. 4-6, 2010, Austin, USA.

[8] Woo-Young Choi, Myung-Jae Lee, and **Jin-Sung Youn**, "CMOS-Compatible Si Avalanche Photodetectors (Invited Paper)," *Asia-Pacific Radio Science Conference*, Sep. 22-26, 2010, Toyama, Japan.

[9] Myung-Jae Lee, **Jin-Sung Youn**, Hyo-Soon Kang, Duho Kim, Minsu Ko, Kang-Yeob Park, and Woo-Young Choi, "622-Mb/s Downlink Transmission in a Fiber-Fed 60-GHz Wireless System Using a CMOS Integrated Optical Receiver," *IEEE International Topical Meeting on Microwave Photonics (MWP)*, Oct. 14-16, 2009, Valencia, Spain.

[10] **Jin-Sung Youn**, Hyo-Soon Kang, Myung-Jae Lee, Kang-Yeob Park, and Woo-Young Choi, "CMOS Integrated Optical Receivers for Radio-over-Fiber Transmission of IEEE 802.11g WLAN Signals," *Asia-Pacific Microwave Photonics Conference (APMP)*, Apr. 22-24, 2009, Beijing, China.

Domestic Conference Presentations

[1] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, and Woo-Young Choi, "애벌런치 광 검출기를 사용한 10 Gb/s CMOS 집적 광 수신기," *The 19th Korean Conference on Semiconductors (KCS)*, Feb, 15-17, 2012, Seoul, Korea.

[2] Minsu Ko, Jeong-Min Lee, **Jin-Sung Youn**, Myung-Jae Lee, and Woo-Young Choi, "60GHz 광섬유-무선 다운링크를 위한 SiGe BiCMOS 집적화된 광-밀리미터파 변환기," *The 19th Korean Conference on Semiconductors (KCS)*, Feb. 15-17, 2012, Seoul, Korea.

[3] **Jin-Sung Youn**, Myung-Jae Lee, Kang-Yeob Park, Holger Rücker, and Woo-Young Choi, "A 9 Gb/s Optical Receiver Front-End With a Monolithically Integrated Avalanche Photodetector in 0.25 μm SiGe BiCMOS Technology," *The 18th Korean Conference on Semiconductors (KCS)*, Feb, 16-18, 2011, Jeju, Korea.

[4] Inyong Kwon, Myung-Jae Lee, Chang-Kyung Seong, **Jin-Sung Youn**, and Woo-Young Choi, "High-Speed Peripheral Circuit for Geiger-Mode Avalanche Photodiode in Standard CMOS Technology," The 18th *Photonics Conference*, Dec. 2-4, 2009, PyeongChang, Korea.

[5] **Jin-Sung Youn** and Woo-Young Choi, "CMOS Avalanche Photo-detector for Radio-over-Fiber Systems," *통신학회 학술대회*, Jun. 22-24, 2009, Jeju, Korea.

[6] **Jin-Sung Youn**, Hyo-Soon Kang, Myung-Jae Lee, Kang-Yeob Park, and Woo-Young Choi, "애벌런치 광 검출기를 사용한 CMOS 집적 광 수신기," *The 16th Conference on Optoelectronics and Optical Communications (COOC)*, May 13-15, 2009, Daecheon, Korea.

[7] Myung-Jae Lee, **Jin-Sung Youn**, Hyo-Soon Kang, Kang-Yeob Park, and Woo-Young Choi, "표준 CMOS 공정에서 제작된 집적 광수신기를 이용한 저비용 Radio-over-Fiber 다운링크," *The 16th Conference on Optoelectronics and Optical Communications (COOC)*, May 13-15, 2009, Daecheon, Korea.

[8] **Jin-Sung Youn** and Woo-Young Choi, "지연을 최소화히기 위한 인터커넥트 모델링," *SOC2008 Conference*, May 10, 2008, Seoul, Korea.

Patents

[1] Woo-Young Choi, **Jin-Sung Youn**, Myung-Jae Lee, and Wang-Soo Kim, "Optical Receiver Having Avalanche Photodetector and Operation Method Thereof,"
Korean Patent (Registered), Patent No. 10-1087247, Nov. 21, 2011.

Awards

[1] **IEEE Student Paper Contest (Gold Paper Award)**, "8 Gb/s 0.63 pJ/bit Optoelectronic IC Receiver in Standard 65-nm CMOS Technology," *IEEE Seoul Section*, Dec. 2013.

[2] **Scientific and Information Technology Paper Award (Encouragement Prize)**, "Fully-Integrated 850-nm CMOS Optical Receiver: Achieving a World Record Speed of 12.5 Gb/s," *IDIS-The Electronic Times*, Dec. 2013.

[3] **Chip Design Contest Session (Best Demo Award)**, "An 8.7-mW 7-Gb/s CMOS OEIC Receiver," *International SoC Design Conference, Chip Design Contest, Busan, Korea*, Nov. 2013.

[4] **TMS Best Paper Award (Silver Prize)**, "An Integrated 12.5-Gb/s Optoelectronic Receiver With a Silicon Avalanche Photodetector in Standard SiGe BiCMOS Technology," *BK21 TMS Institute of Information Technology, School of Electrical and Electronic Engineering, Yonsei Univ., Seoul, Korea*, Jan. 2013.

[5] **Best Paper Award (Dongbu HiTek Prize)**, "A 9 Gb/s Optical Receiver Front-End With a Monolithically Integrated Avalanche Photodetector in 0.25 μm SiGe BiCMOS Technology," *The 18th Korean Conference on Semiconductors (KCS)*, Feb. 2012.

[6] **TMS Best Paper Award (Bronze Prize)**, "High-Speed CMOS Integrated Optical Receiver With an Avalanche Photodetector," *BK21 TMS Institute of Information Technology, School of Electrical and Electronic Engineering, Yonsei Univ., Seoul, Korea*, Feb. 2011.