A Novel PSK Demodulation Scheme Using 1bit-sampling Phase Comparison

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Using 1bit-sampling Phase Comparison

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Abstract

A Novel PSK Demodulation Scheme
Using 1bit-sampling Phase Comparison

Conventional IQ-demodulation schemes suffer from non-idealities such as quantization noise and clipping, and using ADCs for its implementation causes a considerable amount of power consumption. In this dissertation, a novel PSK demodulation scheme that can overcome above problems and deliver much better performance is demonstrated. In the proposed demodulation scheme, the phase of the input signal is compared with multiple reference phases, and from that, the input symbol is recovered. The phase comparison can be realized in the time domain by 1bit-sampling the input signal with multiphase clocks having reference phases. The BER performance of the proposed scheme is derived and it is verified that the proposed scheme is more robust to non-idealities distorting amplitude information. To verify the proposed scheme, two implementations for 60GHz wireless PAN and retinal prosthesis are demonstrated.

Keywords: PSK, demodulation, phase comparison, 60GHz, WPAN, retinal prosthesis, inductive link.

I. Introduction

As wireless communication systems advance, low power consumption becomes an essential requirement while maintaining other performances. A general super-heterodyne receiver consists of analog RF circuits, and the demodulator including IQ-mixers, low-pass filters, ADCs, and digital baseband circuit as shown in Figure 1.1(a) [1]. This scheme is general-purpose because the digital baseband using IQ-demodulation scheme is able to demodulate any kinds of modulations flexibly. Also, the channel estimation and equalization can be done in the digital domain, while these functions are much more difficult to achieve with analog implementation. However, some of applications can use only one modulation scheme or have ignorable distortion. Accordingly, low power consumption can be achieved by abandoning less important functions. After removing them, the baseband circuit doesn’t have to be implemented in the digital domain anymore so that ADC, which consumes considerable amount of power consumption, can be also removed. Consequently, application-optimized schemes using analog or mixed-mode demodulator shown in Figure 1.1(b) are beneficial to low power consumption.

The conventional IQ-demodulation scheme is based on amplitude

information [2, 3, 4]. Therefore, quantization noise from ADC also decreases effective SNR [5, 6, 7]. Additionally, clipping caused by large signal makes upper limit of dynamic range. These become burden to analog RF circuits, thus, increases power consumption and design complexity of them. Consequently, a demodulation scheme not affected by quantization noise and clipping is also advantageous to achieve low power consumption of the whole system.

This dissertation demonstrates a PSK-optimized low-power demodulation scheme that is not affected by amplitude distortions. In the proposed demodulation scheme, the phase of the input signal is compared with multiple reference phases, and from that, the input symbol is recovered. The phase comparison can be realized in the time domain by 1bit-sampling the input signal with multiphase clock signals having reference phases. Compared with the conventional IQ-demodulation scheme, the proposed scheme consumes less power because it uses 1bit-samplers instead of multi-bit-sampling ADCs. The proposed scheme is based-on timing information, consequently, is not affected by quantization noise and clipping, which distort amplitude information.

Following of this section shows the conventional IQ-demodulation scheme and two applications, 60GHz WPAN and retinal prosthesis,

which can be optimized by the proposed scheme. Section II describes the proposed demodulation scheme and the BER performance is also derived. Two implementations for applications are demonstrated in section III and IV. The conclusion is given in section V.

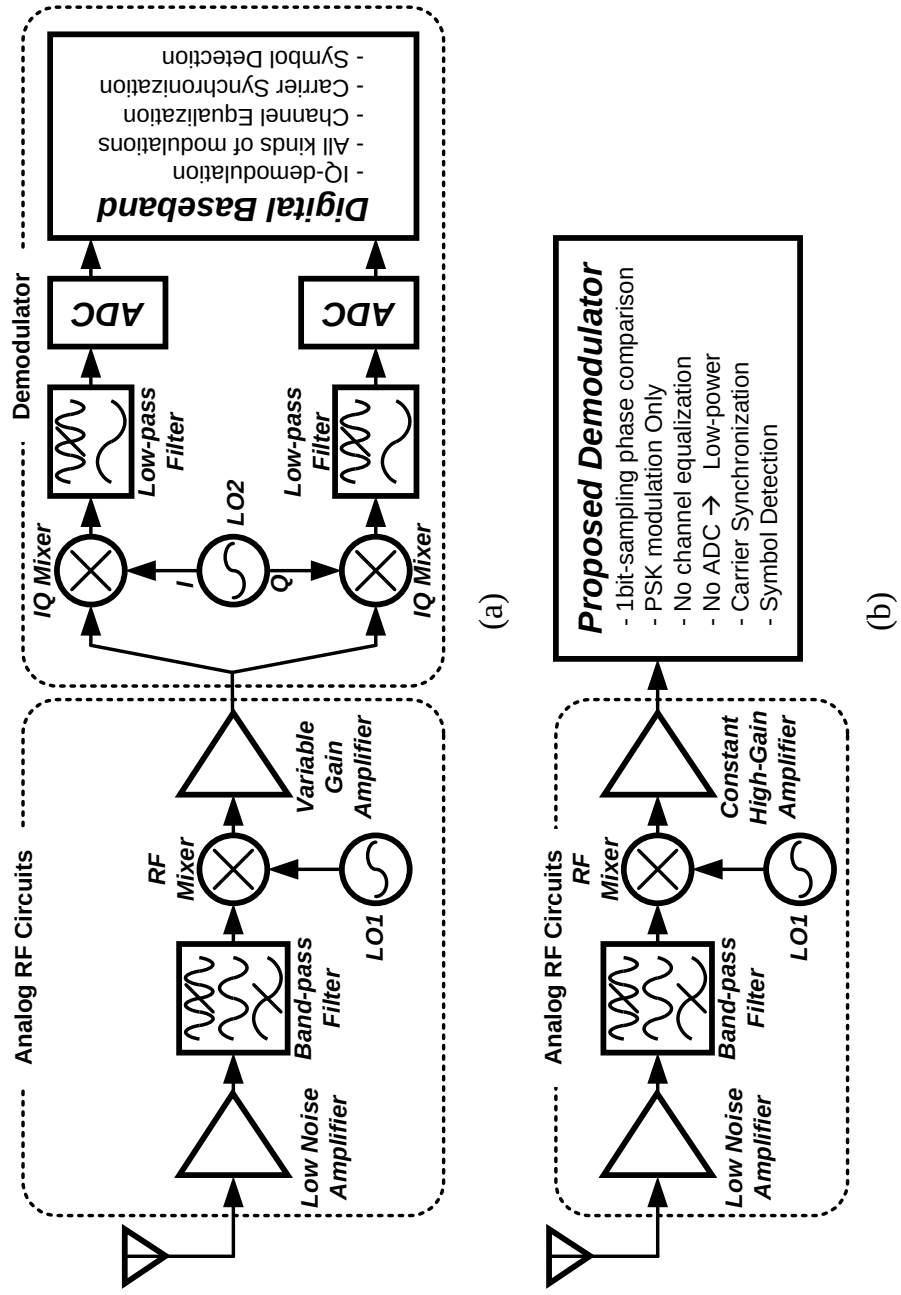


Figure 1.1 Block diagram of super-heterodyne receiver.

A. Application-I: 60-GHz Wireless PAN

The unlicensed 60-GHz band provides opportunities for the wireless personal area network application, and there are several standards using this band such as WiHD, WiGig, and, IEEE 802.15.3c. This band offers wide bandwidth (7GHz), therefore, Gb/s data transmission is possible [7, 8]. Two main applications are A/V data streaming and file downloading, which are depicted in Figure 1.2.

Figure 1.2(a) shows uncompressed video streaming from set-top box to display terminals. In this application, two devices are fixed. Since the link has to support up to 10 meter of long distance, the wave can be blocked by objects. To avoid this problem, an omni-directional antenna can be employed, however, it brings new problem, multi-pass fading effect resulting deeps in frequency response. Consequently, this application prefers OFDM that is robust to frequency-selective distortion.

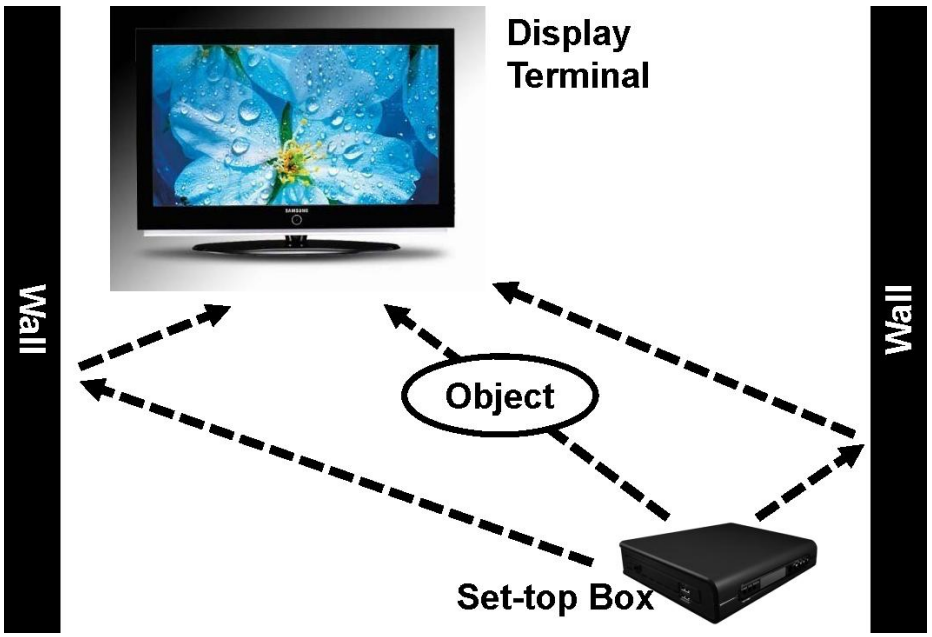
Figure 1.2(b) shows file downloading between various mobile devices. In this application, devices are very easy to relocate, thus, line-of-sight channel is easily set-up by users. But mobile devices prefer simple hardware for low power consumption and small area, consequently, single carrier modulation is preferred in this application

and a directional antenna can be employed to avoid multi-path fading effect.

Accordingly, links can be implemented in different ways as applications as shown in Table 1.1 [7]. While A/V streaming application is implemented with an omni-directional antenna and OFDM modulation, file downloading application uses a directional antenna and single carrier modulation for low hardware complexity. The target of this work is the second application, mobile device file downloading, in which line-of-sight channel is guaranteed so that multi-path fading effect is ignorable. Consequently, the simple structure of the proposed scheme excluding channel equalization can provide enough performance with low power consumption.

Table 1.1 Characteristic of each application

	A/V streaming	**File downloading**
Line-of-sight	LOS/NLOS	LOS only
Distance	~10m	~1m
Antenna	Omni-directional	Directional
Modulation	OFDM	Single Carrier
Hardware Complexity	High	Low



(a)

(b)

Figure 1.2 Applications using 60GHz band. (a) Uncompressed video streaming. (b) Mobile device file downloading.

B. Application-II: Retinal Prosthesis

A retinal prosthesis is a medical device that recovers sight of blind patients. In the normal eye, photoreceptors in a retinal cell convert optical signals into neural signals, which are conveyed to the brain via the optic nerve. Consequently, a malfunction of photoreceptors from diseases or accidents causes blindness. In those cases, however, neurons connected photoreceptors maintain normal function at high rate so that patients can recognize visual information by directly stimulating retinal cells with an implanted device [9]. Since the direct connection between the external camera and the implanted stimulator with cables has hazard of secondary infection by exposing the operated part, wireless connections are preferred. Figure 1.3 shows the block diagram of a retinal prosthesis [10, 11]. The camera unit makes visual information, which is processed by the external unit and transmitted through skin. The implanted unit recovers clock and data from the received signal, drives internally-connected stimulators.

There are three kinds of power supplying methods, implanting batteries with devices, synthesizing electronic energy bio-chemically and power-transmission from external devices by electromagnetic waves. A retinal prosthesis consumes large power, because it drives

numbers of electrodes to stimulate synapses and also has to be always operating while the user is awakened unlike other implantable devices have sleep-mode. The first solution has a problem of the limited capacity, and the second solution cannot provide large amount of energy. Conclusively, the third method that can provide relatively large energy steadily is appropriate. Since power transmission via skin can cause damage from absorption of electromagnetic energy, the communication band has to be carefully selected. 1-10 MHz band shows the lowest absorption rate for electromagnetic waves [11], and inductive links are commonly used for establishing link in this low frequency band. The frequency response of an inductive link is similar to that of resonant circuits, and therefore, the modulated signal is advantageous to maximum power transmission. Constant-amplitude modulation schemes such as pulse width modulation (PWM) [11], frequency shift keying (FSK) [12], and phase shift keying (PSK) [13-15], are preferred for the downlink (transmission from external units), because they are appropriate for rectifier-based power recovery.

Most implantable medical devices require high data rate for the uplink (transmission from implanted units), because they are purposed to sense internal bio-signals. A retinal prosthesis, however, should support the high-speed downlink to transmit visual information from

the external camera unit. Although wide bandwidth offers large data capacity, its low Q-value reduces efficiency of power transmission. Moreover, an E-class power amplifier, which is commonly used in inductive link applications because of its high efficiency, can offer minimum 1.8 of Q-value [16]. Accordingly, higher-order modulations are required to improve data rate within limited bandwidth. Nevertheless, low-order modulations are generally employed, since high-order modulations increase the burden of hardware complexity causing large power consumption. Additionally, rectifier-based power recovery highly distorts amplitude information, therefore, the conventional IQ-demodulation cannot be applied. However, the proposed demodulation scheme is not affected by this problem because it is based on timing information not amplitude information, and capable of demodulating high-order PSK signals while achieving low power consumption.

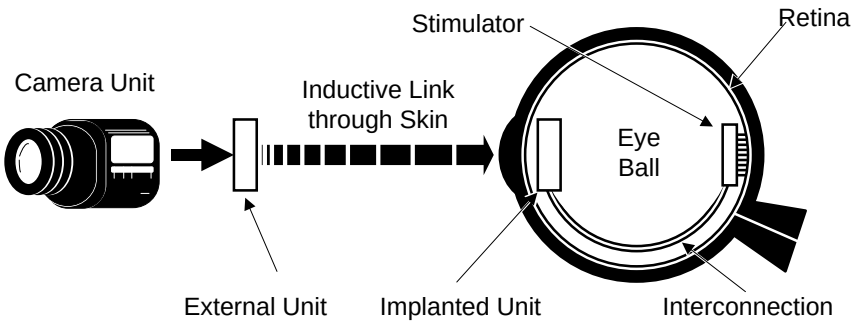


Figure 1.3 Retinal prosthesis.

C. Conventional IQ-Demodulation Scheme

Figure 1.4 shows the conventional IQ-demodulation for 8PSK-modulated signal. Each symbol has its own position vector, which can be detected by down-conversion with IQ-mixers and following integration. Since the decision circuit requires amplitude information, this scheme is usually implemented using ADCs [2].

Figure 1.5 shows an example of IQ-demodulation flow using the digital interpolation technique [3, 4]. After IQ-mixers convert the IF signals to baseband, ADC samples them with a sampling clock. Then, signals between sampled data are produced by interpolation in digital domain. Synchronization and symbol detection are also performed in digital domain. Accordingly, the minimum ADC sampling rate is twice of the data rate to satisfy Nyquist condition ($f_{sampling} > 2 \times$ {Symbol rate}). Several CMOS ADCs operating at GSample/s have been reported, but they usually require large power consumption and chip area [17]. Consequently, the ADC limits the data rate of the system in the digital approach.

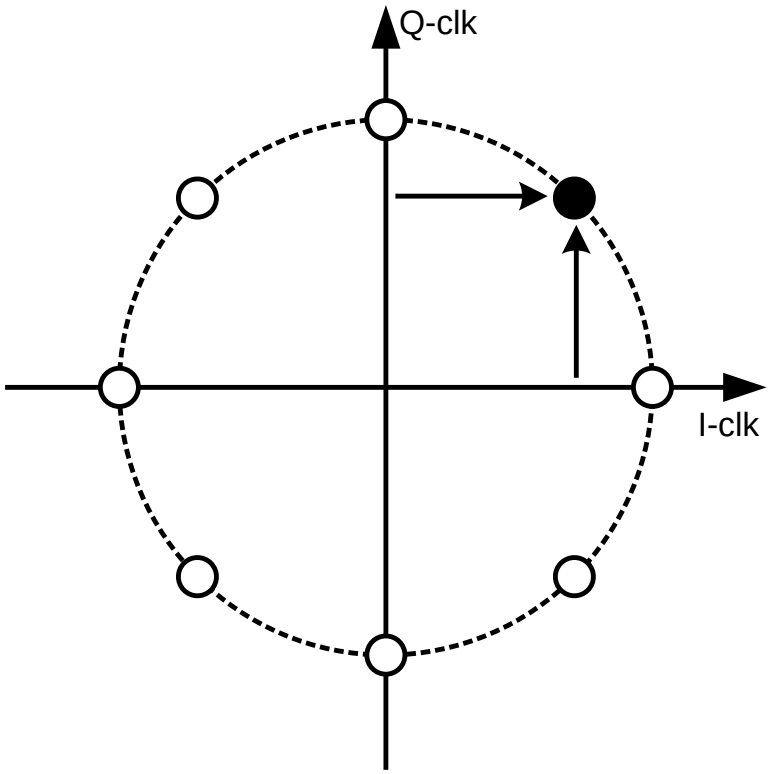


Figure 1.4 IQ-demodulation.

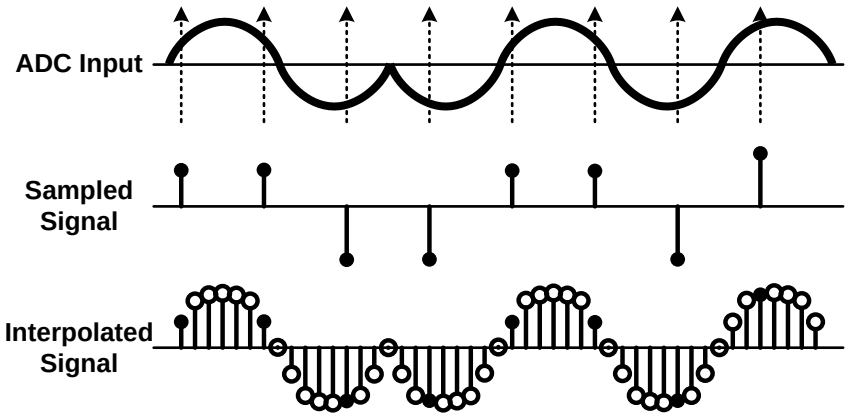


Figure 1.5 Digital interpolation. (a) block diagram. (b) operation

II. Proposed PSK Demodulation Scheme

In the proposed demodulation scheme, the phase of input signal is compared with multiple reference phases, and from this, the input symbol is recovered. Figure 2.1 shows the constellation of 8PSK symbols represented by circles and reference phases by arrows (θ_{ref0-7}), which are

$$\theta_{ref(n)} = n \times \frac{2\pi}{M} \ (n = 0, 1, \dots, M-1)$$

where M is the order of PSK. The phase of any input symbol can be determined by comparing the input symbol phase with each of 8 reference phases. The phase comparison can be done by determining the sign of the phase difference between the input symbol and each reference, $\theta_{ref(n)} - \theta_{input}$. Table 2.1 shows the comparison result for each symbol in 8PSK.

This function can be realized in the time domain by sampling the input signal with multiphase clock signals having reference phases. Sampling is to get amplitude information at a specific timing. Assuming that the input signal is IN and a clock signal having reference phase, $\theta_{ref(n)}$, is $CK_{ref(n)}$, the sampling timing using rising

edges is found as

$$IN(t) = cos\left(\omega t - \theta_{input}\right)$$
$$CK_{ref(n)}(t) = cos\left(\omega t - \theta_{ref(n)}\right)$$
$$\omega t_{r,ref(n)} = \frac{3\pi}{2} + 2k\pi + \theta_{ref(n)}\ (k: integer)$$

Sampling reads the amplitude of the input signal, IN, at $t = t_{r,ref(n)}$. Then, sampled value at rising edges of $CK_{ref(n)}$, is represented as following.

$$\begin{aligned} S_{r,ref(n)}(k) &= IN\left(t_{r,ref(n)}\right) \\ &= cos\left[\frac{3\pi}{2} + 2k\pi + \left(\theta_{ref(n)} - \theta_{input}\right)\right] \\ &= \begin{cases} > 0, & if\ (\theta_{ref(n)} - \theta_{input}) > 0 \\ < 0, & if\ (\theta_{ref(n)} - \theta_{input}) < 0 \end{cases} \end{aligned}$$

1bit-sampling also digitizes sampled analog value to discrete 1bit data, high or low.

$$S_{r,ref(n)}[k] = \begin{cases} High, & if\ (\theta_{ref(n)} - \theta_{input}) > 0 \\ Low, & if\ (\theta_{ref(n)} - \theta_{input}) < 0 \end{cases}$$

Figure 2.2 shows the timing diagrams for 8PSK input signal 011

with each of 4 multiphase clock signals, CK_{ref0-3}. CK_{ref0} and CK_{ref1} produce sampled values of high, and CK_{ref2} and CK_{ref3} low. For each symbol of 8PSK, sampled values are given in Table 2.2. Since the result of phase comparison with θ_{ref4-7} is simply inversion of that with θ_{ref0-3} as shown in Table 2.1, only half of reference phases, or multiphase clocks, are needed in demodulation. Demodulation is complete when sampled values are decoded into the corresponding symbol.

Compared with the widely-used IQ demodulation scheme for PSK modulation, the proposed scheme consumes less power because it uses 1bit-samplers instead of multi-bit-sampling ADCs. It is noticeable that 8PSK demodulator includes reference phases required for BPSK and QPSK as shown in Figure 2.3. Consequently, the demodulator operation mode can be easily switched when necessary using the decoding table given in Table 2.2.

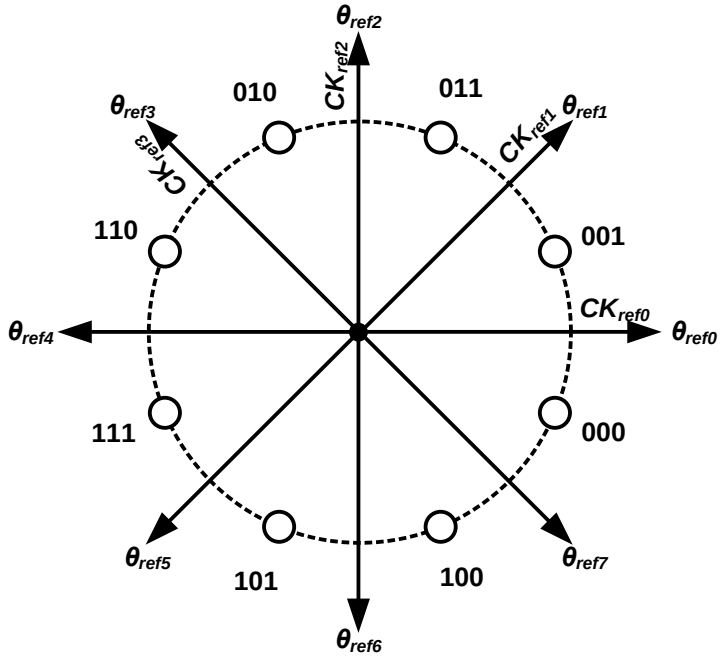


Figure 2.1 Constellation of 8PSK and reference phases.

Table 2.1 Phase comparison results for 8PSK.

Symbol	$\theta_{ref(n)} - \theta_{input}$							
	θ_{ref0}	θ_{ref1}	θ_{ref2}	θ_{ref3}	θ_{ref4}	θ_{ref5}	θ_{ref6}	θ_{ref7}
000	+	+	+	+	-	-	-	-
001	-	+	+	+	+	-	-	-
011	-	-	+	+	+	+	-	-
010	-	-	-	+	+	+	+	-
110	-	-	-	-	+	+	+	+
111	+	-	-	-	-	+	+	+
101	+	+	-	-	-	-	+	+
100	+	+	+	-	-	-	-	+

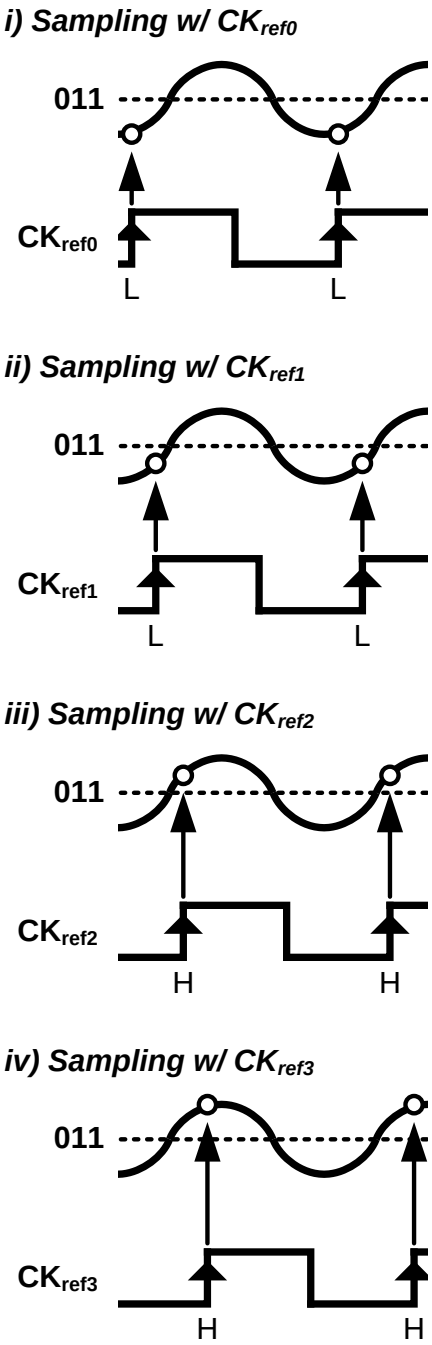
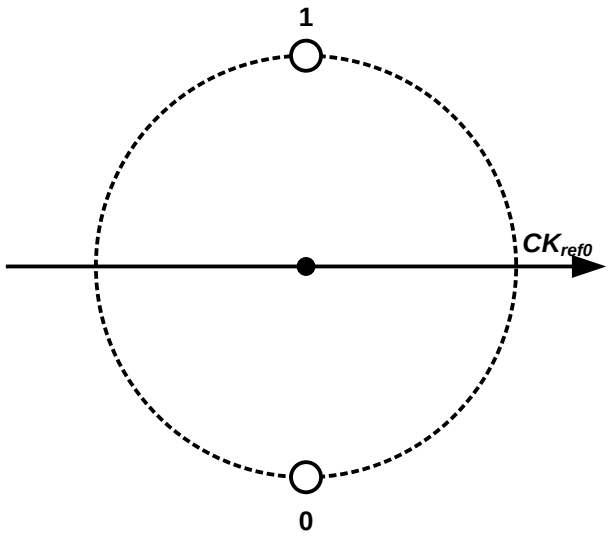


Figure 2.2 Timing diagrams of 1bit-sampling for input symbol 011

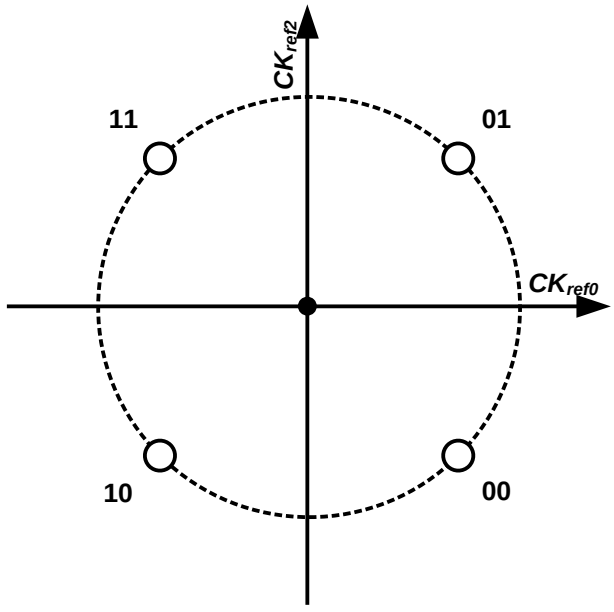
Table 2.2 PSK decoding table for different operation modes.

Operation Mode	**Symbol**	**Sampled Value**			
		$S_{r,ref0}$	$S_{r,ref1}$	$S_{r,ref2}$	$S_{r,ref3}$
BPSK	0	H	×	×	×
	1	L	×	×	×
QPSK	00	H	×	H	×
	01	L	×	H	×
	11	L	×	L	×
	10	H	×	L	×
8PSK	000	H	H	H	H
	001	L	H	H	H
	011	L	L	H	H
	010	L	L	L	H
	110	L	L	L	L
	111	H	L	L	L
	101	H	H	L	L
	100	H	H	H	L

(H: High, L: Low, ×: don't care)



(a)



(b)

Figure 2.3 Constellations of BPSK and QPSK.

A. BER Analysis

Bit-error-rate (BER) is an important figure of a communication system. SNR and non-linearity of RF system firstly limit BER, and then, baseband non-idealities affect it again [5, 6, 7]. There are several kinds of non-idealities in conventional demodulation schemes such as quantization noise, clipping, and etc. However, BER analysis of the proposed demodulation scheme differs from that of conventional schemes, because the proposed scheme detects symbols using timing information not amplitude information. Consequently, it should be verified that the proposed scheme can replace the conventional scheme without much performance degradation.

In this section, the BER performance of the proposed scheme is derived. Then, non-idealities of conventional IQ-demodulation schemes and their effects on the proposed demodulation scheme are analyzed.

A.1. BER vs. SNR

BER analysis of the proposed scheme can be also performed in the time domain. Assuming that $x_t(t)$ is the transmitted signal and $n(t)$ is sum of noise and non-linearity, the received signal, $x_r(t)$, is

$$x_r(t) = x_t(t) + n(t)$$

Figure 2.4 shows waveforms of $x_r(t)$, $x_t(t)$, *and* $n(t)$ for SNR is 3dB. As shown in the figure, $n(t)$ is sometimes larger than $x_t(t)$. Since the symbol detection is based on sampling, error occurs if $n(t)$ is larger than $x_t(t)$ at the sampling moment. Thus, by calculating the probability of that, sampling error probability is derived. At this point, it is noticeable that sampling points are different for each PSK-modulation order in the proposed scheme as shown in Figure 2.5. The minimum value for given PSK-modulation order, S_{min}, is

$$S_{min} = A \sin\left(\frac{\pi}{M}\right)$$

where A is the amplitude of the input signal. Consequently, the error probability of minimum-value sampling is found by calculating the probability of that noise voltage is larger than S_{min}. This process is similar to analysis of jitter in baseband CDR application [18]. Then, the error probability P_e is

$$P_e = \int_{S_{min}}^{\infty} \frac{1}{\sqrt{2\pi\sigma_n^2}} e^{-\frac{(t^2)}{2\sigma_n^2}} dt$$

$$= \int_{A\sin\left(\frac{\pi}{M}\right)}^{\infty} \frac{1}{\sqrt{2\pi\sigma_n^2}} e^{-\frac{(t^2)}{2\sigma_n^2}} dt$$

$$= \int_{\frac{A}{\sigma_n}\sin\left(\frac{\pi}{M}\right)}^{\infty} \frac{1}{\sqrt{2\pi}} e^{-\frac{u^2}{2}} du$$

$$= \mathrm{Q}\left(\frac{A}{\sigma_n} sin\left(\frac{\pi}{M}\right)\right)$$

$$= \mathrm{Q}\left(\sqrt{2 \cdot \frac{A^2}{2\sigma_n^2} sin^2\left(\frac{\pi}{M}\right)}\right)$$

$$= \mathrm{Q}\left(\sqrt{2 \cdot SNR\left[1 - cos^2\left(\frac{\pi}{M}\right)\right]}\right)$$

The derived function is same as the ideal error probability function of PSK signal [Ch. 7 in 19]. However, this is the error probability of the only minimum-value sampling. Thus, the complete error probability function is found after getting error probabilities for all sampling points and calculating the probability of all non-error sampling. Figure 2.6 shows BER vs. E_b/N_0 curve for BPSK, QPSK, 8PSK, and 16PSK. For BPSK, curves are same for the ideal analysis and the proposed scheme. For QPSK, 8PSK, and 16PSK, SNR penalties are under 0.5 dB if target BER is under 10^{-6}.

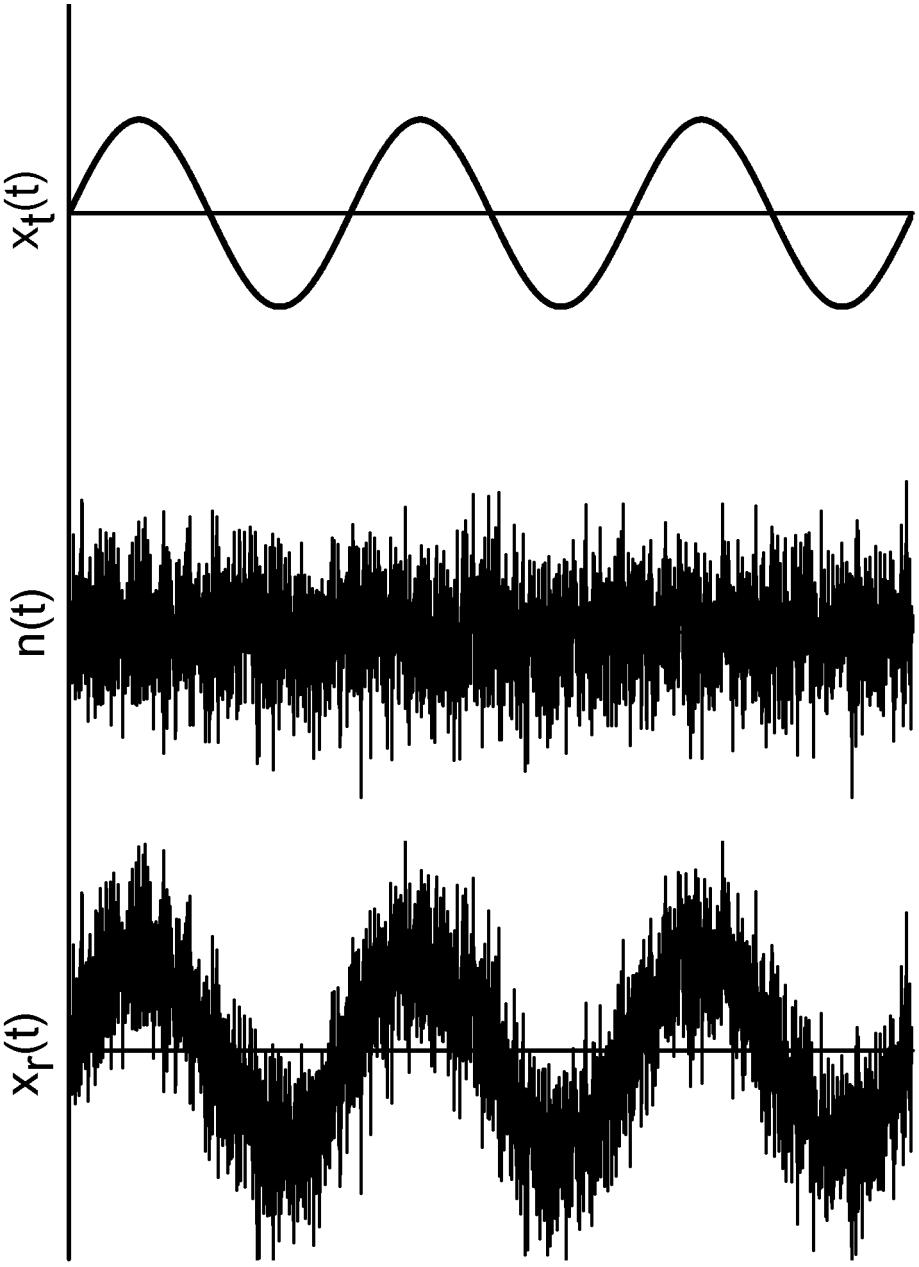


Figure 2.4 Error caused by noise and non-linearity.

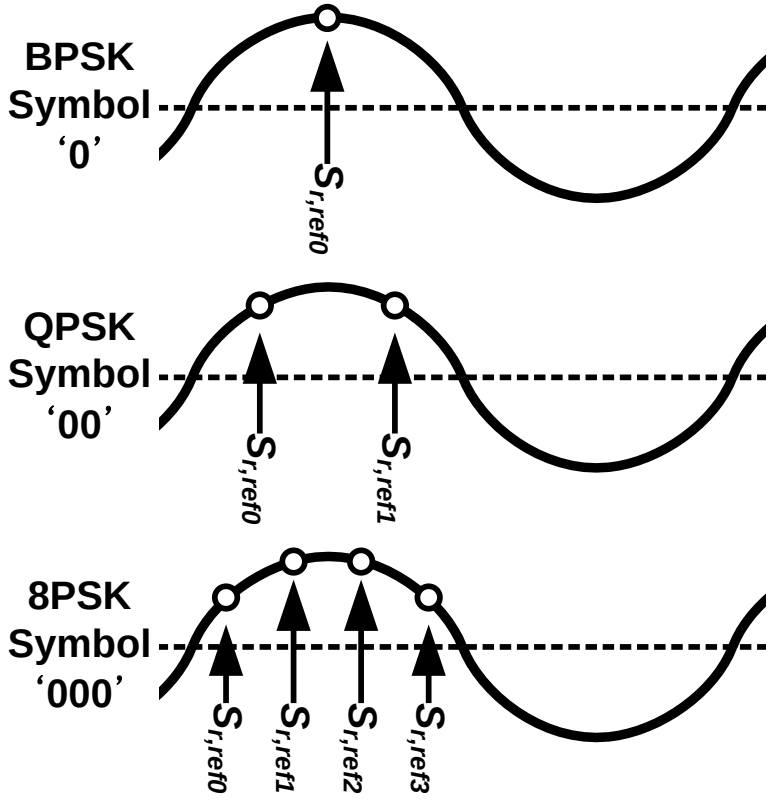


Figure 2.5 Sampling points for each PSK modulation.

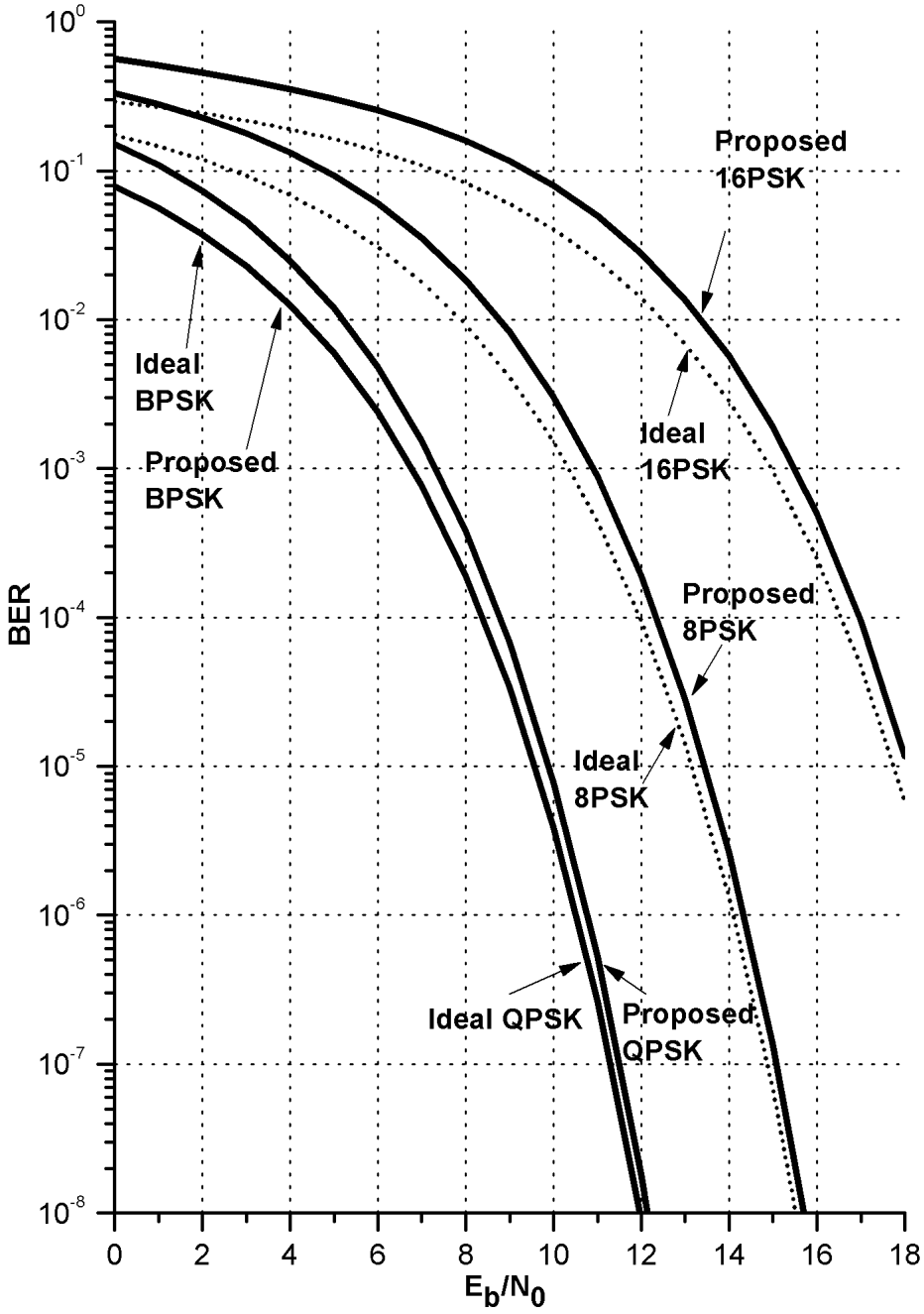
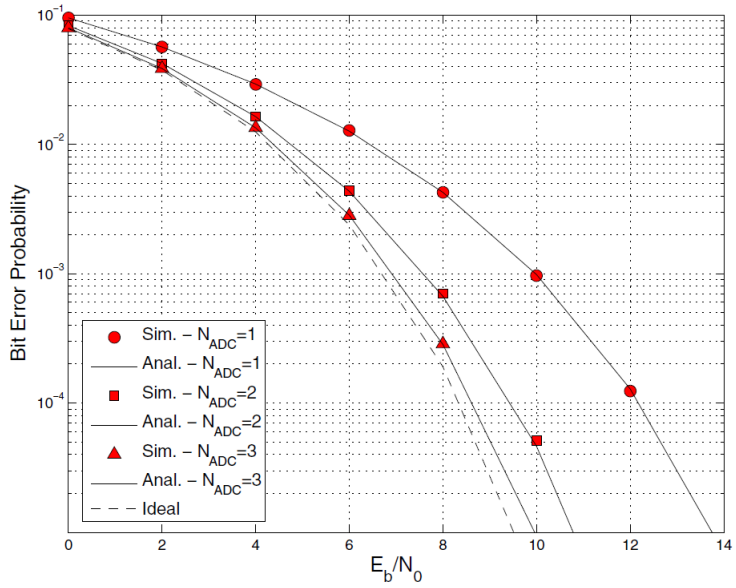


Figure 2.6 Error caused by noise and non-linearity.

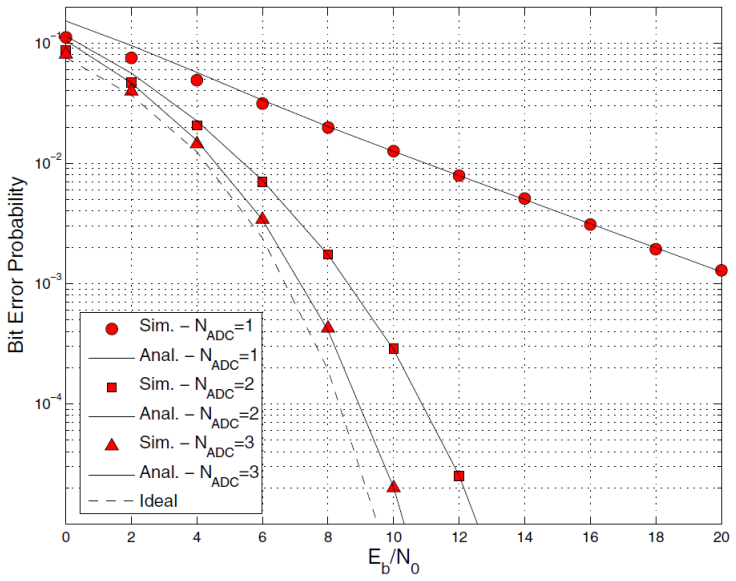
A.2. Quantization Noise

In the IQ-demodulation scheme, the resolution of ADC is also one of important design considerations [5, 6, 7]. Since the IQ-demodulation scheme is based on amplitude information, the remainder of quantization is treated as noise. Figure 2.7 shows BER vs. E_b/N_0 curves for BPSK and QPSK in the presence of ADC quantization noise [6]. A high-resolution ADC results better performance by lowering quantization noise but increases power consumption and area.

However, the proposed scheme is not affected by quantization noise, because it is based on timing information and 1-bit sampling provides enough information for demodulation. Consequently, the BER performance is not degraded from the result in the previous chapter although it can be misunderstood as suffering from large amount of quantization noise because of 1-bit sampling.



(a)



(b)

Figure 2.7 BER analysis considering quantization noise of ADC. (a) BPSK. (b) QPSK. [Fig. 2 and Fig. 6 in 6].

A.3. Clipping of Amplifier

If the input signal to an amplifier is too large, its output waveform is limited by output swing range. That is called clipping and makes upper limit of dynamic range of demodulator [5]. This can be understood as gain distortion of an amplifier caused by rise of higher-order terms, therefore, its output signal is represented as the sum of an original amplified signal and additional higher order terms. That results SNR degradation in conventional demodulation schemes, because those terms distort amplitude information. However, the 1bit-sampled timing information of PSK signal is not affected so that the proposed demodulation scheme is not affected by clipping.

For convenience, only DC-gain characteristic is considered in this analysis, and it is assumed that the frequency response of the amplifier is included in prior BPF. Figure 2.8 shows how clipping affects SNR. In Figure 2.8 (a), 1^{st}- and 3^{rd}-order output signals of an amplifier are illustrated, and their ratio is 3:1. Composition of these signals, the distorted signal, is depicted in Figure 2.8 (b) with the original signal shape (1^{st}-order output signal). The difference between distorted and original signals is converted into the noise in conventional IQ-demodulation scheme, therefore, SNR degrades as 3^{rd}-order distortion increases.

1bit-sampling is to recognize whether the signal is higher or lower than 0. Consequently, it results in correct phase information if zero-crossing points of the output signal of amplifier are same as those of the input signal. Assuming s_o is the output signal corresponding to the input signal, s_i, the non-linear gain affects the output signal as

$$s_o = \alpha_1 s_i + \alpha_2 {s_i}^2 + \alpha_3 {s_i}^3 + \ \ldots$$

$$s_i = A\ cos\ \theta_m$$

whereas α_1, α_2, α_3, … are coefficient for each higher-order terms. The 2nd-order distortion can be easily rejected by using differential topology and higher than 3rd-order terms are ignored here.

$$\begin{aligned} s_o &= \alpha_1 A\ cos\ \theta_m + \alpha_3 A^3 cos^3 \theta_m \\ &= \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right) cos\ \theta_m + (\frac{\alpha_3 A^3}{4}) cos\ 3\theta_m \\ &= g_1 cos\ \theta_m + g_3\ cos\ 3\theta_m \end{aligned}$$

where g_1, g_3 are respectively 1st- and 3rd-order gain. In general differential amplifiers, they have following relationships.

$$g_1 > 0, \quad g_3 < 0, \quad g_1 > -g_3$$

Our focus is that zero-crossing points of s_o are same as those of s_i. Using the characteristic of trigonometric function, zero-crossing points are found as

$$s_o = g_1 cos\ \theta_m + g_3[\frac{1}{2}(cos\ 2\theta_m\ cos\ \theta_m + cos\ \theta_m)]$$
$$= cos\ \theta_m \left[g_1 + \frac{g_3}{2}(cos\ 2\theta_m + 1)\right] = 0$$

$$cos\ \theta_m = 0 \quad or \quad g_1 + \frac{g_3}{2}(cos\ 2\theta_m + 1) = 0$$

The former solution represents zero-crossing points of input signal, s_i. Therefore, if the later solution is not valid, zero-crossing points of s_o are same as those of s_i. The later solution is not valid if

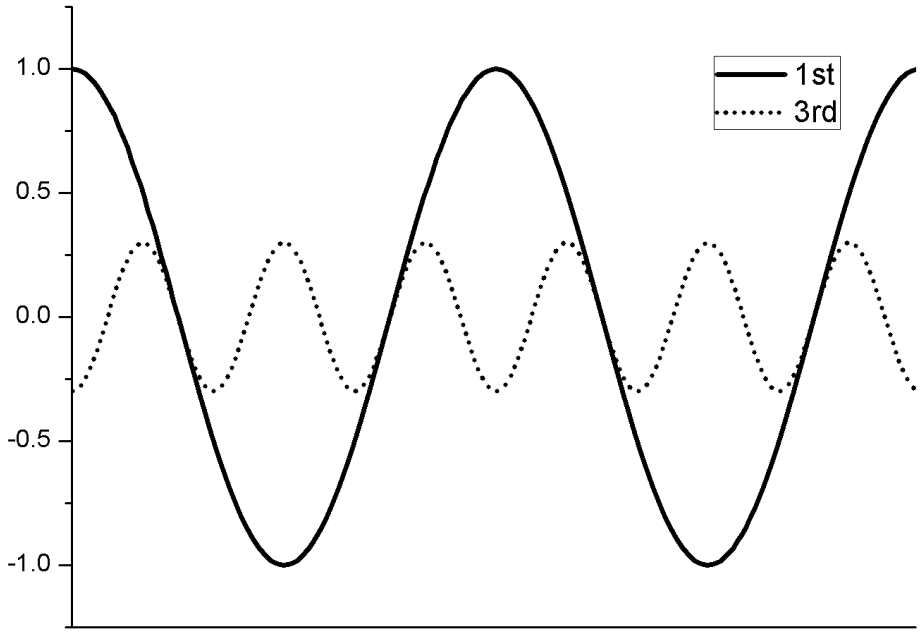
$$cos\ 2\theta_m = \frac{2g_1 - g_3}{-g_3} > 1$$

Since $g_1 > -g_3$, this is always true. Consequently, zero-crossing points of 3rd-order distorted signal are same as original signal.

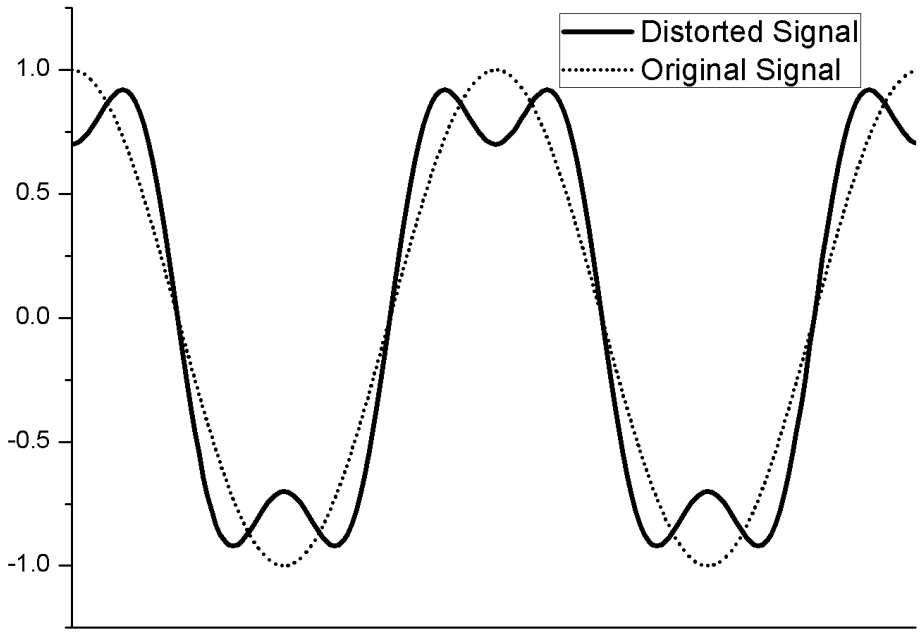
To verify this, a differential amplifier is designed and simulated. For 100MHz of sinusoidal input, the output signal of this amplifier has g_1

and g_3 as shown in Figure 2.9 (a). g_3 increases faster than g_1, but is saturated so that amplitude of g_1 is always larger than that of g_3. Figure 2.9 (b) is time-domain simulation result for various input amplitude. As shown in the figure, zero-crossing points are not changed by 3rd-order distortion.

Consequently, the clipping makes no upper limit of dynamic range in the proposed scheme. Then, the system can employ a constant-high-gain amplifier not a variable gain amplifier, thus, the burden to analog circuit is relieved.

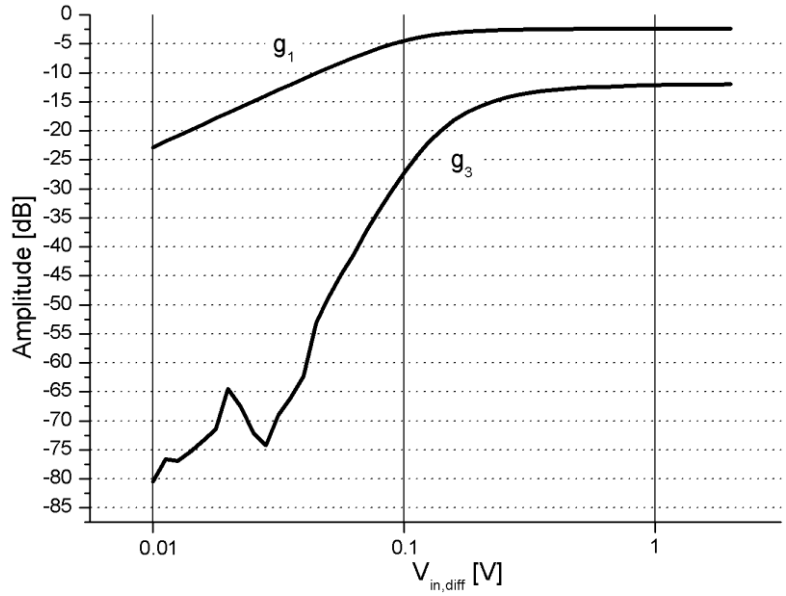


(a)

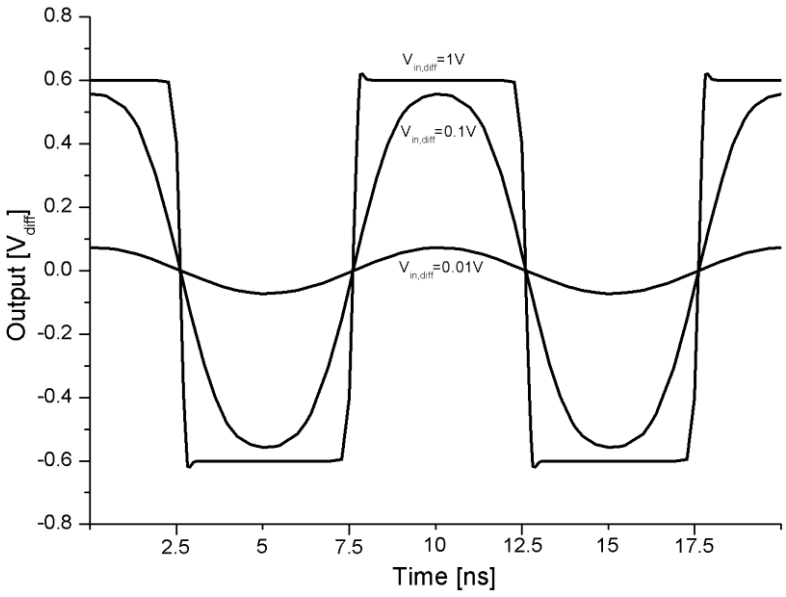


(b)

Figure 2.8 Clipping of amplifier. (a) 1st-order and 3rd-order output signals. (b) Original and distorted signals.



(a)



(b)

Figure 2.9 Simulation results. (a) 3rd-order distortion of designed amplifier. (b) output signals in time domain simulation for various input amplitude.

B. Improving timing resolution

In the proposed scheme, the input signal is sampled with multiphase clocks every receiver clock period, synchronized to the carrier frequency, not to the symbol rate. Thus, a symbol transition occurring between samplings is recognized at the next sampling. This delay causes the quantized timing error.

Figure 2.10 (a) shows the timing diagram for 8PSK demodulation. Since rising edges of receiver multiphase clocks appear one by one, a sample set required for demodulation is complete after the latest sampling, using CK_{ref3} in Figure 2.10 (a). Therefore, transitions of recovered symbol are recognized at rising edges of the latest multiphase clock. Consequently, the maximum quantized timing error is a period of the carrier. This affects jitter performance directly. With a higher carrier frequency, this quantized timing error is reduced because timing resolution is improved.

This timing resolution can be also improved by employing double-edge-triggered sampling. Although the proposed scheme requires only a half of multiphase clocks, another half are generated together in most multiphase clock generation because they are just inversion of required clocks as

$$
\begin{aligned}
CK_{ref(n)}(t) &= \cos\left(\omega t - \theta_{ref(n)}\right) \\
&= -cos\left(\omega t - \theta_{ref(n)} + \pi\right) \\
&= -cos\left[\omega t - \left(n \times \frac{2\pi}{M} - \pi\right)\right] \\
&= -cos\left(\omega t - \theta_{ref\left(n+\frac{M}{2}\right)}\right) \\
&= -CK_{ref\left(n+\frac{M}{2}\right)} \quad \left(0 \le n \le \frac{M}{2} - 1\right)
\end{aligned}
$$

Since rising edges of $CK_{ref\left(n+\frac{M}{2}\right)}$ are same as falling edges of $CK_{ref(n)}$,

$$
\omega t_{f,ref(n)} = \frac{\pi}{2} + 2k\pi + \theta_{ref(n)} \; (k: integer)
$$

$$
\begin{aligned}
S_{r,ref\left(n+\frac{M}{2}\right)}(k) &= S_{f,ref(n)}(k) \\
&= IN\left(t_{f,ref(n)}\right) \\
&= cos\left[\frac{\pi}{2} + 2k\pi + \left(\theta_{ref(n)} - \theta_{input}\right)\right] \\
&= -cos\left[\frac{3\pi}{2} + 2k\pi + \left(\theta_{ref(n)} - \theta_{input}\right)\right] \\
&= -S_{r,ref(n)}(k)
\end{aligned}
$$

$$
S_{r,ref\left(n+\frac{M}{2}\right)}[k] = \overline{S_{r,ref(n)}[k]}
$$

This result is same as given in Table 2.1. Consequently, demodulation is performed every half period of receiver clock by sampling at both rising and falling edges, so that the maximum quantized timing error is halved as illustrated in Figure 2.10 (b).

However, this method is affected by even-order distortion such as duty-cycle distortion. Even-order distortion makes different duration of high and low of the input signal, therefore, a symbol detection at a rising edge might differ from that at a falling edge. In the ideal case, the proposed scheme is not affected if the amount of duty-cycle distortion doesn’t excess the distance between two reference phases. But, considering noise, it degrades the BER performance since noise margin decreases. Consequently, it is better to use only rising or falling edges in the case that even-order distortion is considerable.

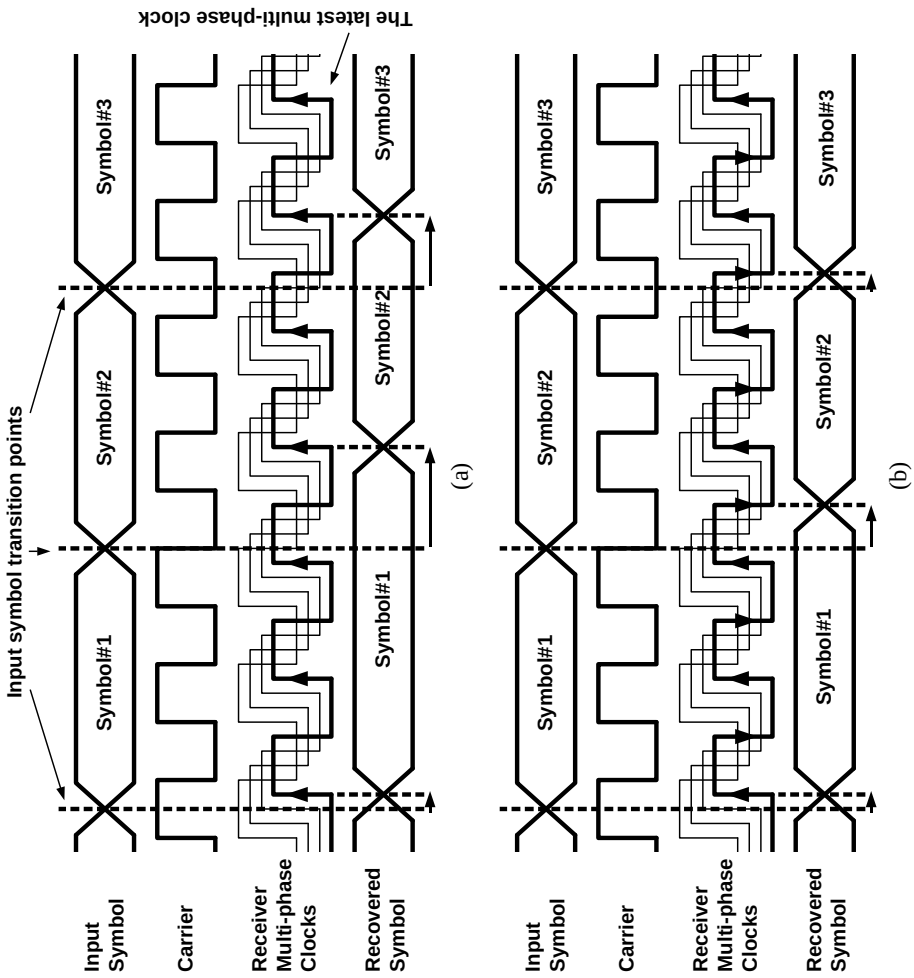


Figure 2.10 Quantized timing error. (a) single-edge-triggered sampling. (b) double-edge-triggered sampling

C. Tracking PSK-modulated Signal

To optimize SNR, an input symbol should be located at the center of two adjacent reference phases. The phase-tracking function for PSK can be implemented by employing a combination of multiple tri-state phase detectors (PD), each of which is assigned for each of symbols and outputs only if the input symbol is assigned one. An assigned PD detects phase information by comparing input signal to the desired symbol phase, $\theta_{sym(n)}$, which are

$$\theta_{sym(n)} = \frac{(2n-1)}{2} \times \frac{2\pi}{M} \quad (n = 0, 1, \ldots, M-1)$$

Figure 2.11 (a) shows the exemplary implementation for 8PSK. Each of phase detectors are assigned at the decision region of each symbol. Additionally to previously shown reference phases for phase comparison, symbol reference phases are illustrated. Assuming the input symbol is 001, Figure 2.11 (b) and (c) show two possible cases that the phase of input symbol is not aligned to the desired phase. The assigned tri-state phase detector (PD1) uses three phases, one symbol reference phase ($\theta_{sym\ 1}$) to detect phase difference and two reference phase ($\theta_{ref\ 0}$ and $\theta_{ref\ 1}$) to decide whether detected phase difference

should be output or not. And from this, the receiver clock generator corrects its reference phases to be phase-locked to the input signal. In the figure, the only assigned phase detector (PD1) outputs 1 for UP or DN signal while other phase detectors output 0 for both UP and DN.

This function can be also realized using 1bit-sampling. Assuming that IN is the input signal having symbol phase, θ_{input}, and $CK_{sym(M)}$ is receiver clock having symbol reference phase, $\theta_{sym(M)}$. There is an initial phase error, θ_{error}, which is added to the receiver clock phase.

$$IN(t) = cos\ (\omega t - \theta_{input})$$

$$CK_{sym(n)}(t) = cos\ (\omega t - \theta_{sym(n)} - \theta_{error})$$

$$\omega t_{r,sym(n)} = \frac{3\pi}{2} + 2k\pi + \theta_{sym(n)} + \theta_{error}\ (k: integer)$$

Thus, sampled value is represented as

$$S_{sym(n)}(k) = IN\left(t_{r,sym(n)}\right)$$
$$= cos\ [\frac{3\pi}{2} + 2k\pi + \left(\theta_{sym(n)} - \theta_{input}\right) + \theta_{error}]$$

Since the phase detection is valid for that input symbol is same as symbol reference phase, $\theta_{sym(n)} - \theta_{input} = 0$.

$$S_{sym(n)}(k) = \begin{cases} > 0, & if\ \theta_{error} > 0 \\ < 0, & if\ \theta_{error} < 0 \end{cases}$$

As shown above, 1bit-sampling also digitizes sampled analog value to discrete 1bit data, high or low.

$$S_{sym(n)}[k] = \begin{cases} High, & if\ \theta_{error} > 0 \\ Low, & if\ \theta_{error} < 0 \end{cases}$$

The phase controller then adjusts its clock phase using the detected phase information to reject the phase error. If θ_{error} is positive, receiver clock should increase its phase, and if negative, decrease. Thus, UP_n and DN_n signals from nth phase detector is derived as

$$UP_n = \overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} \bullet S_{r,sym(n+1)}$$
$$DN_n = \overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} \bullet \overline{S_{r,sym(n+1)}}$$

where $\overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)}$ is term for detecting the input symbol and positive only when input symbol is same as symbol reference phase, $\theta_{sym(n+1)}$. Then the output of the combinational phase detection is as following.

$$UP = \sum_{n=0}^{M-1} UP_n$$

$$= \sum_{n=0}^{\frac{M}{2}-1} UP_n + \sum_{n=\frac{M}{2}}^{M-1} UP_n$$

$$= \sum_{n=0}^{\frac{M}{2}-1} \overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} \bullet S_{r,sym(n+1)} + \sum_{n=\frac{M}{2}}^{M-1} \overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} \bullet S_{r,sym(n+1)}$$

$$= \sum_{n=0}^{\frac{M}{2}-1} \overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} \bullet S_{r,sym(n+1)} + \sum_{n=0}^{\frac{M}{2}-1} S_{r,ref(n)} \bullet \overline{S_{r,ref(n+1)}} \bullet \overline{S_{r,sym(n+1)}}$$

$$= \sum_{n=0}^{\frac{M}{2}-1} [\overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} \bullet S_{r,sym(n+1)} + S_{r,ref(n)} \bullet \overline{S_{r,ref(n+1)}} \bullet \overline{S_{r,sym(n+1)}}]$$

$$= \sum_{n=0}^{\frac{M}{2}-1} \left(\overline{S_{r,ref(n)}} \bullet S_{r,ref(n+1)} + S_{r,ref(n)} \bullet \overline{S_{r,ref(n+1)}}\right) \bullet \left(\overline{S_{r,ref(n)}} \bullet S_{r,sym(n+1)} + S_{r,ref(n)} \bullet \overline{S_{r,sym(n+1)}}\right)$$

$$= \sum_{n=0}^{\frac{M}{2}-1} \left(S_{r,ref(n)} \ xor \ S_{r,ref(n+1)}\right) \bullet \left(S_{r,ref(n)} \ xor \ S_{r,sym(n+1)}\right)$$

Similarly, *DN* is also derived as

$$DN = \sum_{n=0}^{\frac{M}{2}-1} \left(S_{r,ref(n)} \ xor \ S_{r,ref(n+1)}\right) \bullet \left(S_{r,sym(n+1)} \ xor \ S_{r,ref(n+1)}\right)$$

With that sampling is done in the order of $S_{r,ref(n)}$, $S_{r,sym(n+1)}$, and $S_{r,ref(n+1)}$, this result is same as the output of bang-bang type phase detector in baseband CDR application [Sec. 9.2.2 in 20], outputs of which are represented as

$$UP = (S_1 \ xor \ S_3) \bullet (S_1 \ xor \ S_2)$$
$$DN = (S_1 \ xor \ S_3) \bullet (S_2 \ xor \ S_3)$$

In other words, the edge-tracking structure of CDR application can be applied to phase-tracking of PSK signals. As previously demonstrated, 1bit-sampling phase comparison concerns only zero-crossing points, therefore, slicing PSK signal with a limiting amplifier doesn't affect the performance. Figure 2.12 shows sliced PSK symbols of BPSK-, QPSK-, and 8PSK-modulated signals in the time domain. After slicing, each of symbols becomes NRZ signal in baseband application. Consequently, CDR circuits for baseband application can be applied to tracking and

demodulating PSK signals.

As the order of PSK increases, the number of bits representing a symbol increases, and the data rate the employed CDR has to operate at is calculated as following.

$$DR = (Carrier\ frequency) \times M$$

To maintain the theoretical basis of the proposed scheme, the receiver clock has the same frequency as the carrier in following implementations of this dissertation.

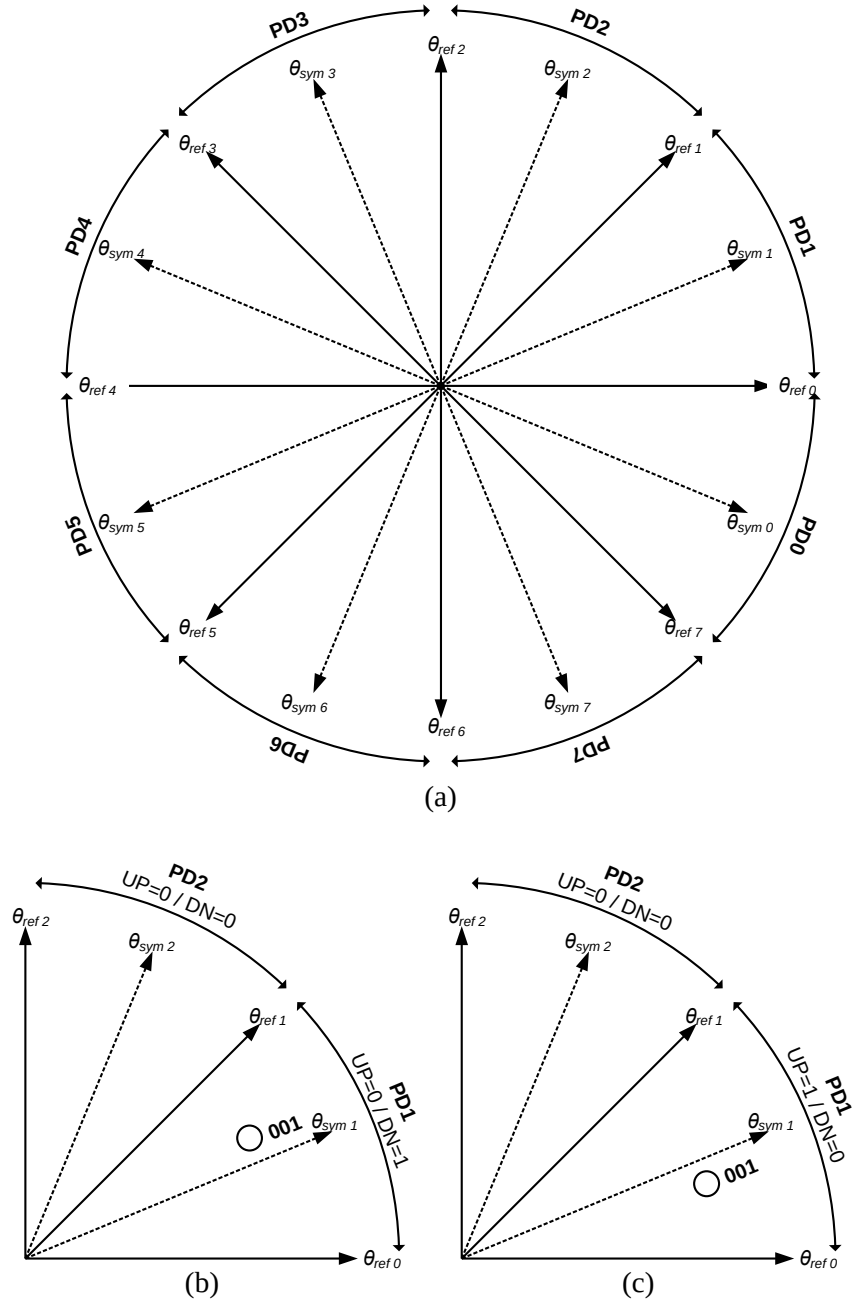


Figure 2.11 Phase tracking.

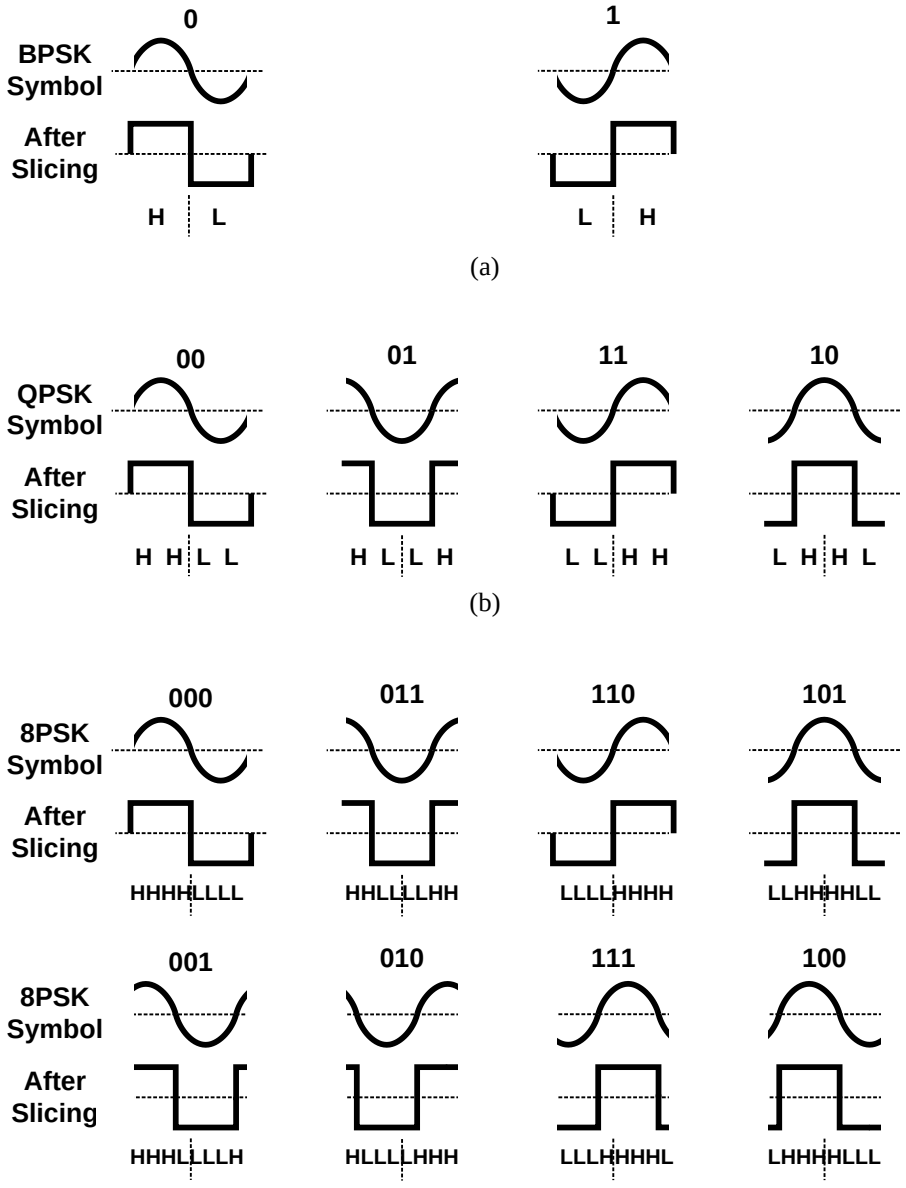


Figure 2.12 Sliced PSK symbols in time domain. (a) BPSK. (b) QPSK. (c) 8PSK.

III. Implementation-I: 60-GHz Wireless PAN

Among two previously introduced applications, the target application of this work is mobile device file downloading, in which systems are usually implemented using single carrier modulation for simple hardware and a directional antenna to avoid fading effect. Therefore, the IQ-demodulation scheme using ADCs is not very advantageous to this application although it is powerful at channel estimation. Additionally, high-speed ADCs usually employ flash-type structure that includes 2^{bit}-1 of samplers. For example, 3-bit ADC includes 7 samplers. The IQ-demodulation scheme requires 2 ADCs including 14 samplers and digital baseband circuits occupying large area. The proposed demodulation scheme using 1-bit sampling cannot provide enough information for channel estimation, however, it is acceptable because of non-fading channel. It achieves both low power consumption and small area since it uses only 8 samplers and small circuits of phase synchronization for QPSK. Consequently, it can be a good solution for the short range and line-of-sight mobile applications.

A. Circuit Implementation

The proposed demodulation scheme is complete by phase comparison using 1bit-sampling, and decoding the result. However, QPSK doesn't require decoding because sampled results directly indicate original symbols. As shown in Table 3.2, a sampled value is H for 0 of input data and L for 1. Consequently, each of $S_{r,ref\ 0}$ and $S_{r,ref\ 1}$ represents recovered data.

The target symbol rate is selected as 1.7GSymbol/s, which is compatible to IEEE802.15.3c [21]. Figure 3.1 is the block diagram of the prototype chip. It includes quad-rate CDR, consisting of quad-rate bang-bang PD, charge pump, VCO, and loop filter. The symbol detection block is added for inverting samples at falling edges to improve timing resolution as mentioned in section II. The 4-stage ring VCO provides 8 multi-phase clocks ($CK_{ref\ 0,\ 1}$, $CK_{sym\ 0,\ 1}$ and their inversions).

Table 3.1 QPSK decoding table

Input Symbol		**Sampled Value**	
Data0	***Data1***	$S_{r,ref\ 0}$	$S_{r,ref\ 1}$
0	0	H	H
0	1	H	L
1	1	L	L
1	0	L	H

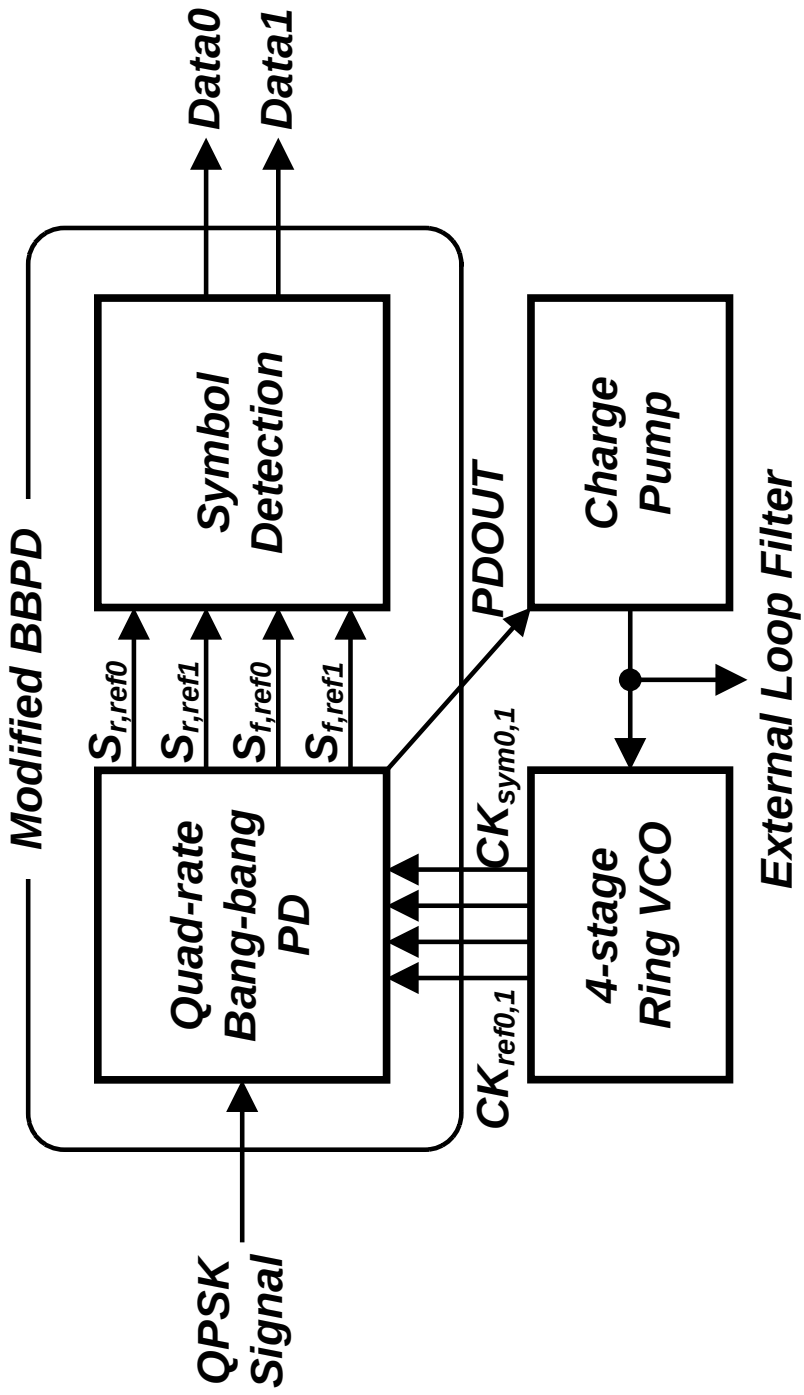


Figure 3.1 Block diagram of prototype chip.

A. 1. Modified Bang-bang Phase Detector

Figure 3.2 shows the block diagram of the designed PD, which is modified from the PD structure given in [22]. It consists of D-FFs (D1-8), XOR gates (X1-8), and comparators (C1-4) along with two additional MUXs (M1-2) for inverting function. M1 and M2 use outputs of D-FFs ($S_{r,ref\ 0}$, $S_{r,ref\ 1}$, $S_{f,ref\ 0}$ and $S_{f,ref\ 1}$) to compose double edge triggered flip-flops, and have one inverted input port in order to invert samples at falling clock edges. Consequently, M1 produces an $S_{r,ref\ 0}$ when $CK_{ref\ 0}$ is low, and inverted version of $S_{f,ref\ 0}$ when $CK_{ref\ 0}$ is high. M2 operates similarly with $S_{r,ref\ 1}$, $S_{f,ref\ 1}$ and $CK_{ref\ 1}$. There are two dummy MUXs to match delays for $S_{r,sym\ 0}$, $S_{r,sym\ 1}$, $S_{f,sym\ 0}$ and $S_{f,sym\ 1}$. These are not shown in the figure.

Latches in D-FFs and XOR gates are derived from the MUX circuit. Figure 3.3 shows the schematic of the MUX circuit, which is realized with the differential current mode logic (CML). The benefit of this is common-mode noise rejection as well as high switching speed. Comparators are implemented using the charge pump shown in Figure 3.4 to realize combining outputs of PD by current summation. The differential charge pump scheme is employed for high speed operation because charge pumps should respond in every carrier period. The additional benefit is power supply noise immunity.

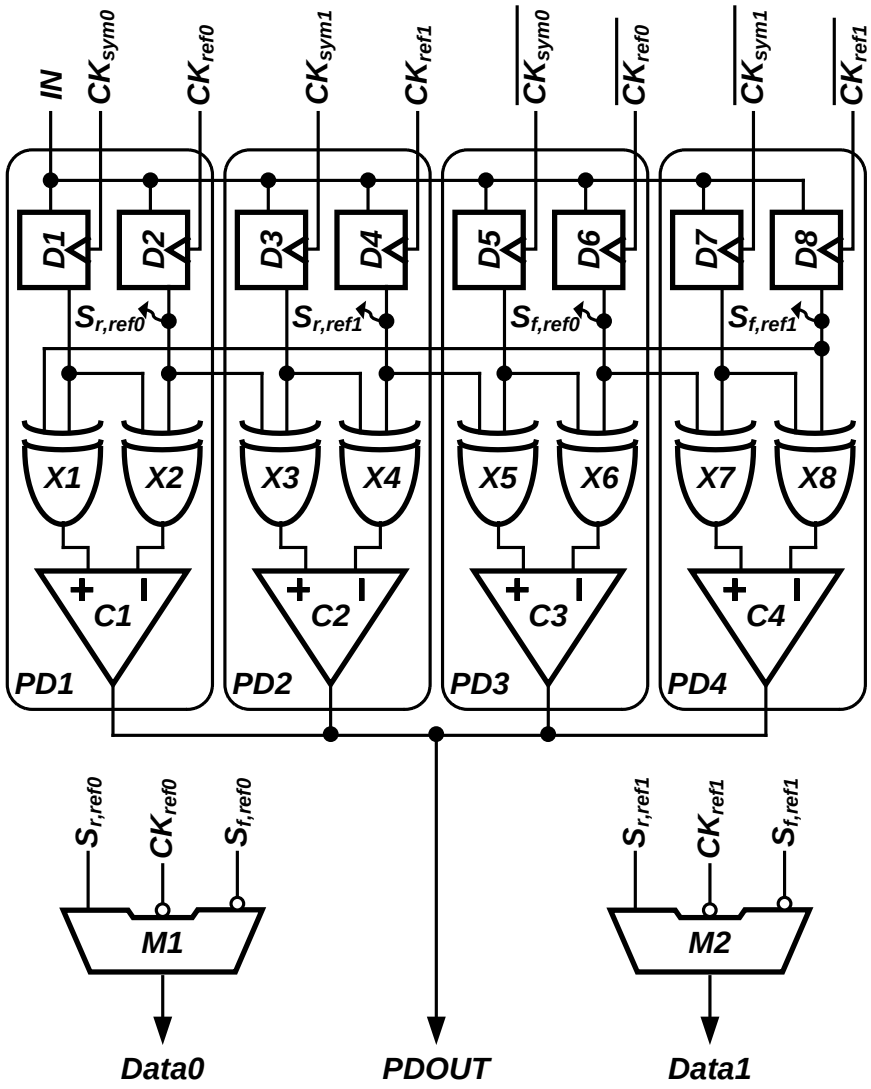


Figure 3.2 Modified quad-rate bang-bang PD.

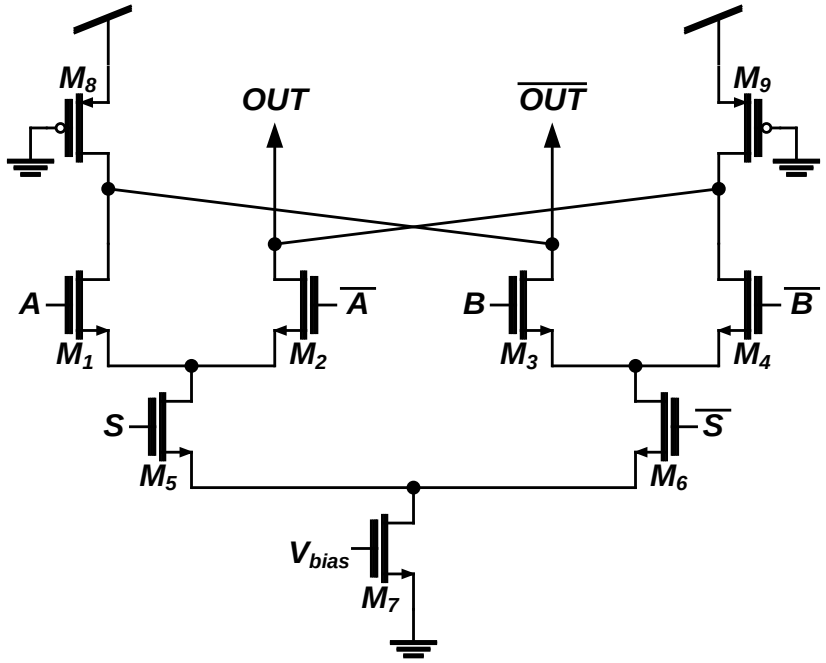


Figure 3.3 Schematic of MUX.

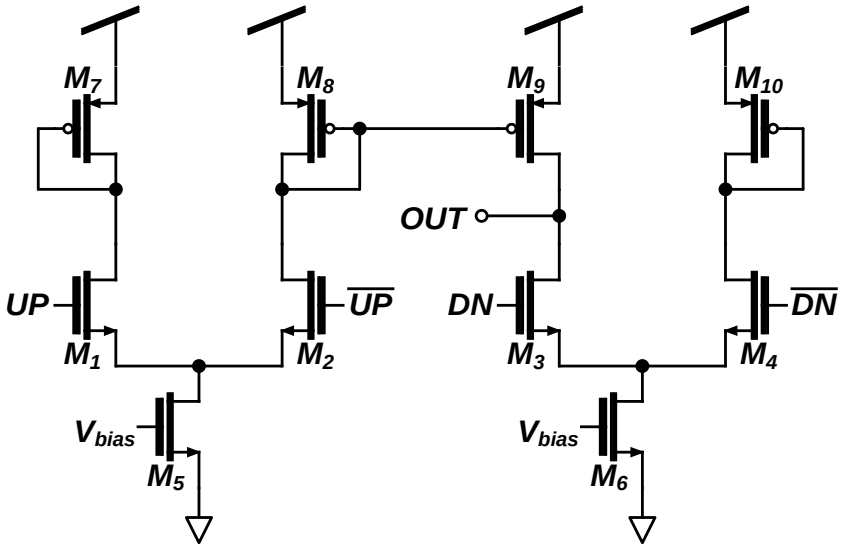


Figure 3.4 Schematic of charge pump.

A. 2. VCO & Charge Pump

The proposed demodulation scheme can employ any type of phase control schemes used in CDR applications. The previous work for BPSK demodulator, [23], employed semi-digital DLL scheme proposed in [24]. However, such a scheme requires multiple interpolators to provide multi-phase clocks. In our prototype QPSK demodulator, four-phase VCO is directly controlled. Although LC oscillators are preferred because of their good phase noise performances, a 4-stage ring VCO is employed in this work, since multi-phase LC oscillators require multiple inductors and occupy a large area [22, 25].

4-stage ring VCO is realized as shown in Figure 3.5(a). The delay cell in the Figure 3.5(b) is controlled by the tail current of the differential pair. While the tail current is tuned, PMOS loads (M5, M6) maintain the output voltage swing by adapting Vconp in the control voltage generator in the Figure 3.5(c).

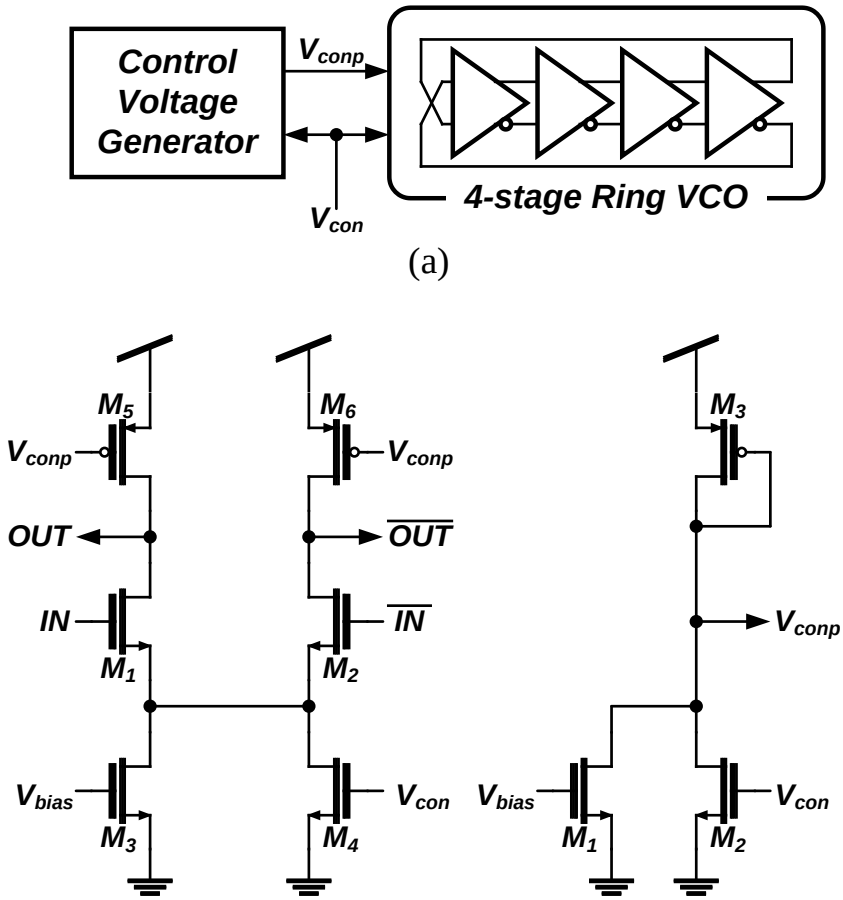


Figure 3.5 4-stage ring VCO; (a) block diagram (b) control voltage generator (c) delay cell.

B. Measurement

The prototype chip was fabricated using 60-nm CMOS technology. Figure 3.6 shows the layout of the prototype chip. The chip area of demodulator is 150 × 150 μm^2. To verify the operation of the prototype chip, 2.4-GSymbol/s QPSK signal using 4.8-GHz carrier frequency, which contains 4.8-Gb/s data in total, is generated by the arbitrary waveform generator (AWG). The fabricated chip consumes 54 mW from 1.2-V power supply at this carrier frequency. Figure 3.7 shows the eye-diagram of demodulated data for each I/Q channel. A single bit of demodulated data consists of 4 samples, which are sampled at rising and falling edges of each 4.8-GHz I/Q clock. Samples of demodulated I/Q data are misaligned by 1/4 period of 4.8-GHz clock since I/Q clock has 90 degree of phase difference. Input symbol transitions in “sample4” make two transition lines on the eye-diagram of Data1. This problem is due to the quantized timing error. Table I summarizes the performance of the fabricated chip.

The fabricated chip was tested for 60-GHz link, implemented with external components as shown in Figure 3.8. 40-dB attenuator models 1-meter of air loss in 60-GHz band using 15-dBi antenna at both Tx and Rx. The whole link has 2-GHz bandwidth and gives 4-dB loss as shown in Figure 3.9. Although a single LO provides RF clocks for both

Tx and Rx in the measurement setup, the proposed scheme is capable of tracking the frequency offset which inevitably appears between Tx and Rx in the super-heterodyne scheme. 1.7-GSymbol/s QPSK signal was generated for feasibility test of IEEE 802.15.3c using a band-limited QPSK modulator, which was implemented as shown in Figure 3.10. Each of two programmable pattern generators (PPGs) provides data for I or Q channel. Two PPGs have to be synchronized, since phase and frequency mismatch results in undesired symbol transitions in QPSK signals. Low pass filters limit their bandwidth and two mixers convert band-limited data to BPSK signal with 4.8-GHz LO signals. In one mixer, LO signals are 90° phase-shifted. Finally, combining two BPSK signals produces the desired QPSK signal. Figure 3.11 shows the measured BER vs. Tx output power curve. The fabricated chip achieved BER under 10^{-6} for larger Tx output power than 4.6 dBm. At this point, the spectrum of Tx output and the eye-diagram of demodulated data are respectively shown in Figure 3.12 and 13. Transition edges of eye-diagram are thick because of the quantized timing error. The BER floor appears at 10^{-7}, and is due to IQ mismatches in both Tx and Rx as well as phase noises of both RF and IF clocks. In addition, the required transmission power can be reduced by further optimization of RF link.

Table 3.2 Performance of prototype chip

Process	CMOS 60nm Logic
Maximum data rate	4.8Gb/s (total) 2.4 Gb/s (each I/Q)
Carrier frequency	4.8GHz
Area	1×1 mm^2 (including PAD) 150×150 μm^2 (demodulator) 50×90 μm^2 (VCO)
Supply voltage	1.2V
Power	54 mW (core + VCO)

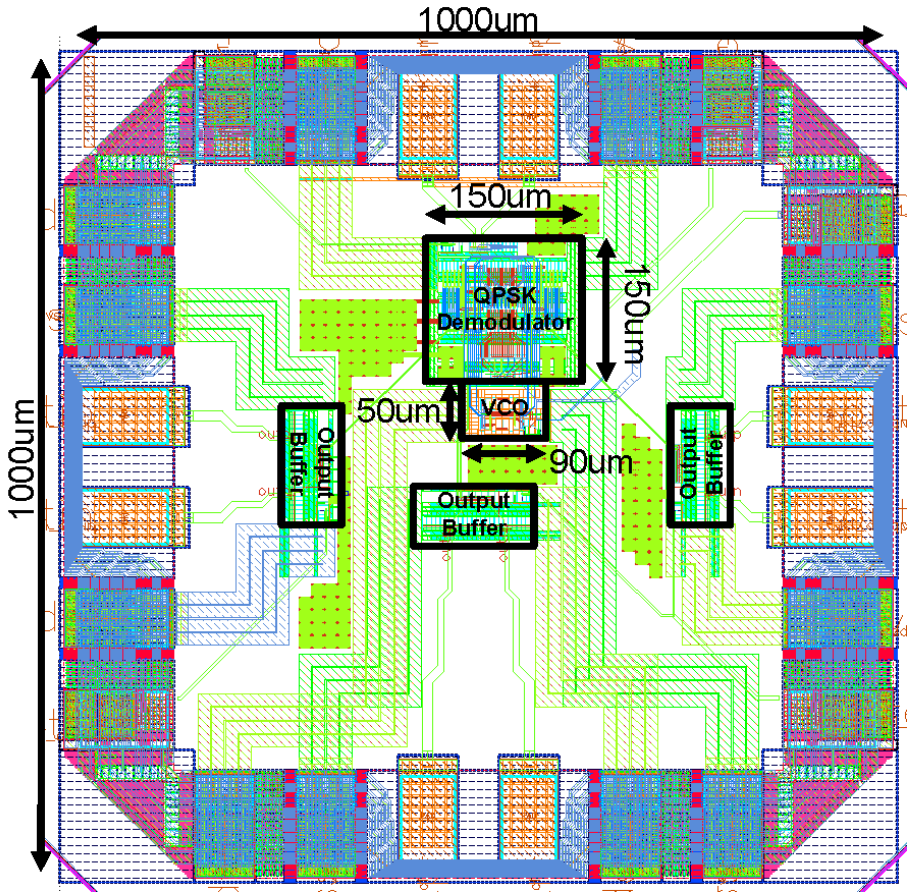


Figure 3.6 Layout of prototype chip.

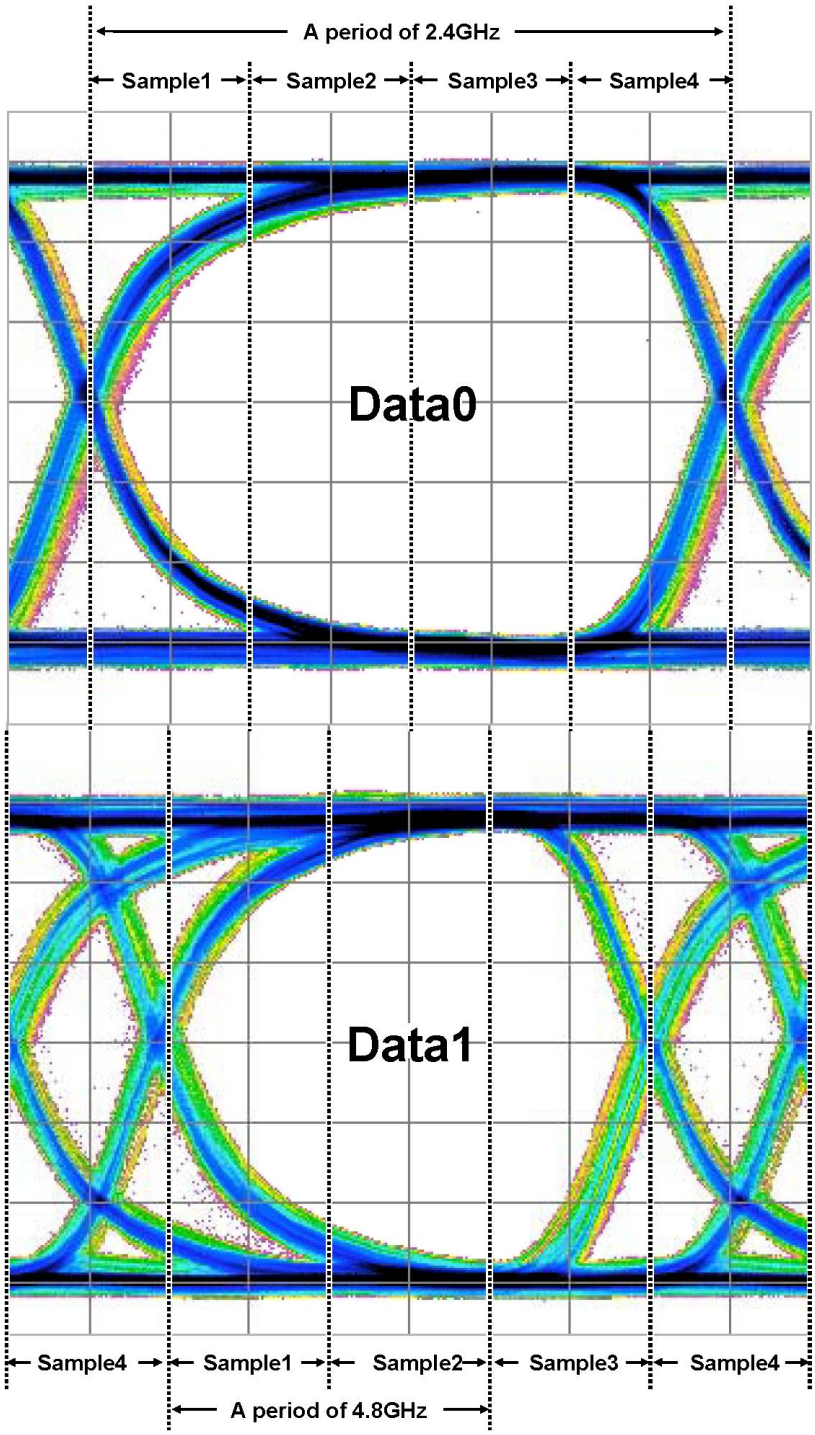
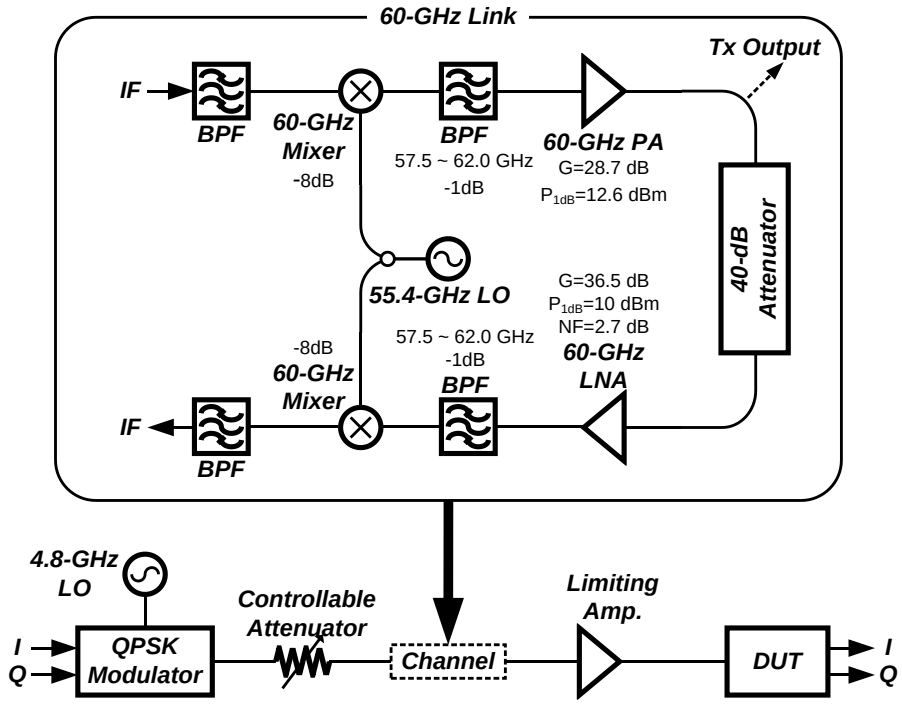
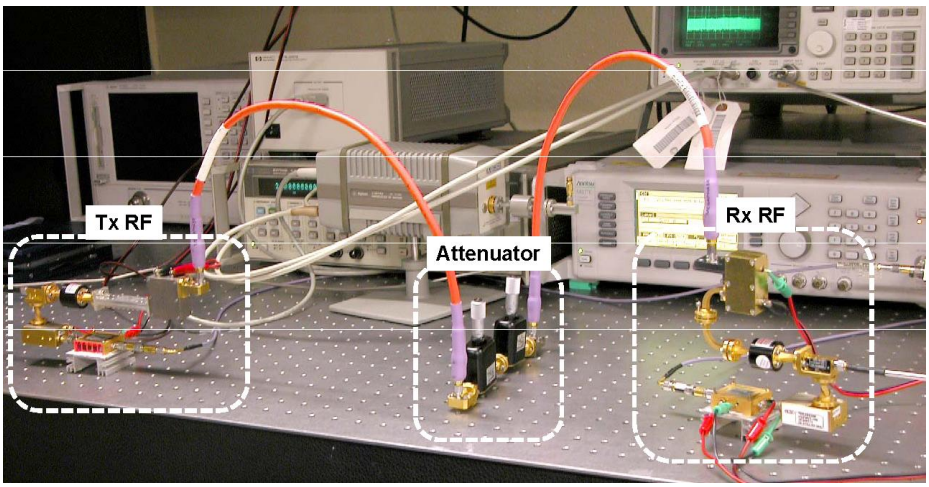


Figure 3.7 Eye-diagram of recovered data.



(a)



(b)

Figure 3.8 60GHz link measurement setup; (a) block diagram. (b) photograph.

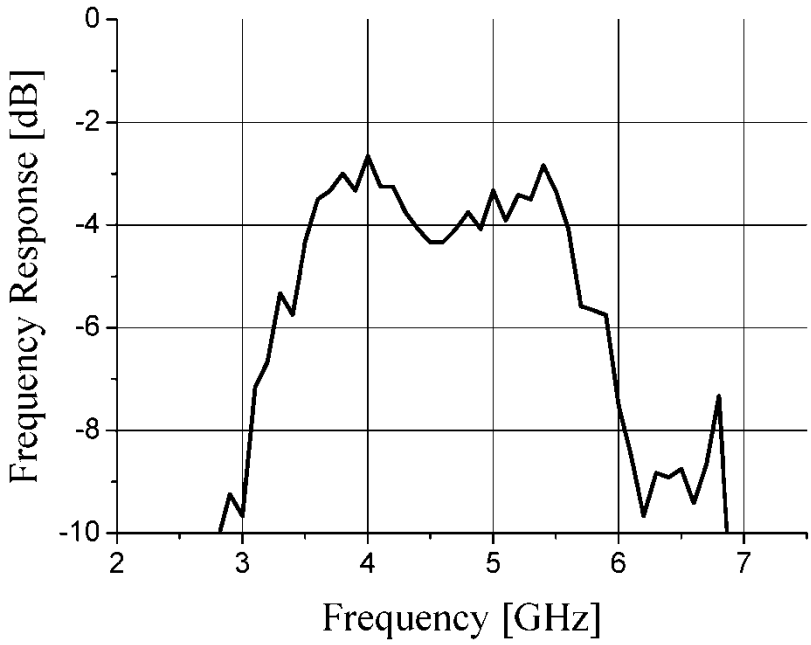


Figure 3.9 Frequency Response of 60GHz link.

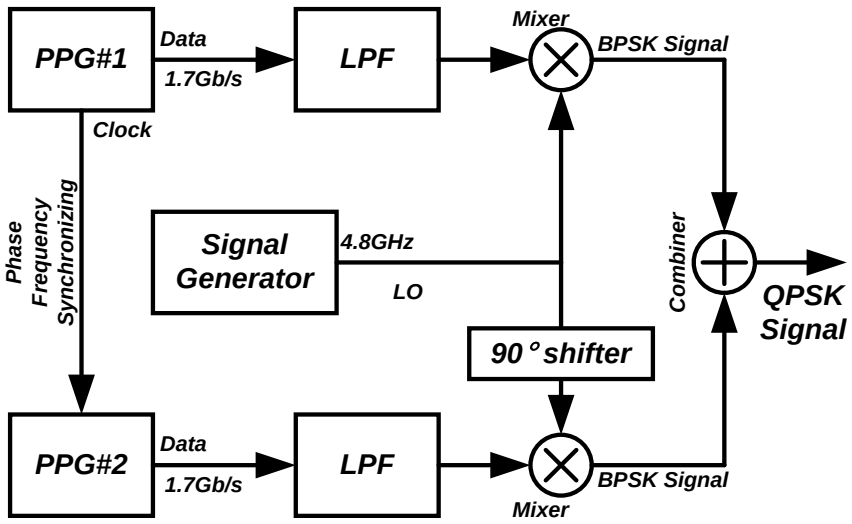


Figure 3.10 Block diagram of QPSK modulator.

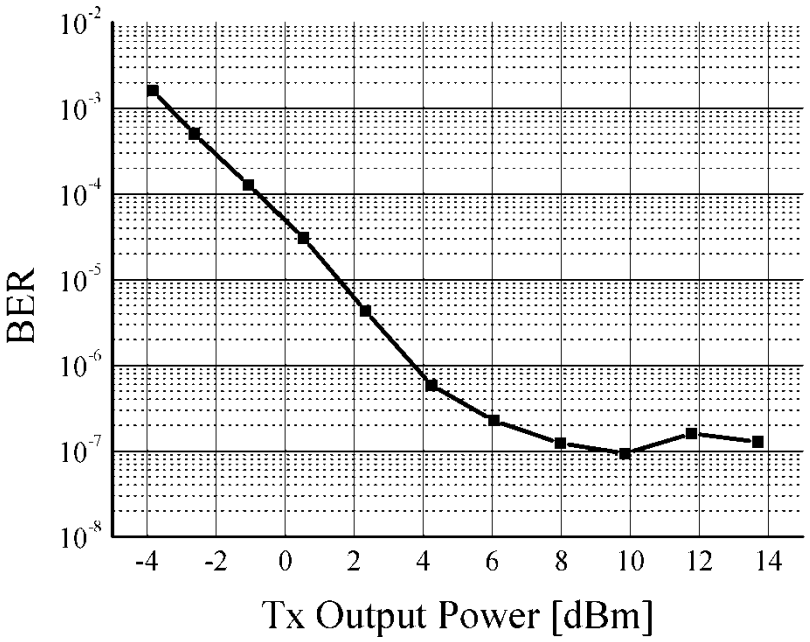


Figure 3.11 Measured BER vs. 60-GHz Tx output power.

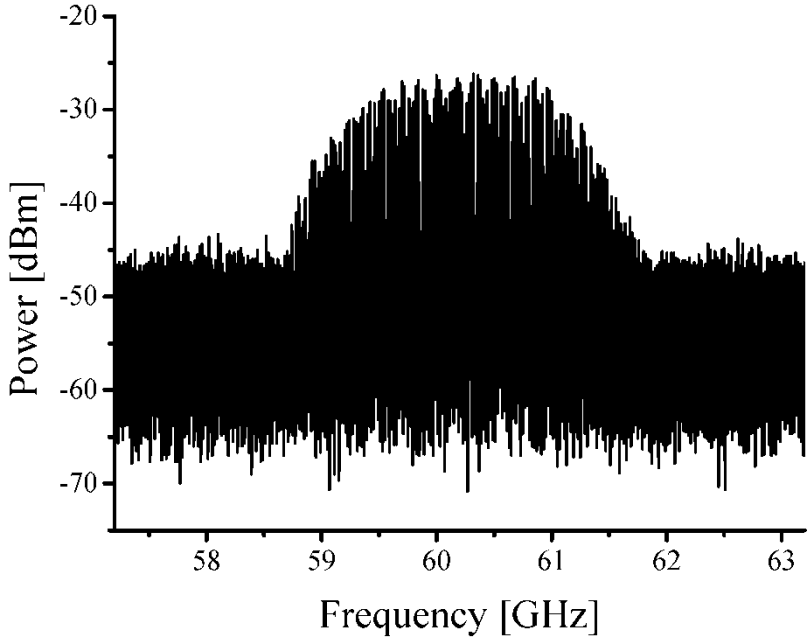


Figure 3.12 Output spectrum of 60-GHz Tx @ 4.6dBm output power.

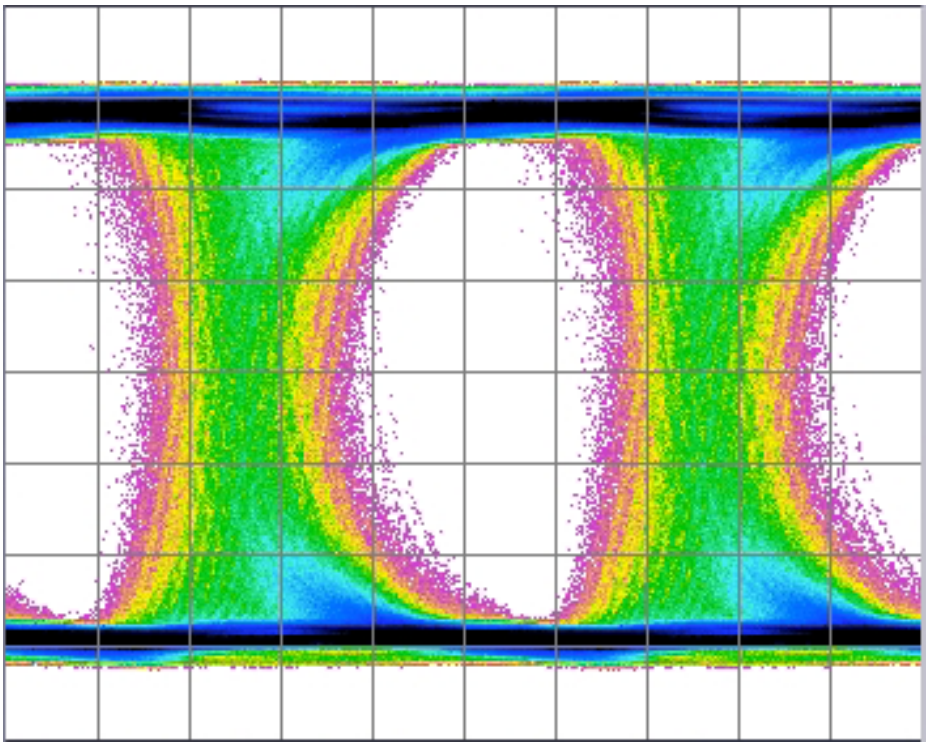
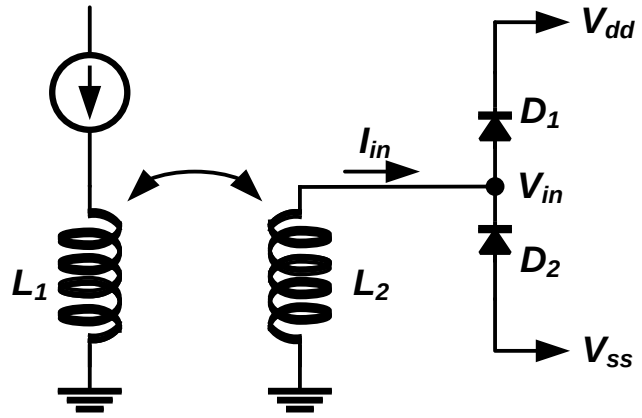


Figure 3.13 Eye-diagram of recovered data @ 4.6dBm output power.

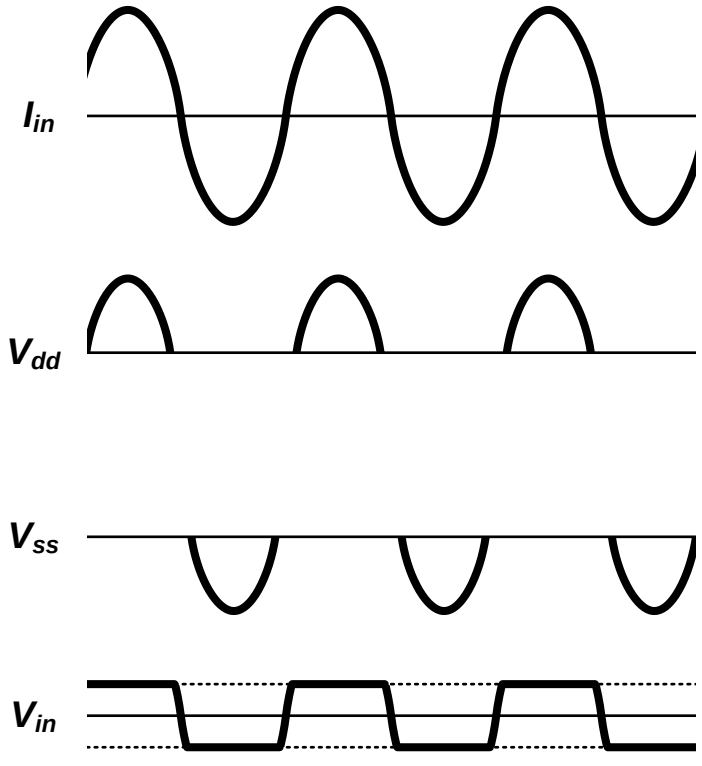
IV. Implementation-II: Retinal Prosthesis

In an inductive link for a retinal prosthesis, a rectifier-based power recovery, the basic schematic of which is illustrated in Figure 4.1 (a), distorts input signal. As shown in Figure 4.1 (b), the inductive coupled signal is transmitted as current, I_{in}, and D_1 and D_2 are turned-on when V_{in} is respectively higher than V_{th} and lower than -V_{th}. Then, V_{dd} and V_{ss} show chopped waveform for upper side than V_{th} and lower side than -V_{th}. V_{in} has the rest of chopped waveform that is similar to the result of clipping. That distorts amplitude information, therefore, IQ-demodulation cannot be applied. However, the proposed demodulation scheme considers only the timing of zero-crossing points, which are not changed by this problem, and is capable of demodulating high-order PSK signals while achieving low power consumption.

Additionally, switching orders of PSK is essential for the retinal prosthesis, because SNR of the transmission channel often changes. For example, when the patient is in motion, the channel SNR degrades but he may not require as much visual data. Consequently, less data transmission with low-order modulation requiring lower SNR can be sufficient. This function can be also realized by the proposed scheme and is included in the implementation of the prototype chip.



(a)



(b)

Figure 4.1 Input signal distortion by rectifier-based power recovery.

A. Circuit Implementation

The external unit should be also designed for low power consumption because it is also a mobile device. The one of main power consuming blocks is the power amplifier, and an E-class power amplifier is employed in this work because of its high power efficiency. The minimum Q-value (f_c/f_{BW}) of an E-class power amplifier is 1.8 [17], therefore, the maximum data rate is limited by carrier frequency. However, an inductive link carrying large electromagnetic power can cause damage to human body, and thus, the 5-MHz carrier frequency and 1.25-MSymbol/s symbol rate, which results 2 of Q-value, are selected.

Figure 4.2 shows the block diagram of prototype transmitter and receiver chips fabricated with TSMC 0.18μm RF process. The core supply voltage is lowered to 1.2V for low power consumption. The transmitter core consists of pattern generator, PSK modulator and PLL. The pattern generator generates four 1.25Mb/s parallel data streams, which are 1:4-deserialized from 5Mb/s 2^7-1 PRBS pattern. PSK modulator can select the operation mode (BPSK, QPSK, 8PSK or 16PSK). PLL provides multiphase clocks to PSK modulator and the pattern generator. The receiver uses differential signaling to avoid 2nd-order distortions and achieve supply noise immunity. The input signal

is 1bit-sampled by 16 multiphase clocks generated from VCO to support up to 16PSK operation. Sampled data are processed in the digital domain for detecting the symbol and extracting phase information. Phase and frequency detector (PFD) unit offers up or down signal to the charge pump so that the phase of VCO is phase-locked to the input signal for coherent operation. A digital CDR is employed to reject any ISI. The PSK decoder, which can be switched into BPSK, QPSK, 8PSK or 16PSK mode by an external control, produces demodulated symbols as parallel data streams. Pattern generator, PSK modulator, CDR, PSK decoder and PFD unit are all implemented by auto P&R using standard logic cells. The power recovery circuit consists of rectifier, bias generator with a start-up circuit, and 1.2V regulator.

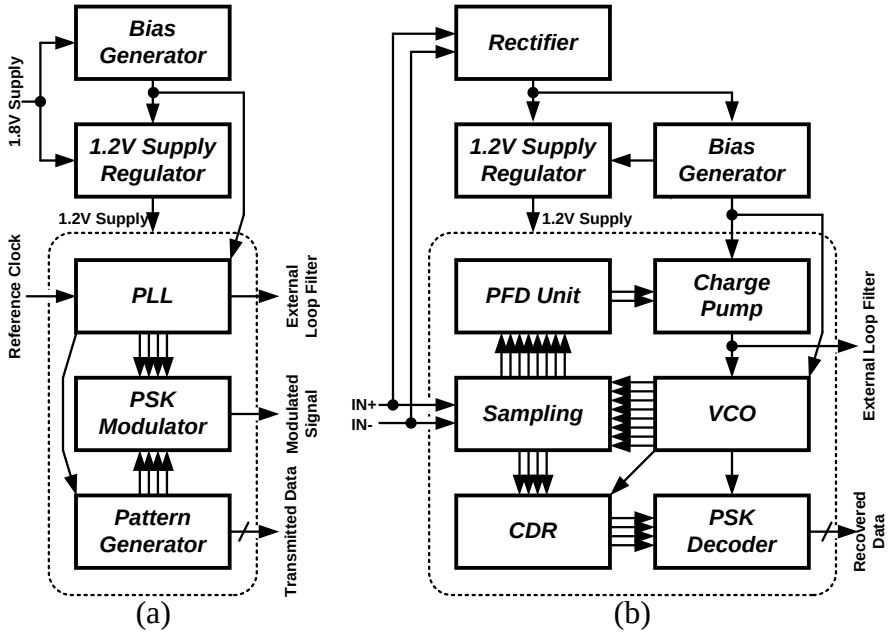


Figure 4.2 Block diagram of prototype chips. (a) Transmitter. (b) Receiver.

A. 1. Sampling Block

Figure 4.3 is the block diagram of sampling block. There are two kinds of differential-type samplers, CML-latch-based and sense-amplifier-based flip-flops [26]. [27] reported that CML-latch-based flip-flops provide higher gain, while sense-amplifier-based flip-flops achieve superior time resolution capacity. However, input signal carrying power is over rail-to-rail of receiver circuit, therefore, sense-amplifier-based flip-flops shown in Figure 4.4 are employed. After sampled with each multiphase clock, sampled data are aligned to $CK_{ref\,0}$ or $\overline{CK_{ref0}}$ with D-flip-flops for parallel processing. To improve resolution between samples, input signal is sampled at both rising and falling edges. Since samples at falling edges are inversion of samples at rising edges for identical symbols, inverted outputs of SAFF are used. $S_{r,sym\,0}$ and $S_{f,sym\,0}$ are re-sampled by respectively opposite clocks, $CK_{ref\,0}$, and $\overline{CK_{ref0}}$, to offer the last phase information of previous sample set to PFD unit. Consequently, 8 sample sets are gathered within a period for 1.25-MSymbol/s data with 5-MHz double-edge-triggered sampling.

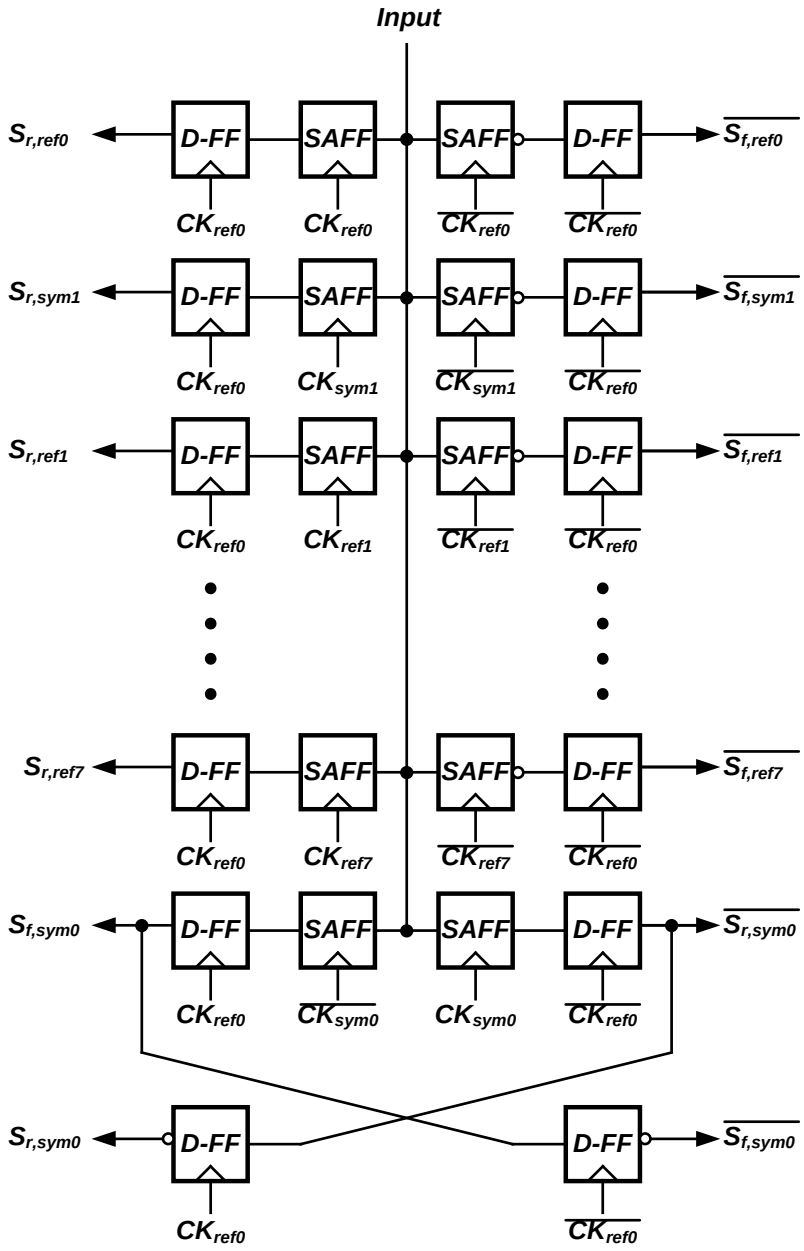


Figure 4.3 Block diagram of sampling block.

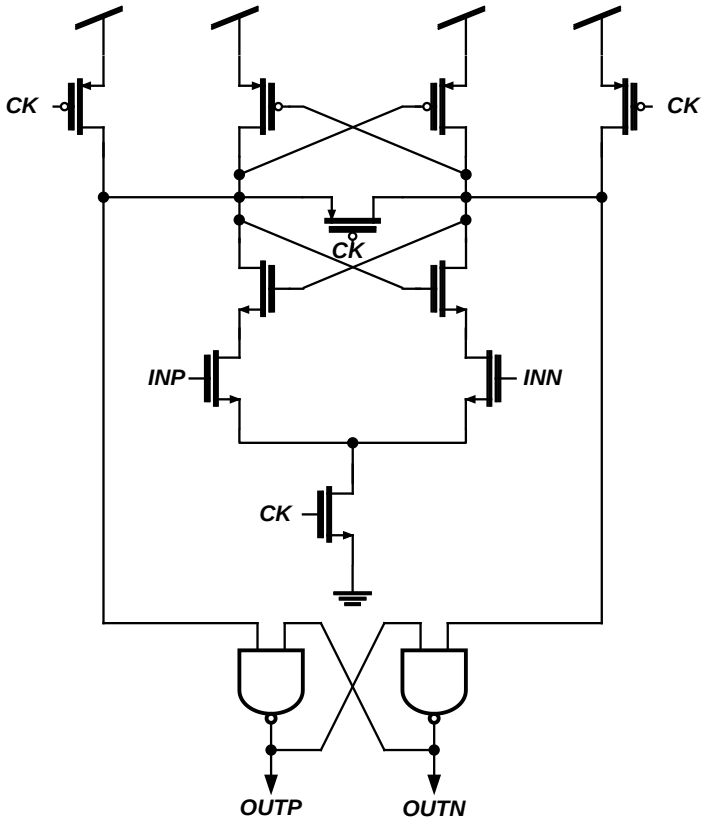


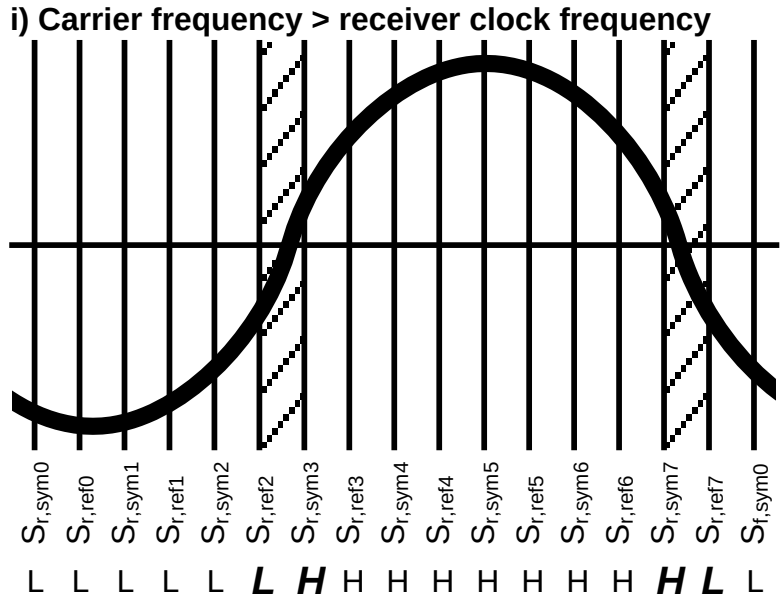
Figure 4.4 Schematic of sense-amplifier-based flip-flop.

A. 2. PFD Unit

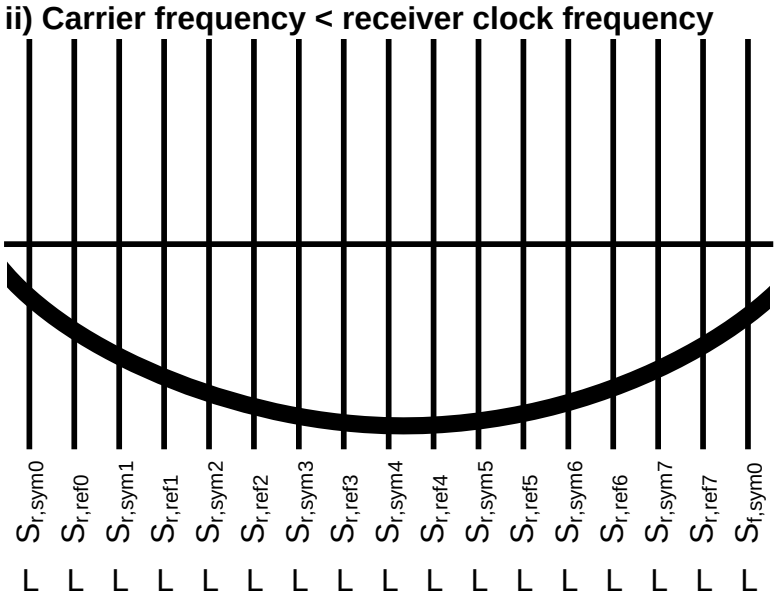
In order to achieve initial phase and frequency acquisition without a reference oscillator in the implanted unit, the initial training period is required. Before data transmission, the prototype transmitter sends the sinusoidal wave having the phase of symbol '0' to wake up device and achieve frequency acquisition. After that, the receiver aligns its clock phase to the input sinusoidal wave, since symbol decision is done by relative phase to the initial phase. Although this period can be removed by employing differential PSK (DPSK) scheme, it requires additional hardware resulting additional power consumption.

Figure 4.5 shows the operation of PFD unit. The sampling unit gathers 16 samples at each rising or falling edges. If the frequency of input signal is higher than the frequency of receiver clocks, more than one zero-crossing (between $S_{r,ref\ 2}$ and $S_{r,sym\ 3}$, and between $S_{r,sym\ 7}$ and $S_{f,sym\ 0}$) appear as shown in Figure 4.5 (a). If the input frequency is lower than receiver clock frequency, no zero-crossing appears as shown in Figure 4.5 (b). Thus, frequency is detected by detecting and counting zero-crossings, which are found by XOR gates using two adjacent samples as inputs. After frequency acquisition, the receiver aligns the phase of $CK_{sym\ 0}$ to the input phase. As shown in Figure 4.5 (c) and (d), $S_{r,sym\ 0}$ is low when the phase of $CK_{sym\ 0}$ is earlier, and high when later

than the phase of the input signal. Finally, multiple PDs operate as mentioned in Section II to maintain locked state for input symbols. Figure 4.5 (e) and (f) is the case that the input symbol is ‘0011’ in the 16PSK mode. $S_{r,ref\,1}$ and $S_{r,ref\,2}$ have different value and that indicate the input symbol is ‘0011’ so that only PD2 outputs, and $S_{r,sym\,2}$ represents phase information.

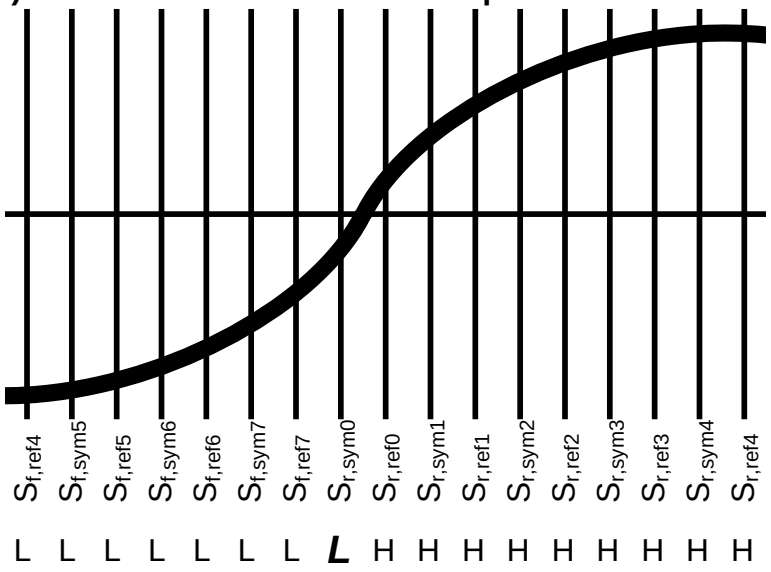

i) Carrier frequency > receiver clock frequency
Sr,sym0
Sr,ref0
Sr,sym1
Sr,ref1
Sr,sym2
Sr,ref2
Sr,sym3
Sr,ref3
Sr,sym4
Sr,ref4
Sr,sym5
Sr,ref5
Sr,sym6
Sr,ref6
Sr,sym7
Sr,ref7
Sf,sym0
L L L L L L H H H H H H H H L L

(a)


ii) Carrier frequency < receiver clock frequency
Sr,sym0
Sr,ref0
Sr,sym1
Sr,ref1
Sr,sym2
Sr,ref2
Sr,sym3
Sr,ref3
Sr,sym4
Sr,ref4
Sr,sym5
Sr,ref5
Sr,sym6
Sr,ref6
Sr,sym7
Sr,ref7
Sf,sym0
L L L L L L L L L L L L L L L L

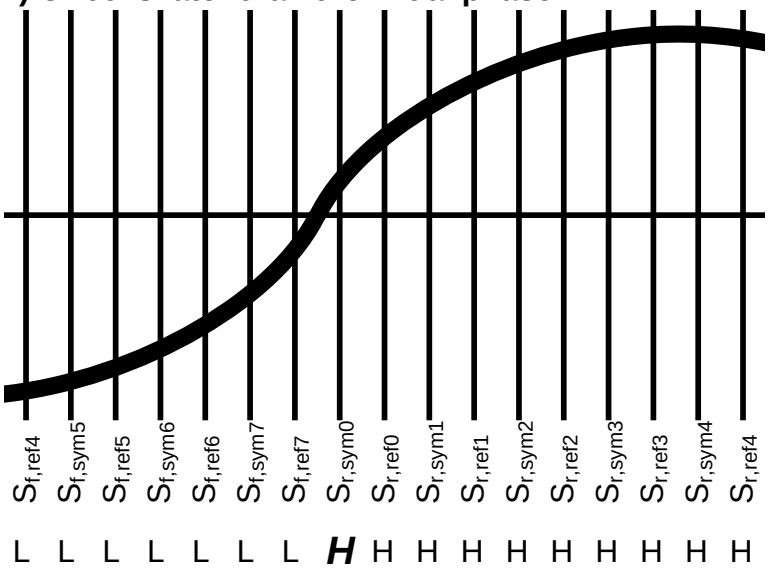
(b)

i) CK00 is earlier than the initial phase

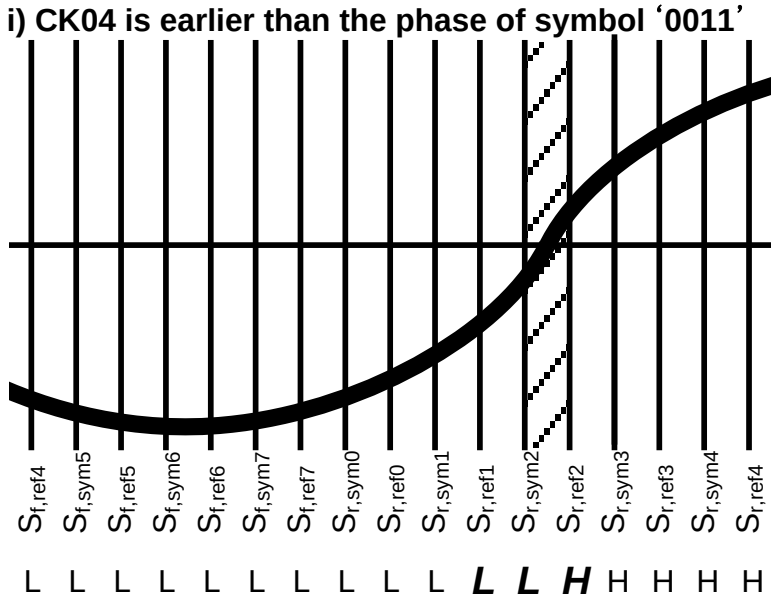


(c)

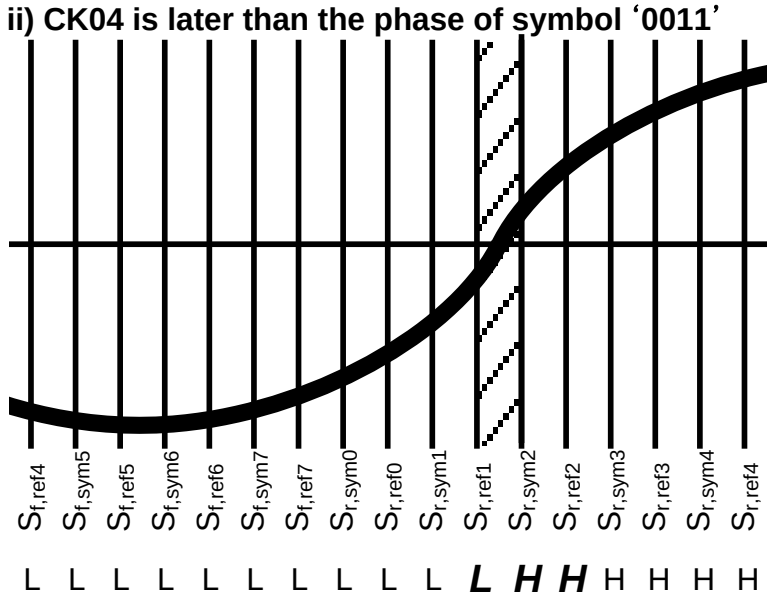
ii) CK00 is later than the initial phase



(d)



(e)



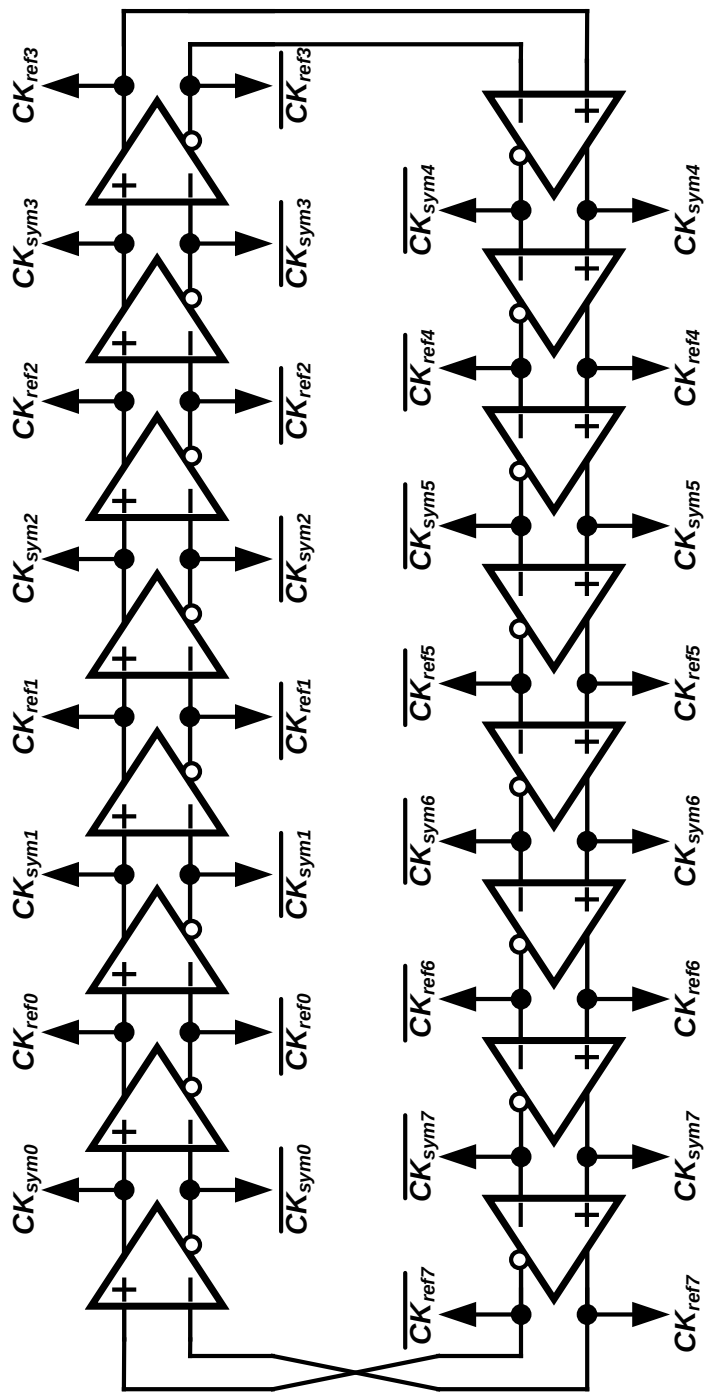
(f)

Figure 4.5 Operation of PFD unit.

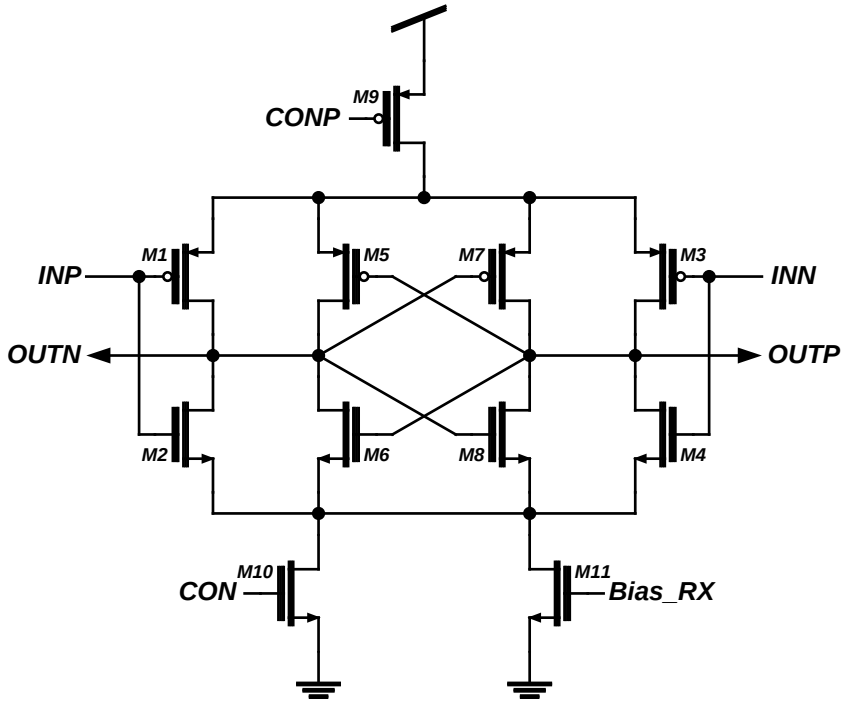
A. 3. VCO & Charge Pump

Since the proposed demodulation scheme requires 16 multiphase clocks for 16PSK mode, 16-stage ring-type VCO shown in Figure 4.6 (a) is employed in this work. Figure 4.6 (b) shows the schematic of a voltage controlled delay cell implemented by pseudo-differential type to provide differential clocks. The delay is controlled by changing the current using M9-11. To reduce mismatch between rising and falling time, *CONP* is generated by control circuit shown in Figure 4.6 (c).

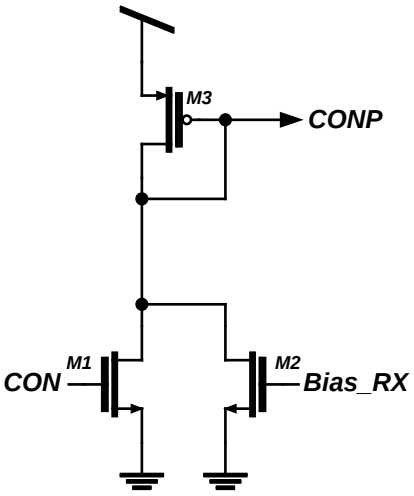
Figure 4.7 is the schematic of the charge pump and 2nd-order loop filter. The digital PD operates synchronously and outputs up or down signal as long as a period, therefore, current mismatch affects more than linear type phase detector such as PFD in a conventional PLL. In order to reduce mismatch between up and down currents, negative feedback is employed. Since a bang-bang type phase detector usually requires large capacitance, the loop filter is not included in the prototype chip.


CK_{ref3}
$\overline{CK}_{ref3}$
CK_{sym3}
$\overline{CK}_{sym3}$
CK_{ref2}
$\overline{CK}_{ref2}$
CK_{sym2}
$\overline{CK}_{sym2}$
CK_{ref1}
$\overline{CK}_{ref1}$
CK_{sym1}
$\overline{CK}_{sym1}$
CK_{ref0}
$\overline{CK}_{ref0}$
CK_{sym0}
$\overline{CK}_{sym0}$
$\overline{CK}_{ref7}$
CK_{ref7}
$\overline{CK}_{sym7}$
CK_{sym7}
$\overline{CK}_{ref6}$
CK_{ref6}
$\overline{CK}_{sym6}$
CK_{sym6}
$\overline{CK}_{ref5}$
CK_{ref5}
$\overline{CK}_{sym5}$
CK_{sym5}
$\overline{CK}_{ref4}$
CK_{ref4}
$\overline{CK}_{sym4}$
CK_{sym4}

(a)



(b)



(c)

Figure 4.6 Schematic of 16-stage ring VCO.

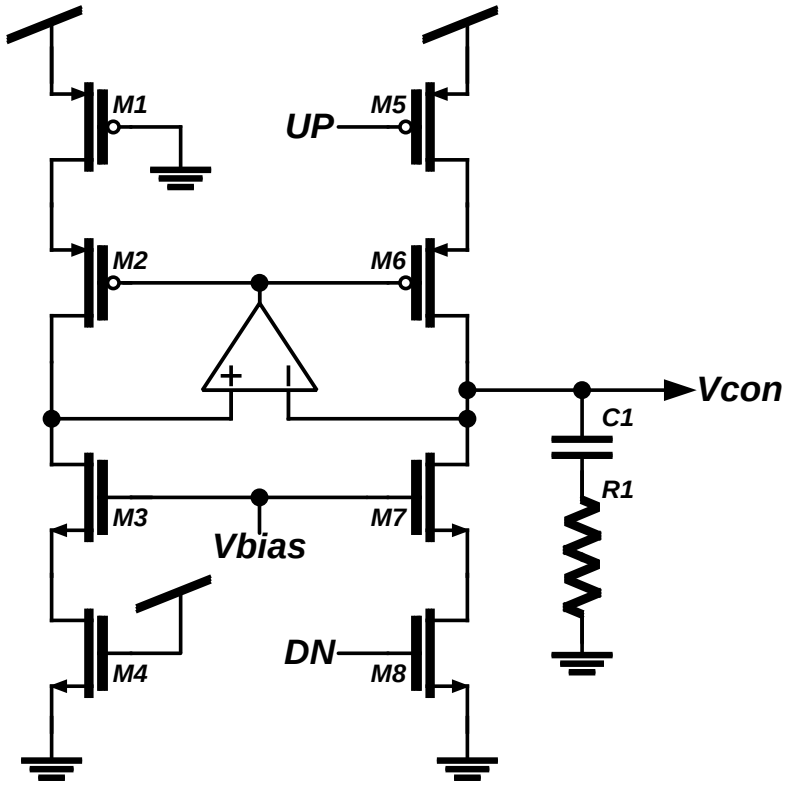


Figure 4.7 Schematic of charge pump.

A. 4. Clock and Data Recovery

Since the receiver gathers 8 sample sets per one symbol period, it is easier to use a digital CDR. Figure 4.8 shows the operation of CDR. The input signal is sampled by 5-MHz multiphase clocks resulting in 8 sample sets, *SET0-7*. Transitions are detected by recognizing difference between two adjacent sample sets. Since the input signal contains noise and ISI, transitions usually appear around, not only at, symbol transitions as shown in the figure. Consequently, the transition point has to be confirmed by voting. The figure shows the case that the result indicates between *SET7* and *SET0*. Although, the minimum error point is the farthest sample set from the transition point, even-number oversampling does not sample at the farthest point from the transition point. For example, it is located between *SET3* and *SET4* in the figure. In the prototype chip, the later one, *SET4* in the figure, is selected as the data-decision point. The above flow is same as that of a conventional feed-forward oversampling CDR [28], which stores sampled values until the data-decision point is found so that the delay occurs inevitably. However, this delay is critical to the retinal prosthesis, because the sight should be updated immediately. In this work, the present symbol is decided by the data-decision point found from previous symbols, and output immediately.

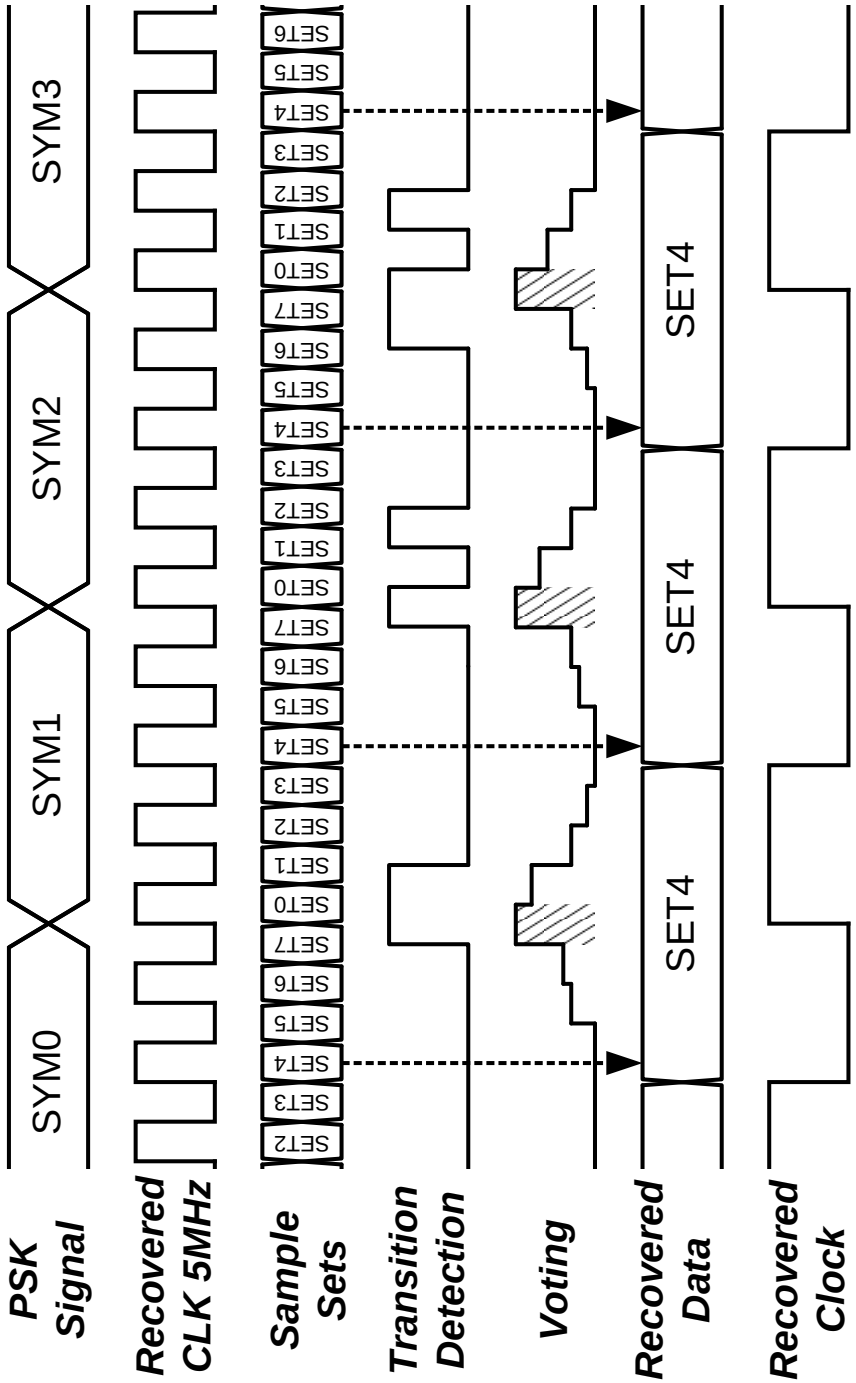


Figure 4.8 Operation of CDR.

A. 5. Power Recovery Circuit

Figure 4.9 is the schematic of the power recovery circuit that consists of rectifier, bias generator with start-up circuit, and regulator. Since the rectifier provides DC voltage with large fluctuation because of the input signal, the supply voltage, V_{DD}, is regulated referencing the output of bias generator having high immunity to supply noise. V_{bias} is also used for current bias voltage of VCO and charge pump.

The rectifier is implemented for differential inputs as well as sampler. When the voltage of *INP* is higher than that of *INN*, M1 and M4 turn on and *INP* is connected to high rail while *INN* is connected to low rail, *VSS*. The rectified voltage is smoothed by C1. Since the rectifier treats high voltage so that large substrate noise is generated, M1-4 is isolated by deep N-well layer. The bias generator employed boot-strap structure. To reduce fluctuation on V_{bias} by noisy supply voltage, 1:40 of current ratio is selected [29], thus the simulated supply dependency of V_{bias} is less than 1%. M5-6 and C2-3 is added to start up the bias generator. M11-12 isolates the generated bias voltage from ac-coupled noise from next stages, VCO and charge pump. Finally, the rectified voltage is regulated referencing V_{bias} at the regulator.

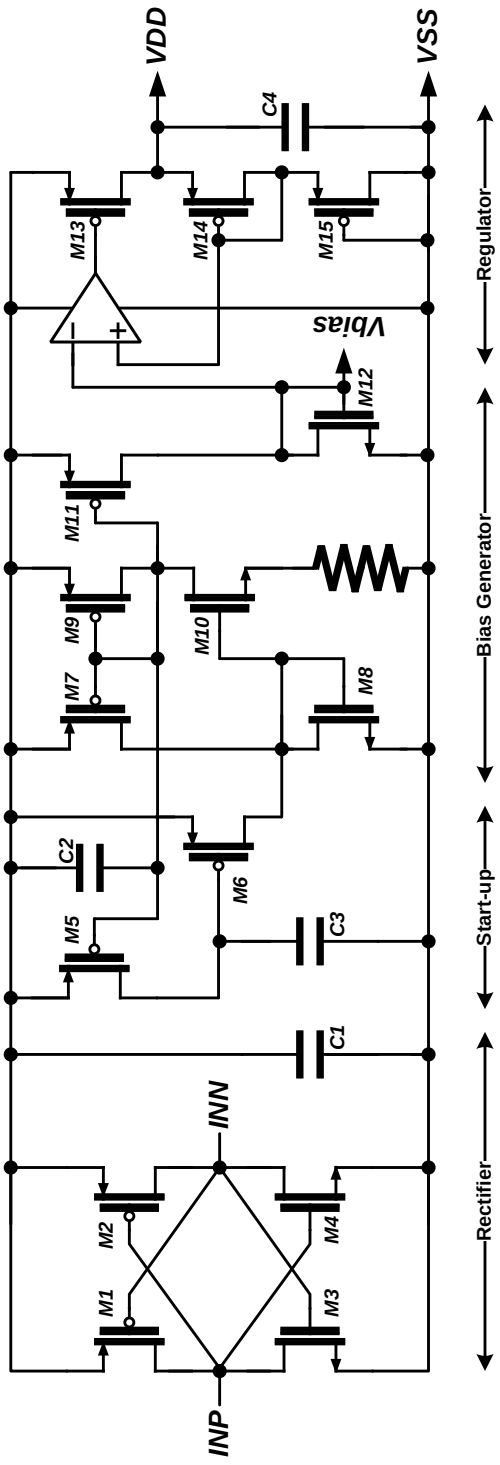


Figure 4.9 Schematic of power recovery circuit.

B. Measurement

Figure 4.10 shows die photographs of transmitter and receiver chips, which occupy respectively $135\times160\mu m^2$ and $240\times385\mu m^2$. To verify the proposed demodulation scheme, fabricated transmitter and receiver chips were directly connected. The receiver chip successfully demodulated 1.25-MSymbol/s 16PSK signal modulated by 5-MHz carrier, resulting total 5Mb/s data, in back-to-back measurement while consuming 145μA from 1.2V regulated supply. The transmitter chip consumes 110μA and the receiver 140μA from 1.2V regulated supply. For receiver power measurement, a prototype receiver chip having no power recovery function was used. Figure 4.11 shows 4 transmitted (upper) and recovered (lower) parallel data streams for 16PSK. The performance of our receiver is compared with that of previously reported inductive-link receivers [7-10] in Table 4.1. This work achieves the highest data rate while consuming the lowest power and occupying the smallest area, even though it includes CDR.

A link test with 0.5cm inductive link was performed with the fabricated transmitter and receiver chips. Figure 4.12 shows the measurement scheme. The power amplifier was implemented with commercial discrete devices with the target of Q-factor 2. Integration of the power amplifier with the transmitter was not possible since the

fabrication did not support high-voltage devices. Coupling coils were realized with Litz wires in order to reduce losses by the skin effect. The estimated transmitted output power produced by the power amplifier was 187mW. Two capacitors in series were added at the receiver to set the resonant frequency for 5MHz. The recovered supply voltage at the receiver was 1.46V, which was regulated to 1.17V for the core supply voltage. The link successfully achieved transmission of 1.25MSymbol/s BPSK, QPSK and 8PSK signals, resulting in 3.75Mb/s in total for 8PSK mode. Figure 4.13 shows (a)-(c) 3 transmitted and recovered parallel data streams for 8PSK, and (d) the recovered data eye-diagram and the recovered clock signal. The rising edge of recovered clock is aligned to the center of recovered data.

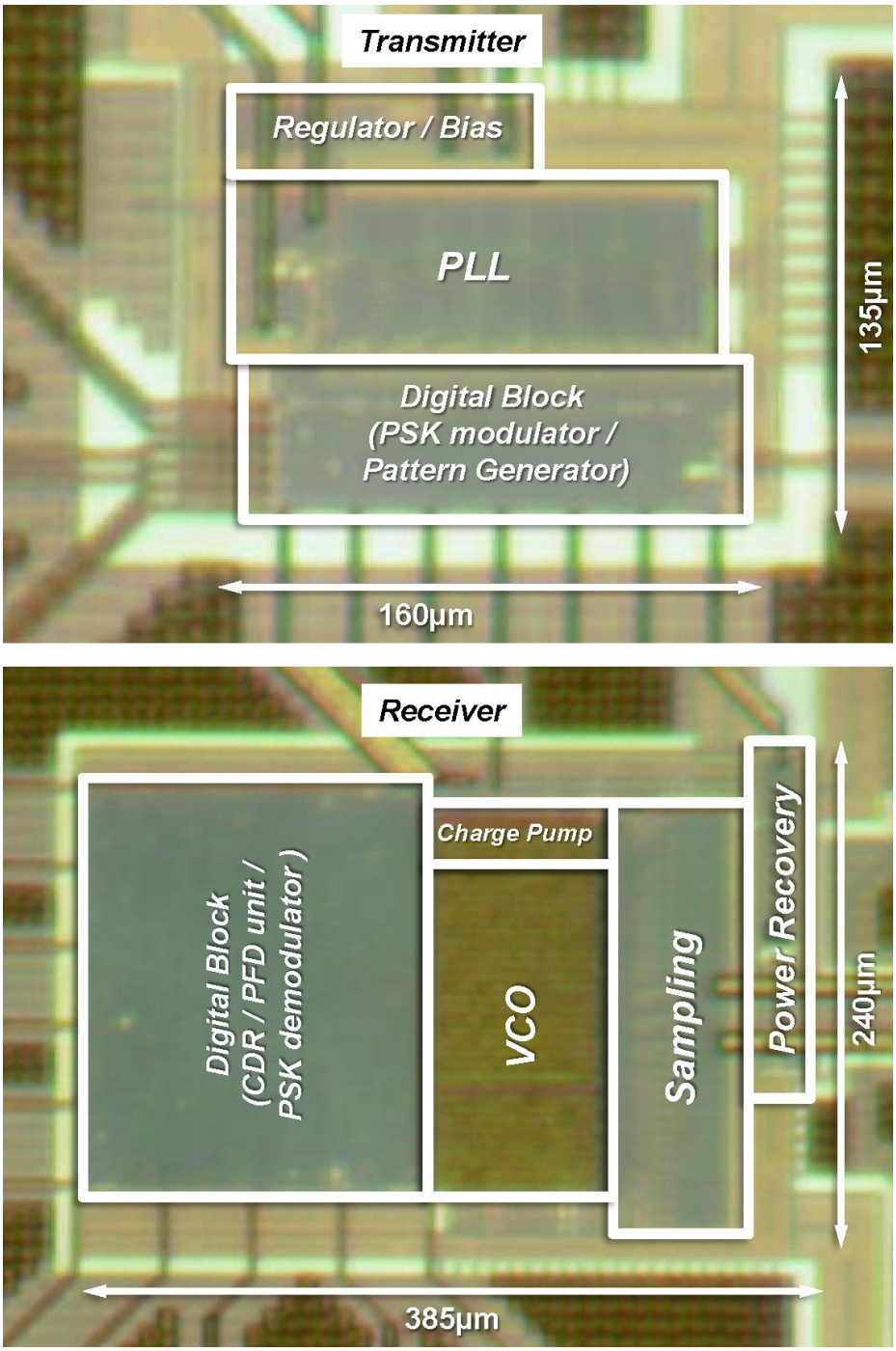


Figure 4.10 Die photographs of prototype transmitter and receiver.

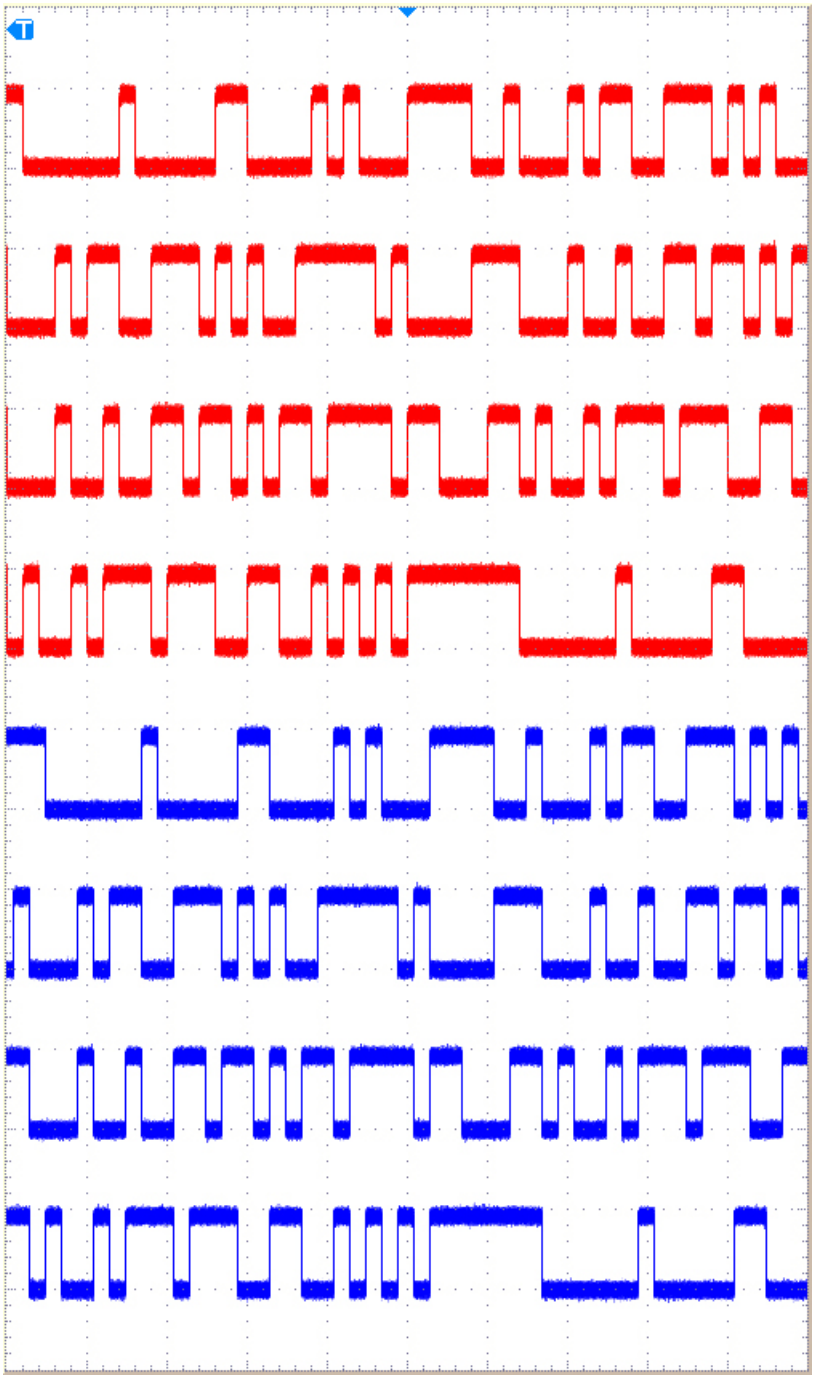
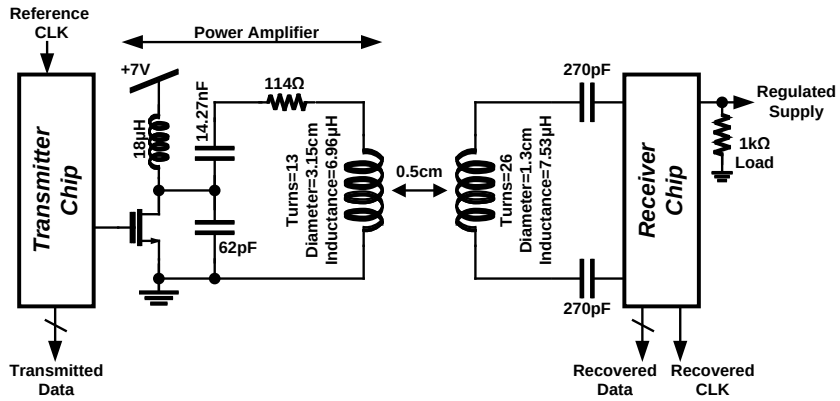


Figure 4.11 Demodulation of 16PSK in back-to-back measurement. (X: 4μs/div, Y: 2V/div).

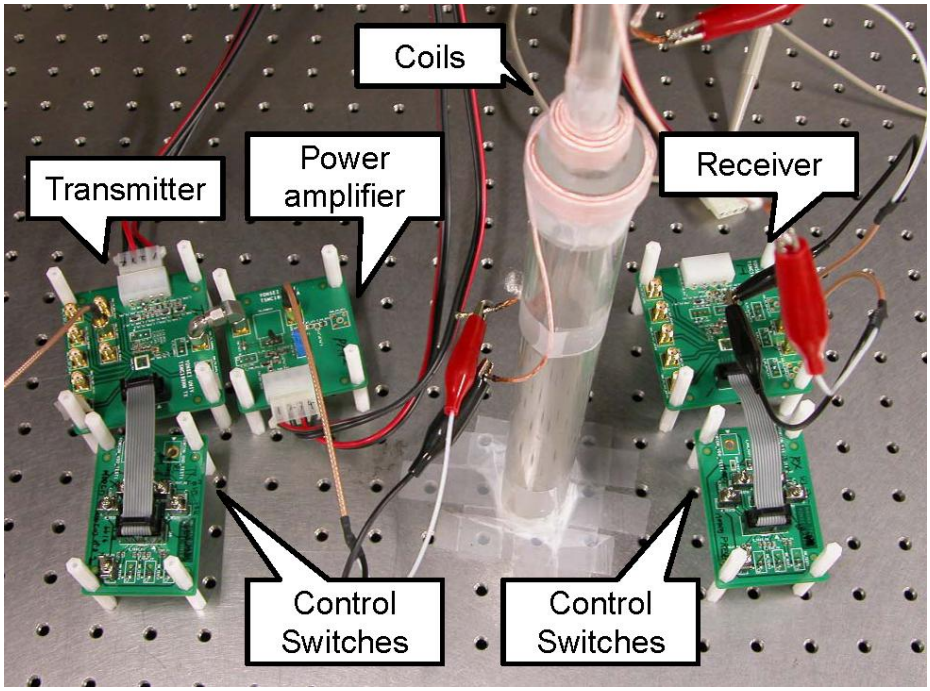
	[7]	[8]	[9]	[10]	**This Work**
Process [μm]	1.5	0.18	0.5	0.35	**0.18**
Modulation	FSK	BPSK	BPSK	DPSK	**BPSK/ QPSK/ 8PSK/ 16PSK**
Maximum data rate [Mb/s]	2.5	1.12	0.02	2	**5 (16PSK)**
Carrier frequency [MHz]	7.5	10	13.56	20	**5**
Power consumption [mW]	0.38	0.61	3	6.2	***0.168**
Supply voltage [V]	5	1.8	3.3	3.3	**1.2**
Area of receiver [mm^2]	0.29	0.19	1	4.42	***0.0924**

*: including CDR

Table 4.1 Performance comparison with previous works

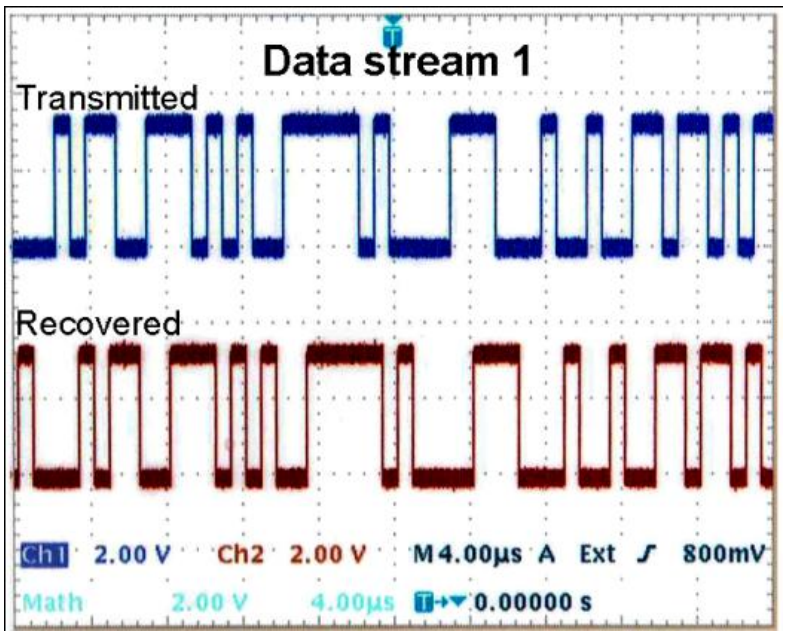


(a)

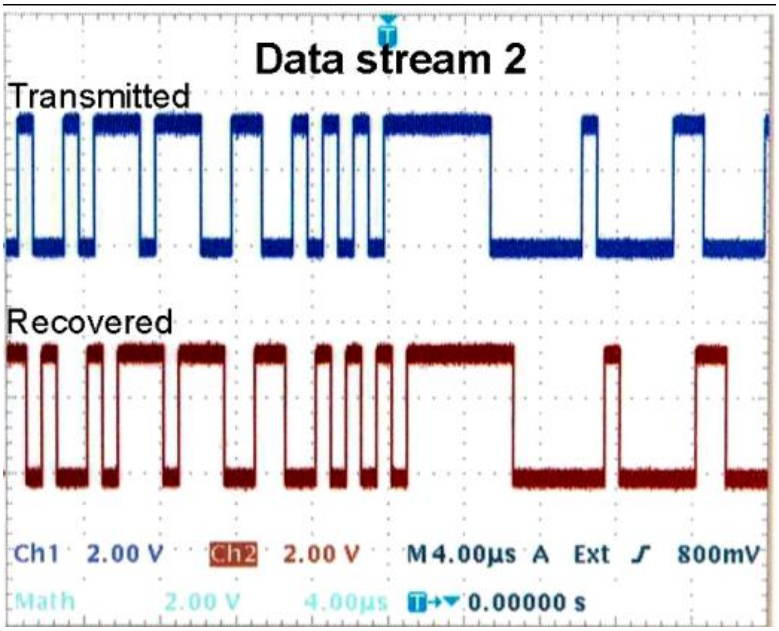


(b)

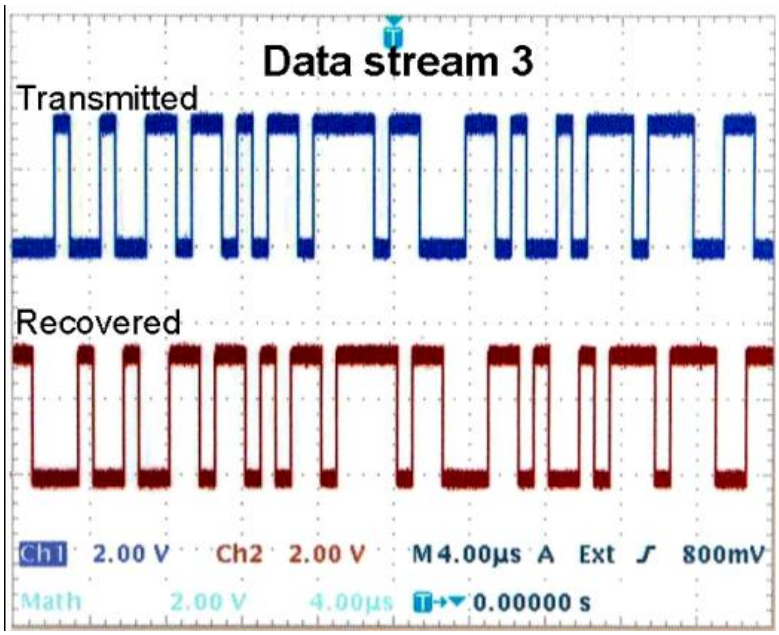
Figure 4.12 Measurement setup.


Data stream 1
Transmitted
Recovered
Ch1 2.00 V
Ch2 2.00 V
M4.00µs A Ext 800mV
Math 2.00 V 4.00µs 0.00000 s

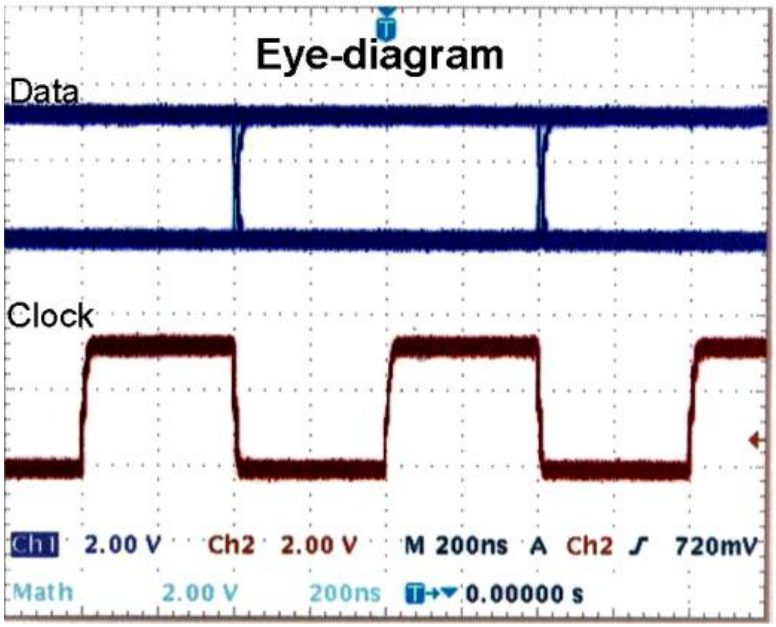
(a)


Data stream 2
Transmitted
Recovered
Ch1 2.00 V
Ch2 2.00 V
M4.00µs A Ext 800mV
Math 2.00 V 4.00µs 0.00000 s

(b)



(c)



(d)

Figure 4.13 Demodulation of 8PSK with 0.5-cm inductive link.

V. Conclusion

A novel PSK demodulation scheme is demonstrated that can be used for applications requiring low power consumption. In this scheme, demodulation is performed by 2 steps, phase-comparison by 1bit-sampling using multiphase clocks and decoding sampled results. The proposed scheme is not affected by amplitude distortions such as quantization noise of ADC and clipping of amplifiers, because it requires timing information of zero-crossing points not amplitude information. It also enables an ADC-less receiver structure so that low power consumption can be achieved. Additionally, 1-bit sampling operates at higher speed than a multi-bit-sampling ADC that is bottle-neck for high-speed performance. To verify the proposed scheme, 2 applications, which target respectively high-speed operation and low-power consumption, are demonstrated.

Mobile device file downloading using 60-GHz band requires Gb/s data transmission, however, demodulators operating at this speed are difficult to implement using the conventional IQ-demodulation scheme since ADC limits the operation speed. Although the proposed scheme cannot provide enough information for channel equalization, it is applicable to this application because non-fading channel is guaranteed

using a directional antenna. The prototype chip achieved demodulation of 4.8-Gb/s QPSK signal using 4.8-GHz carrier frequency, and is also tested on 1-m 60-GHz link transmitting 1.7-GSymbol/s of QPSK signal.

A retinal prosthesis is an implantable device, thus, required to operate with low power consumption. Usual implementations using power transmission by electro-magnetic wave suffer from distortion caused by rectifier-based power recovery, consequently, conventional IQ demodulation scheme is not feasible. However, the prototype chip is not affected by such a distortion, thus, improve data rate by using high-order PSK modulations. The prototype chip achieved 3.75Mb/s of 8PSK signal transmission while consuming the smallest power in inductive link receivers ever reported.

Conclusively, the proposed scheme is verified that it can achieve both low power consumption and high-speed capability and ease the burden of RF circuits.

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국문요약

1비트 샘플링 위상비교를 이용한 새로운 구조의 PSK 복조방법

일반적인 구조의 IQ-복조방식은 양자화잡음이나 clipping과 같은 non-ideality에 의해 성능이 열화되며, ADC를 사용하여 구현되므로 많은 전력을 소모한다. 본 논문에서는 이런 문제를 극복하기 위해 새로운 구조의 PSK 복조방식을 제안한다.

제안된 복조방식에서는, 입력신호의 위상을 여러 개의 기준 위상들과 비교하고, 이를 통하여 입력 심볼을 복원한다. 위상 비교는 time domain에서 복수 위상 클럭을 이용하는 1비트 샘플링으로 구현된다. 제안된 방식의 비트에러율이 분석되며, 크기 정보의 왜곡에 영향 받지 않음을 검증한다.

제안된 복조 방식을 검증하기 위해, 60GHz 대역 WPAN과 망막보철의 두 가지 응용분야에 대해 수신기를 구현하고, 성능을 평가한다.