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Study on High-k Gate Oxides of $In_{0.53}Ga_{0.47}As$ Photo-FET Fabricated by Wafer Bonding Technique on Si Substrate

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This certifies that the master’s thesis of Sung-Han Jeon is approved.

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List of Abbreviations

ALD	:	Atomic Layer Deposition
APD	:	Avalanche Photo Diode
BEOL	:	Back end of line
BJT	:	Bipolar Junction Transistor
BOE	:	Buffered Oxide Etch
CCP	:	Capacitively Coupled Plasma
CET	:	Capacitance equivalent thickness
CMOS	:	Complementary Metal Oxide Semiconductor
Cox	:	Capacitor oxide semiconductor
CVD	:	Chemical Vapor Deposition
Dit	:	Interface Trap density
DRAM	:	Dynamic Random Access Memory
EOT	:	Equivalent oxide thickness
hf	:	High Frequency
HF	:	hydrogen fluoride
ICP	:	Inductively Coupled Plasma
JFET	:	Junction Field-effect Transistor
LiDAR	:	Laser Detection And Ranging
lf	:	Low Frequency
Nfix	:	Slow Trap density
MOSFET	:	Metal-Oxide-Semiconductor Field-Effect Transistor
PDA	:	Post Deposition Annealing

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PIN	:	Positive Intrinsic Negative
PMA	:	Post Metal Annealing
RIE	:	Reactive Ion Etching
ROIC	:	Readout integrated circuit
SWIR	:	Short Wave InfraRed
TDS	:	Thermal desorption spectroscopy
TEMAHf	:	Tetrakis(ethylmethylamido)hafnium
TEMAZr	:	Tetrakis(ethylmethylamido)zirconium
UID	:	Unintended Doping
VIS	:	Visible spectrum
εr	:	Relative permittivity

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Abstract

Study on High-k Gate Oxides of $In_{0.53}Ga_{0.47}As$ Photo-FET Fabricated by Wafer Bonding Technique on Si Substrate

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SWIR (Short-wave infrared) detectors are widely used in Si Photonics, medical devices, LiDAR sensors, and quantum computing. Especially, $In_{0.53}Ga_{0.47}As$ has been used to detect SWIR wavelengths due to lattice-matched InP wafer and high absorption coefficient. The PIN and APD structures are widely used in the $In_{0.53}Ga_{0.47}As$ photodetector. However, there are challenges in the detection of weak light since PIN does not provide any internal gain and APD suffers from the high operating voltage with a large excess noise [1]. To solve the aforementioned problems, Photo-FETs, which have middle internal gain and low operating voltage, have been researched. Recently, organic and 2D material-based Photo-FET structures have been widely studied, but these materials are unsuitable for the SWIR region due to low mobility [2].

Chapter 2 shows previous research and this paper objective. in the previous research, We have fabricated Photo-FET based on $In_{0.53}Ga_{0.47}As$ with wafer bonding technology and compared a P+Si

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gate with a metal gate(W/Au/W) structure for the optoelectrical characteristics of this device. As a result, We confirm that the metal gate is 2 times higher responsivity than the P+Si gate due to optical confinement in ranges of SWIR wavelength. To improve the responsivity of InGaAs Photo-FET, We have performed the Al_2O_3 gate oxide replaces high-k dielectric gate oxide(HfO_2/Al_2O_3, ZrO_2/Al_2O_3), which is a method commonly used to increase gate drivability in the CMOS technology roadmap. Additionally, the operating mechanism of the Photo FET is presented. The photo conducting and photo gating effects, which contribute to I_{ph} (Photocurrent), are presented.

Chapter 3 shows that the process flow for $In_{0.53}Ga_{0.47}As$ mos capacitor was first presented and the interface trap and slow trap were evaluated depending on PDA and PMA temperature conditions. This interface trap and slow trap were evaluated by the terman method and V_{start} fixed and V_{end} variated C-V measurement method, respectively.

Chapter 4 shows the optimization conditions of the wafer bonding process for high bonding yield and good quality epi, and then The overall process flow of InGaAs Photo FET is shown. This chapter also shows the measurement method such as confocal microscopy and optoelectrical evaluation of InGaAs Photo-FET with gate oxide of Al_2O_3, HfO_2/Al_2O_3, and ZrO_2/Al_2O_3. Also, the optoelectrical characteristics of this device depending on the channel lengths(10um, 50um) are presented.

Keywords: $In_{0.53}Ga_{0.47}As$, Phototransistor, Photo-FET, MOS capacitor, MOSFET, Monolithic 3D Integration, Wafer bonding, high-k dielectric.

1. Introduction

1.1 Various Applications of IR Sensors

In general, the IR(infrared) region is a wavelength of 0.7 um or more. IR detectors are widely used in Si Photonics, healthcare, surveillance, Face ID, and LiDAR sensors as shown in fig.1.1. However, since silicon, which is efficiently not able to absorb wavelengths above about 1000 nm due to its bandgap characteristics, is impossible to make an efficient SWIR detector with silicon CMOS(Complicate Metal Oxide Semiconductor) technology.

Otherwise, InGaAs material can not only control the band gap by adjusting the composition ratio of indium and gallium but also grow high-quality InGaAs thin films on InP wafer because of the lattice constant matching. Especially, in the case that the composition of indium and gallium is respectively 0.53 and 0.47, that is, the $In_{0.53}Ga_{0.47}As$ material has a high absorption coefficient in the IR region as shown in fig 1.2.

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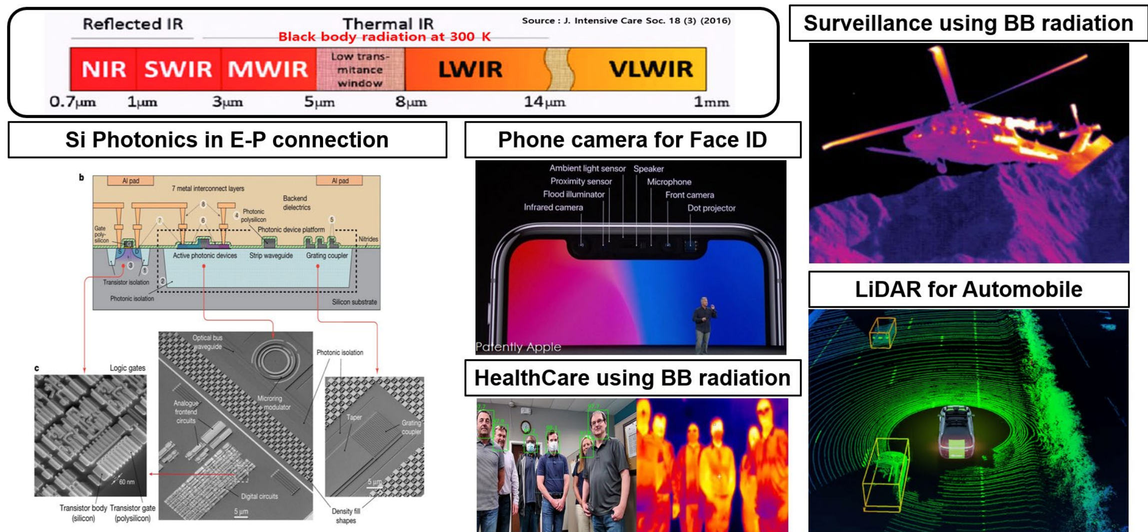

Fig.1.1 Applications of IR sensors: Si Photonics, Phones, Health Care, Surveillance, Automobiles

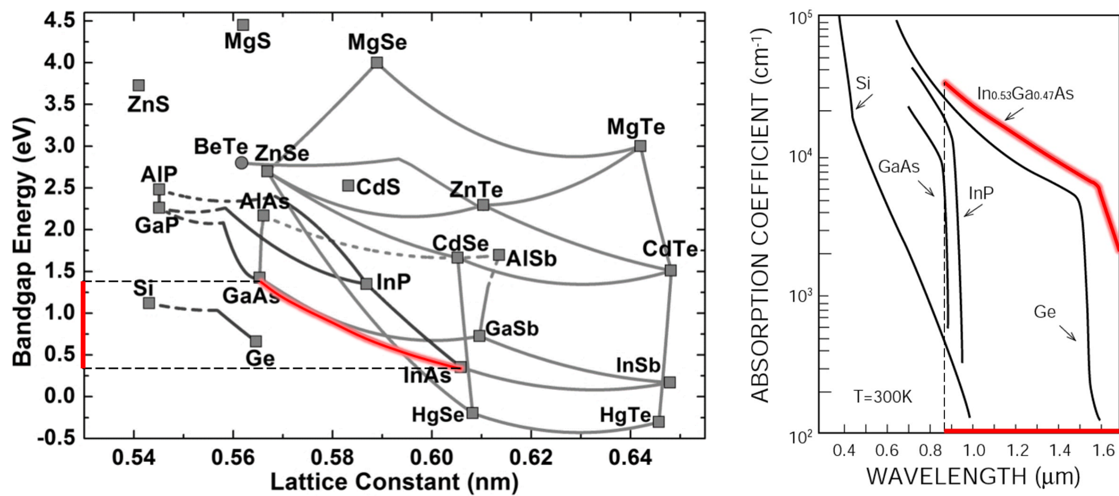

Fig 1.2. (a) Lattice Constant verse bang gap. Fig 2. (b) Absorption coefficient verse wavelength

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1.3 Heterogeneous Integration of $In_{0.53}Ga_{0.47}As$ SWIR Detector on Si Substrate

Figure 3(a) sequentially shows the cross-section of the interface between pixel and DRAM, the interface between DRAM and Logic after the hybrid bonding process. Wafer bonding technology, which is the basis of hybrid bonding, has the following advantages. In the case of electrical characteristics, the power consumption and RC delay can be reduced due to the reduction of metal lines In the BEOL process. Also, in the case of the process, wafers (Pixel, DRAM, Logic) are possible to design process flow with a suitable thermal budget for electrical characteristics[3].

Also, Wafer bonding technology is the key to integrating the CMOS technology process with III-V material, which has excellent optical performance. Figure 3 shows the hybrid bonding process flow of III-V material-based pixels and ROIC using the CMOS process. Based on this technology, Sony proposed a prototype of an image sensor that detects both VIS and SWIR wavelength ranges[4].

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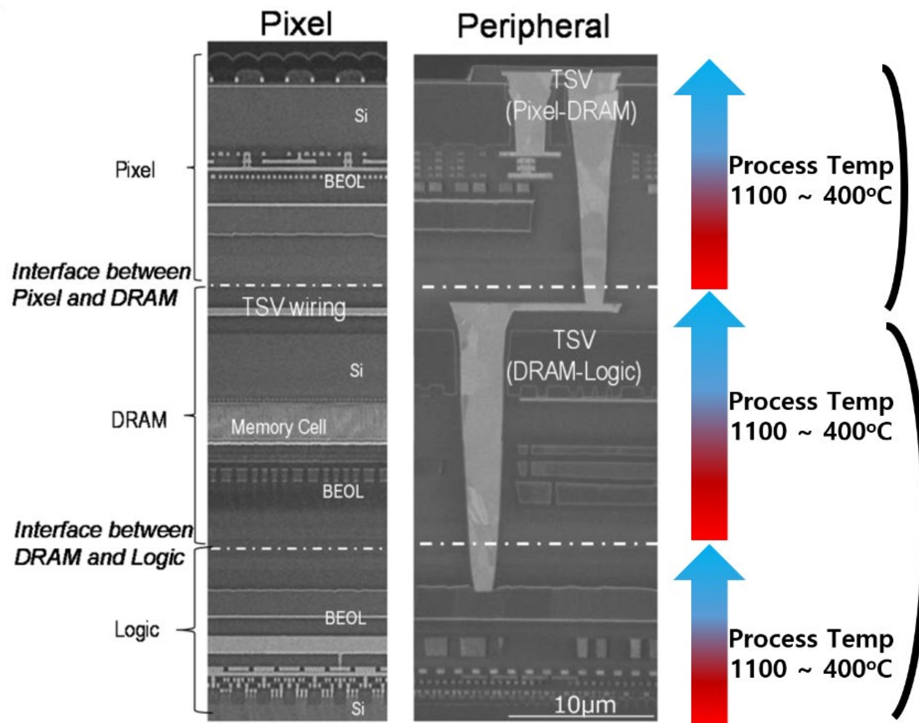

Fig. 1.3 (a) Pixel/DRAM/logic 3-layer stacked CMOS image sensor made by Sony[3]

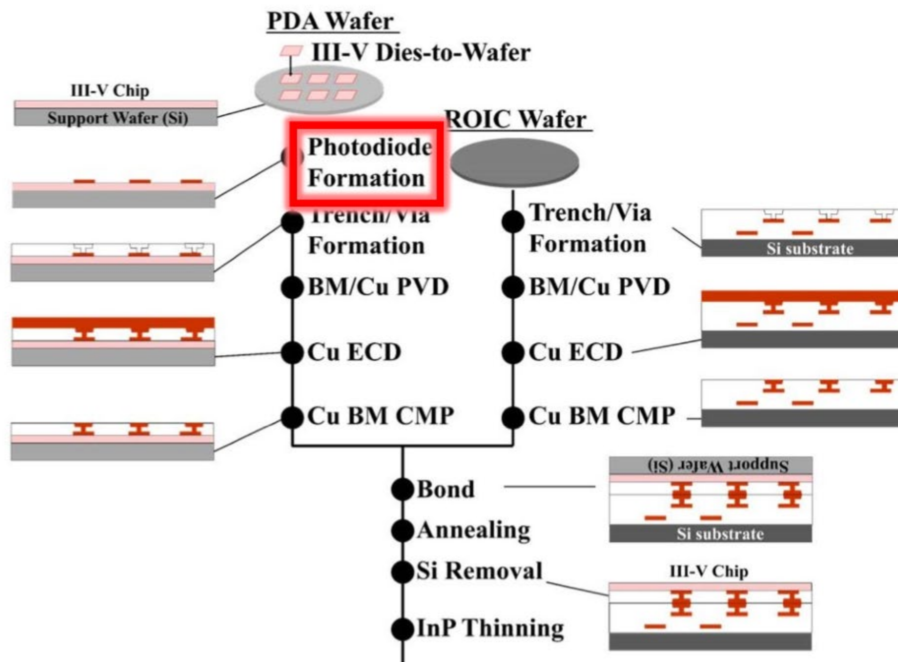

Fig.1.3 (b) High-definition Visible-SWIR InGaAs Image Sensor using Cu-Cu Bonding of III-V to Silicon Wafer[4]

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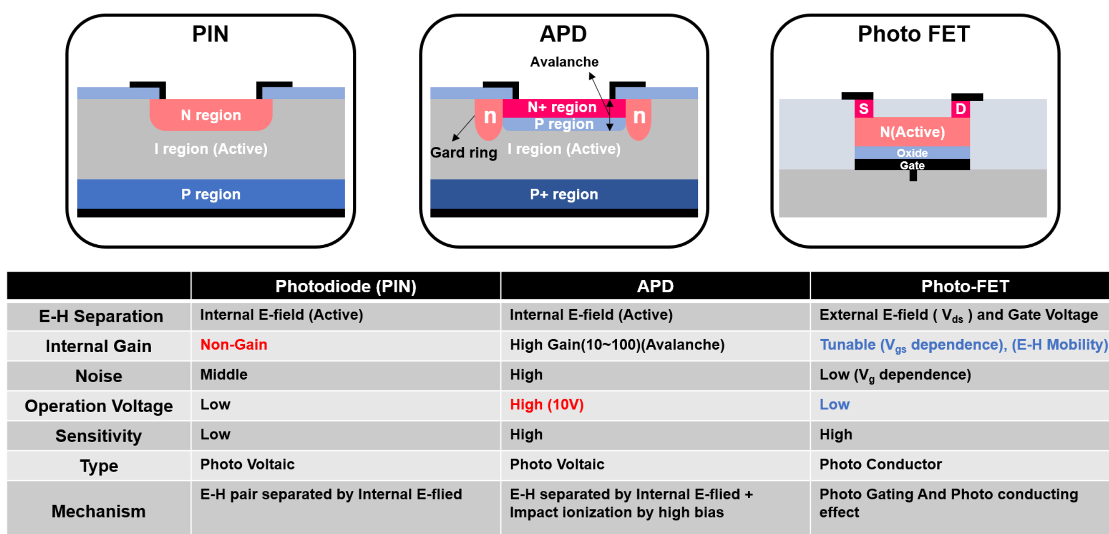
1.4 Various Structures of $In_{0.53}Ga_{0.47}As$ IR Detectors

The previously mentioned $In_{0.53}Ga_{0.47}As$ pixel is able to use photodetectors with various structures as shown in fig 1.4. In PIN and APD, the e-h pairs, which are generated by photon injection, are separated by an internal E-field. But, in the case of photo-FET, the generated e-h pairs are separated by an external e-filed.

The PIN structure has no internal gain so unsuitable that use in low light or special environments. On the other hand, APD and Photo-FET structures are able to be used in this situation(e.g low light, special environment) due to having an internal gain. However, the APD structure has greater operating voltage than photo-FET since the avalanche effect is required for amplification. On the other hand, since the gain of Photo-FET is based on the Photo conducting effect (Photoconductive effect), this structure consumes lower voltage than the APD structure. Therefore, Photo-FET is available for applications requiring low operating voltage in low-light environments[5][6].



	Photodiode (PIN)	APD	Photo-FET
E-H Separation	Internal E-field (Active)	Internal E-field (Active)	External E-field (V_{ds}) and Gate Voltage
Internal Gain	Non-Gain	High Gain(10~100)(Avalanche)	Tunable (V_{gs} dependence), (E-H Mobility)
Noise	Middle	High	Low (V_g dependence)
Operation Voltage	Low	High (10V)	Low
Sensitivity	Low	High	High
Type	Photo Voltaic	Photo Voltaic	Photo Conductor
Mechanism	E-H pair separated by Internal E-flied	E-H separated by Internal E-flied + Impact ionization by high bias	Photo Gating And Photo conducting effect

Fig. 1.4 Various Structures of $In_{0.53}Ga_{0.47}As$ IR Detectors

1.5 Another Application: Si Photonics in Power Monitor

As mentioned previously, Figure 1.5 (a) shows that the InGaAs Photo-FET is advantageous in low-light environments since it has higher responsivity than other APDs and photodiodes. Also, the process of InGaAs Photo-FET CMOS- compatibility. The process of InGaAs Photo-FET is able to be fabricated in low temperatures conditions since it is not using an ion implantation process. Thus, The CMOS compatibility is excellent[7].

Additionally, Figure 1.5 (b) shows that InGaAs Photo-FETs can is able to be used as optical power monitors in Si photonics circuits due to not only their excellent responsivity(10^{-6}A/W) but also their fast response time(10^{-6} s)[8].

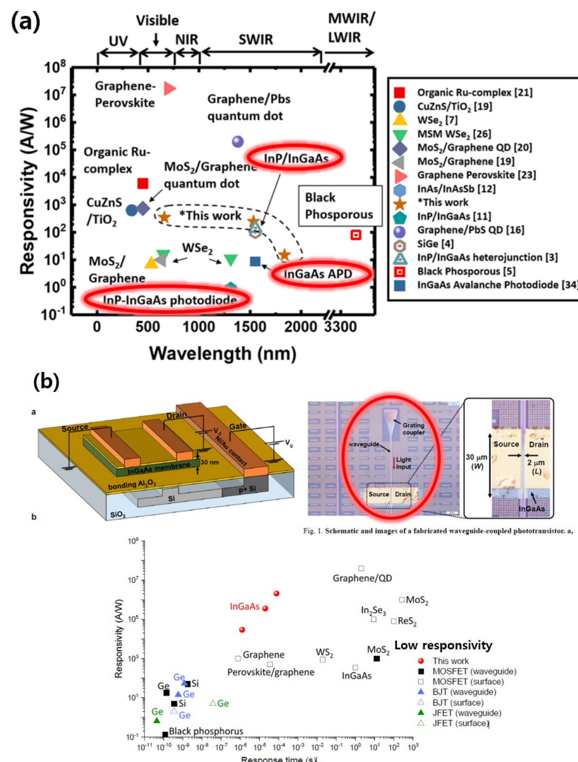


Fig 1.5 (a) the responsivity depending on InGaAs APD, Photodiode, Photo-FET structure (b) Top: optical power monitor using InGaAs Photo-FET. Bottom: the responsivity and response time of comparison among devices (MOSFET, BJT, JFET) with various materials.

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2. $In_{0.53}Ga_{0.47}As$ Photo-FET with High-k Gate Oxide

2.1 Photo-FET Operation Mechanism

The phoo FET is based on a mechanism called the photo-gating effect and photoconductive effect.

First, in the case of the photoconductive effect., An absorbed photon photogenerated an e-p pair, which drift in opposite directions as shown in Fig.2.1 (a). The electron drifts much faster than the hole and therefore leaves from the channel region to drain quickly. The channel, however, must be neutral which means another electron must enter the channel from the source. This new electron also drifts across quickly as in the channel region and leaves the channel while the hole is still drifting slowly in the channel. Thus, another electron must enter the channel to maintain neutrality, until either the hole reaches the drain or recombines with one of these electrons entering the channel[5][6].

Second, in the case of the photo gating effect The holes, which are generated by the photons, are trapped in gate oxide at the interface trap site or border trap sites and therefore shift in the V_{th} to a negative direction. As a result, photosensitivity is increased at a flat voltage region. Also, the channel must be in a neutral condition which is supplied free electrons from the source due to the hole being trapped at gate oxide[6].

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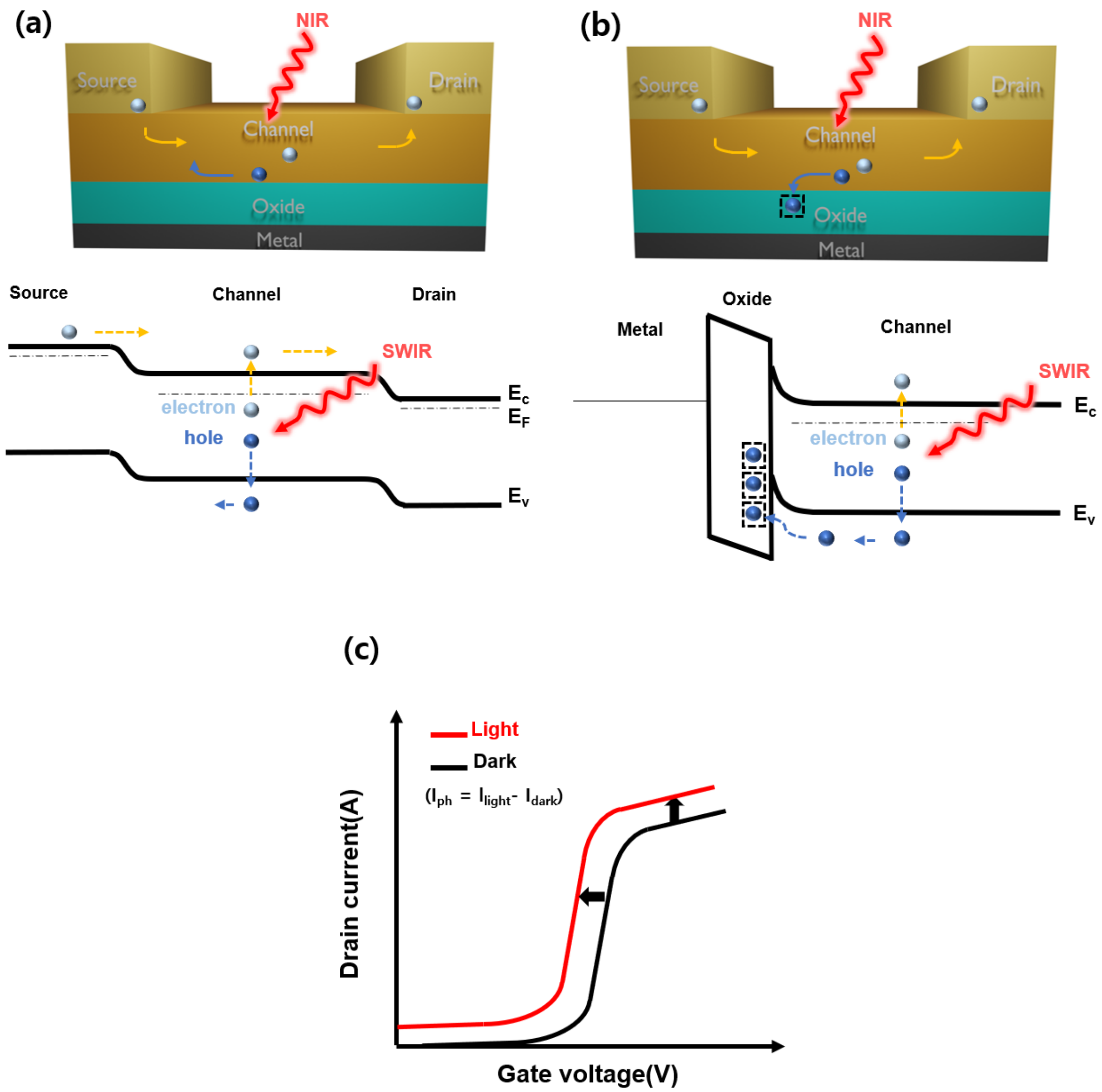

Fig.2.1 (a) Photo Conducting Effect and Source/Channel/ Drain band diagram (b) Photo Gating Effect and Gate/Oxide/channel band diagram (c) I-V Characteristics of Photo FET in light on/off-state

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2.2 Previous Research: Cavity Effect for High-Performance Photo-FET with Thin Channel

In the accumulation type MOSFET, the I_{off} current is able to be reduced by reducing the thickness of the channel. However, the thickness of the channel reduction not only reduces the I_{off} current but also the light absorption. As a result this light absorption reduction leads to reducing the photocurrent as shown in fig 2.2[6].

In a previous study, the light absorption rate was increased in a thin InGaAs channel in the SWIR range by using a reflective cavity. Fig. 2.3 (a) shows Photo FET of W(10nm)/Au(120nm)/W(10nm) and P+si gate. Metal gate and P+Si photo FET were respectively fabricated using wafer bonding technology on the interface of Au and Al_2O_3. Fig. 2.3 (b) shows the reflectance simulation in the SWIR region. P+Si gate photo-FET indicates the same reflectance rate at all of the ranges. But, Metal gate photo-FET has strong optical absorption from 1100nm to 1600nm wavelength.

Fig. 2.3 (c) shows the responsivity vers power density compared to the metal gate and P+si gate. Metal gate Photo-FET structure has higher responsivity than P+Si gate at all of the range. Additionally, the metal gate shows about twice the absorption rate than P+Si at $3mW/cm^2$[9]

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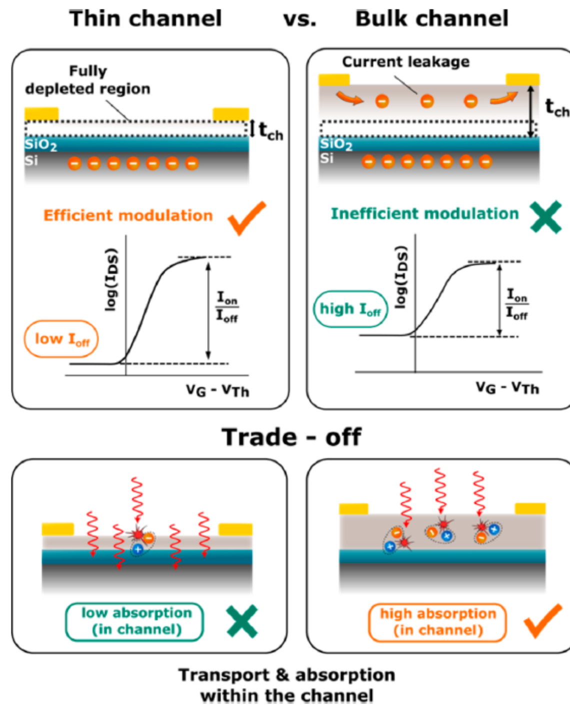

Fig.2.2 Thin channel and bulk channel of Photo FET, In the case of a thin channel, the range of a few nanometers thickness allows efficient field-effect modulation leading to high on/off ratios[6].

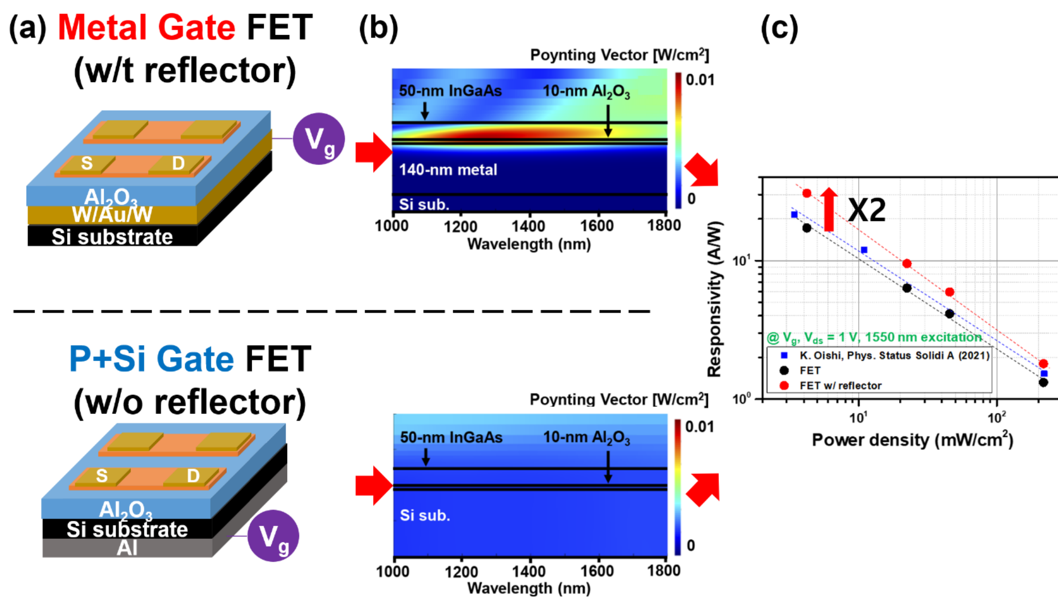

Fig.2.3 (a) W/Au/W gate Photo-FET structure (up) and P+Si gate Photo-FET structure(down) (b) Simulated Poynting vectors of wafer-bonded InGaAs photo-FETs with metal gate reflector(up) and without metal gate reflector(down) (c) Responsivity characteristics of InGaAs photo-FETs with and without metal gate reflector in 1550 nm wavelength[9].

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2.3 Objective: $In_{0.53}Ga_{0.47}As$ Photo-FET with High-k Gate Oxide

Figure 2.4 (a) shows the CMOS technology roadmap, The oxide thickness gradually decreased with the scaling of MOSFETs. This reduction not only increased the gate controllability but also the gate leakage current. This leakage component leads to the degradation of the device and the power consumption increase.

To solve these trade-off phenomena, the gate oxide material has been introduced with a high-k dielectric to reduce power consumption, i.e., this method has reduced the leakage current as well as increased the gate controllability[10].

In this paper, our objective introduces InGaAs Photo FET to high-k dielectric gate oxides such as HfO_2/Al_2O_3, and ZrO_2/Al_2O_3 to enhance device performance. Figure 2.5 (b) shows a cross-section of InGaAs Photo FET with Al_2O_3 gate oxide and high-k gate oxide(HfO_2/Al_2O_3, ZrO_2/Al_2O_3) at the same thickness.

We have compared the electrical and optical characteristics of the existing Al_2O_3 gate oxide InGaAs Photo FET and the high-k dielectric(HfO_2/Al_2O_3, ZrO_2/Al_2O_3) InGaAs Photo FET. Details are presented in chapters 3 and 4.

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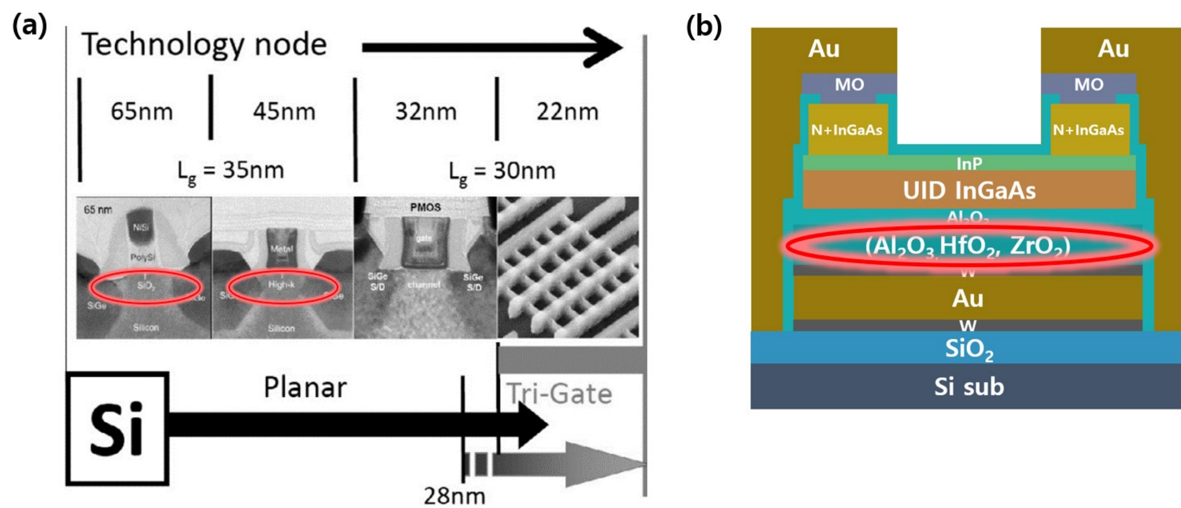

Fig.2.4 (a) CMOS technology road map, in which the red circle indicates gate oxide change from SiO2 at 65nm to high-k dielectric at 45nm[10], (b) Cross section of InGaAs Photo FET using high-k dielectric

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3. W/high-K/Al_2O_3/InGaAs MOS Interface Optimization

3.1 Au/W/Al_2O_3/InGaAs MOS Capacitor Fabrication for PDA and PMA influence

We fabricated the MOS capacitor on Si-doped $In_{0.53}Ga_{0.47}As$ (N_D ~ $5x10^{15}$ cm^{-3}) grown on (100) n+InP with the donor concentration (N_D ~ $3.4x10^{18}$ cm^{-3}).

the $In_{0.53}Ga_{0.47}As$ surface was cleaned with acetone, methanol, and deionized wafer step by step. The native oxide was removed with NH_3OH solution (NH_3OH : DI = 1 : 5) for 1min. The sulfur pre-treatment was performed by dipping in an $(NH_4)S_x$ solution for 5min.

Al_2O_3(10nm) gate oxide film was grown by using ALD(atomic layer deposition) alternating pulses of TMA (Tri-methyl aluminum) and H_2O precursors at 300◦C substrate. In the case of HfO_2 or ZrO_2 Gate oxide, an Al_2O_3(1nm)/HfO_2(9nm) or Al_2O_3(1nm)/ZrO_2(9nm) gate oxide film was grown by using ALD(atomic layer deposition)alternating pulses of TEMAHf(Tetrakis ethyl methyl amino hafnium) or TEMAZr(Tetrakis ethyl methyl amino zirconium) and H_2O precursors at 300◦C substrate. Figures 9 and 10 show the process flow and device structure for the InGaAs MOS interface influence depending on PDA and PMA.

`

In the case of the PDA capacitor, the Post deposition annealing (PDA) process is respectively performed in N_2 gas at 250, 300, 350, and 400°C for 10min. and then, W/Au(10/120nm) was deposited with DC sputter. Au and W etching was performed with aqua regia and ICP-RIE for gate patterning, which Aqua regia was used after 30 minutes of making it, and W dry etching was performed in CHF_3 20sccm and O_2 2sccm at ICP 400W, CCP 50W condition. Finally, the PMA process is performed in N_2 gas at 250°C for 1min to improve adhesion enhancement between W and oxide as shown in fig. 3.1 (a)

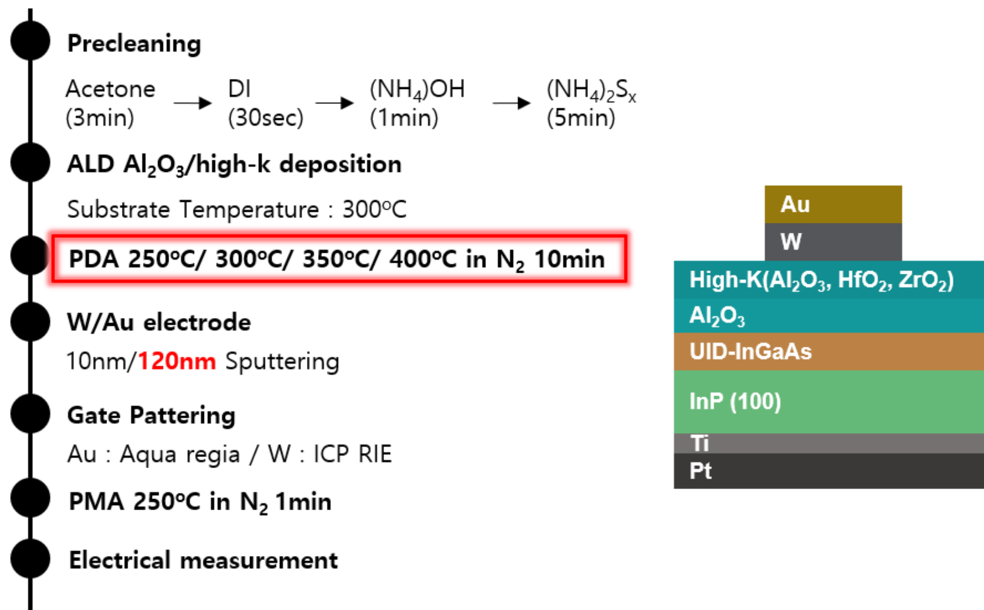

Fig.3.1 (a) W/high-k/Al2O3/$In_{0.53}Ga_{0.47}As$ Capacitor process flow and structure for PDA

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In the case of the PMA capacitor, Also, W/Au(10/60nm) was deposited with DC sputter. Au and W etching was performed with aqua regia and ICP-RIE for gate patterning, which Aqua regia was used after 30 minutes of making it, and W dry etching was performed in CHF_3 20sccm and O_2 2sccm at ICP 400W, CCP 50W condition as shown in fig.3.1 (b)

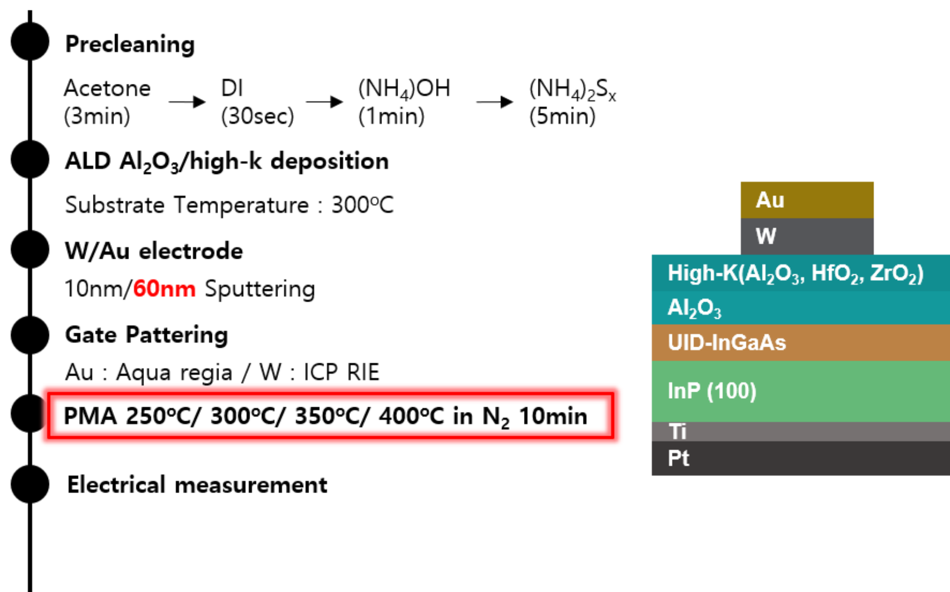

Fig.3.1 (b) W/high-k/Al2O3/$In_{0.53}Ga_{0.47}As$ Capacitor process flow and structure for PMA

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3.2 InGaAs MOS Capacitor C-V Measurement

3.2.1 C-V curve of Au/W/high-k/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS Capacitor with PDA proecss

C-V measurement was performed in a range from -1V to 1V with the double sweep of the 30mV oscillation, which is range from 1MHz to 1kHz. the solid line is the gate voltage sweep from negative to positive, and the dashed line is the gate voltage sweep from positive to negative.

Figure 3.2 shows the Al_2O_3 of gate oxide depending on PDA temperature, the C-V curve gradually shifts in the negative direction depending on the PDA temperature increases. the hysteresis, which is the difference between gate voltage sweep forward and reverses at 1MHz frequency, was greatly unaffected as shown in Fig 3.2.

Figure 3.3 shows the HfO_2/Al_2O_3 of gate oxide depending on PDA temperature, and figures 3.3 (a), (b) and (c) show gradual decreases of hysteresis depending on the increases of PDA temperature in the range from 250°C to 350°C. but figure 3.3 (d) shows that hysteresis no longer decreases at PDA at 400°C. Additionally, the slope of C-V decreases at 400°C PMA temperature. and then the C-V curve also shifts with a negative bias

Figure 3.4 shows the ZrO_2/Al_2O_3 of gate oxide depending on PDA temperature, figure 3.4 shows decreases of hysteresis depending on the increases of PDA temperature in all of the ranges. and then, the C-V slope and Cox was significantly increased above PDA 300°C

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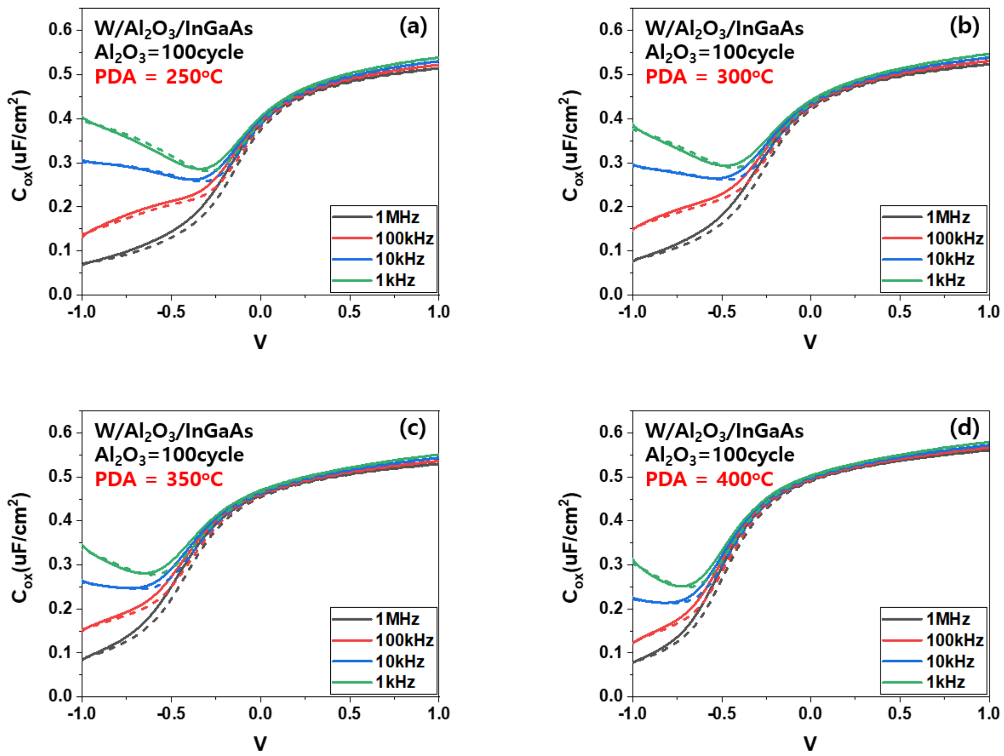

Fig. 3.2 C-V measurement of W/Al_2O_3/$In_{0.53}Ga_{0.47}As$ Capacitor with PDA 10min at (a) 250ºC, (b) 300ºC, (c) 350ºC, and (d) 400ºC. and then, PMA was performed at 250ºC.

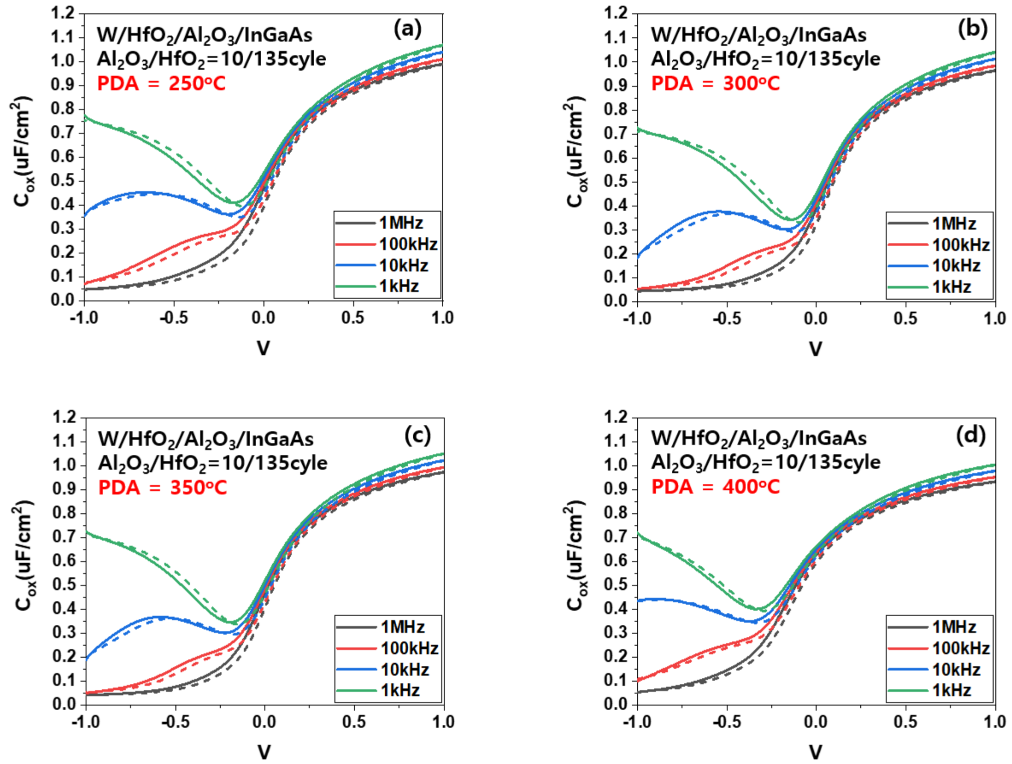

Fig. 3.3 C-V measurement of W/HfO_2/Al_2O_3/$In_{0.53}Ga_{0.47}As$ Capacitor with PDA 10min at (a) 250ºC, (b) 300ºC, (c) 350ºC, and (d) 400ºC. and then, PMA was performed at 250ºC.

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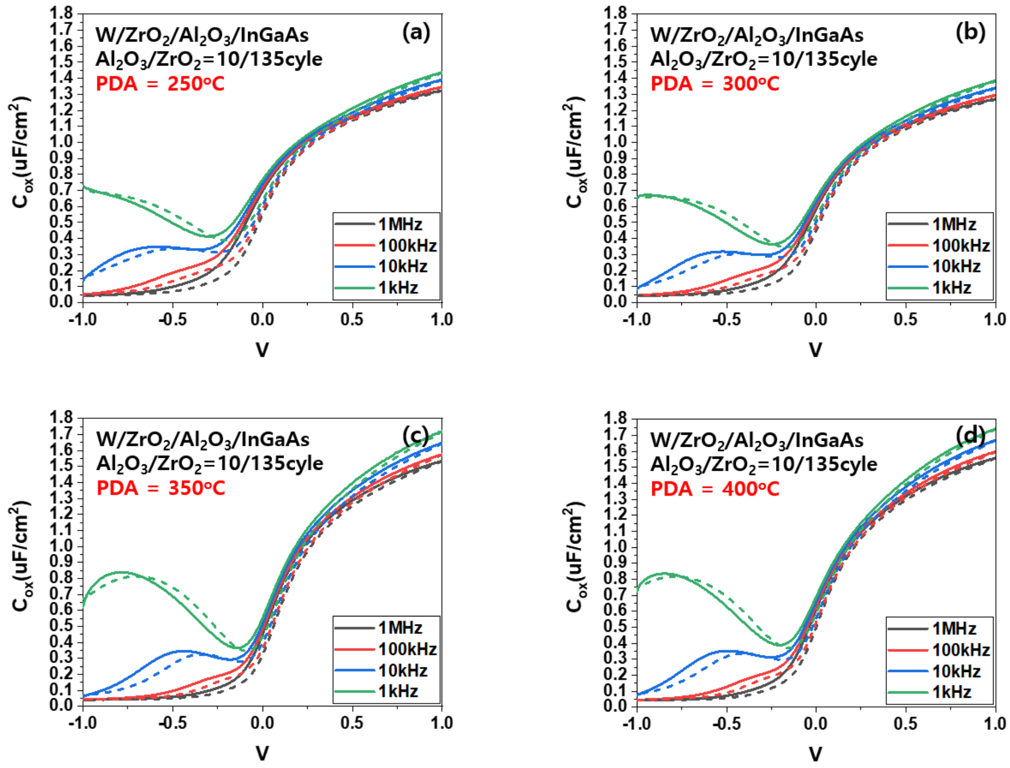

Fig. 3.4 C-V measurement of $W/ZrO_2/Al_2O_3/In_{0.53}Ga_{0.47}As$ Capacitor with PDA 10min at (a) 250ºC, (b) 300ºC, (c) 350ºC, and (d) 400ºC. and then, PMA was performed at 250ºC.

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3.2.2 C-V curve of Au/W/high-k/Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOS Capacitor with PMA proecss

C-V measurement was performed with the double sweep of the 30mV oscillation, which is range from 1MHz to 1kHz. the solid line is the gate voltage sweep from negative to positive, and the dashed line is the gate voltage sweep from positive to negative.

Figure 3.5 shows the Al_2O_3 of gate oxide depending on PMA temperature. figure 3.5 (a),(b) and (c) shows hysteresis was slightly decreased from 250°C to 350°C depending on the increase of PMA temperature. but figure 3.5 (d) shows hysteresis slightly increases at PMA 400°C temperature. Additionally, the C-V curve slightly shifts to a positive bias in the range from 250°C to 350°C, but shifts to a negative bias at PMA 400°C

Figure 3.6 shows the HfO_2/Al_2O_3 of gate oxide depending on PMA temperature. this show that the hysteresis is unaffected, but the C-V curve shifts to positive bias depending on the increase of PMA.

Figure 3.7 shows the ZrO_2/Al_2O_3 of gate oxide depending on PMA temperature. hysteresis is gradually decreased, and the C-V curve gradually shifts to a positive bias depending on the increase of PMA temperature. especially, Cox was drastically increased between 250°C and 300°C PMA temperature

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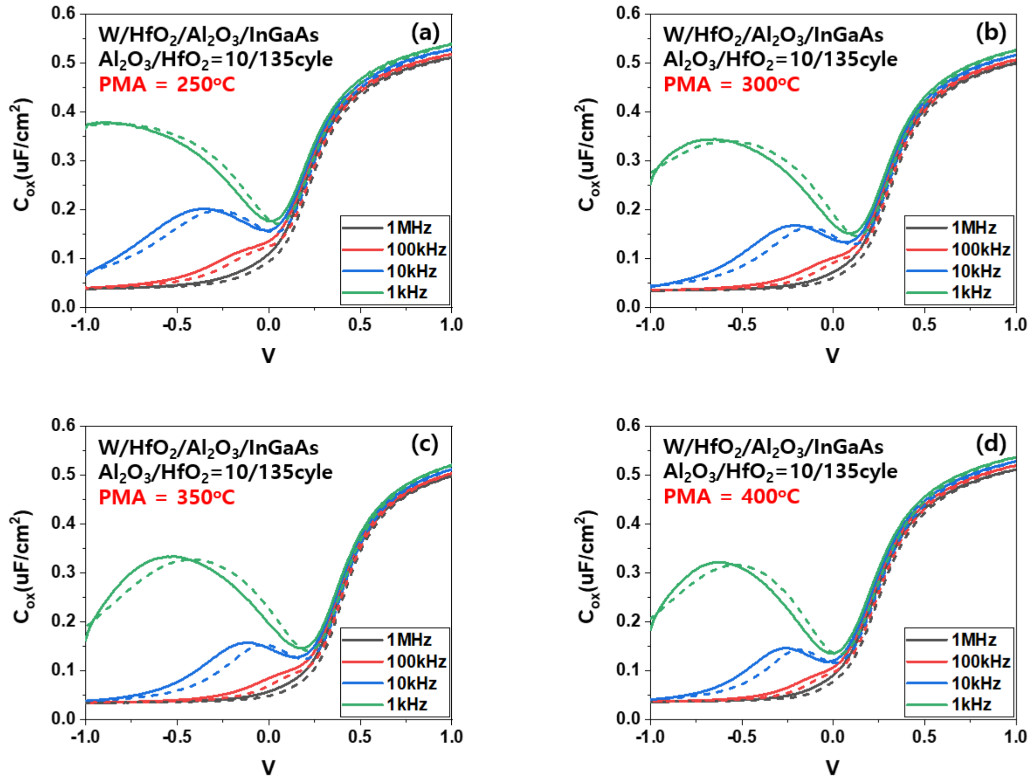

Fig. 3.5 C-V measurement of W/Al_2O_3/$In_{0.53}Ga_{0.47}As$ Capacitor with PMA 10min at (a) 250ºC, (b) 300ºC, (c) 350ºC, and (d) 400ºC.

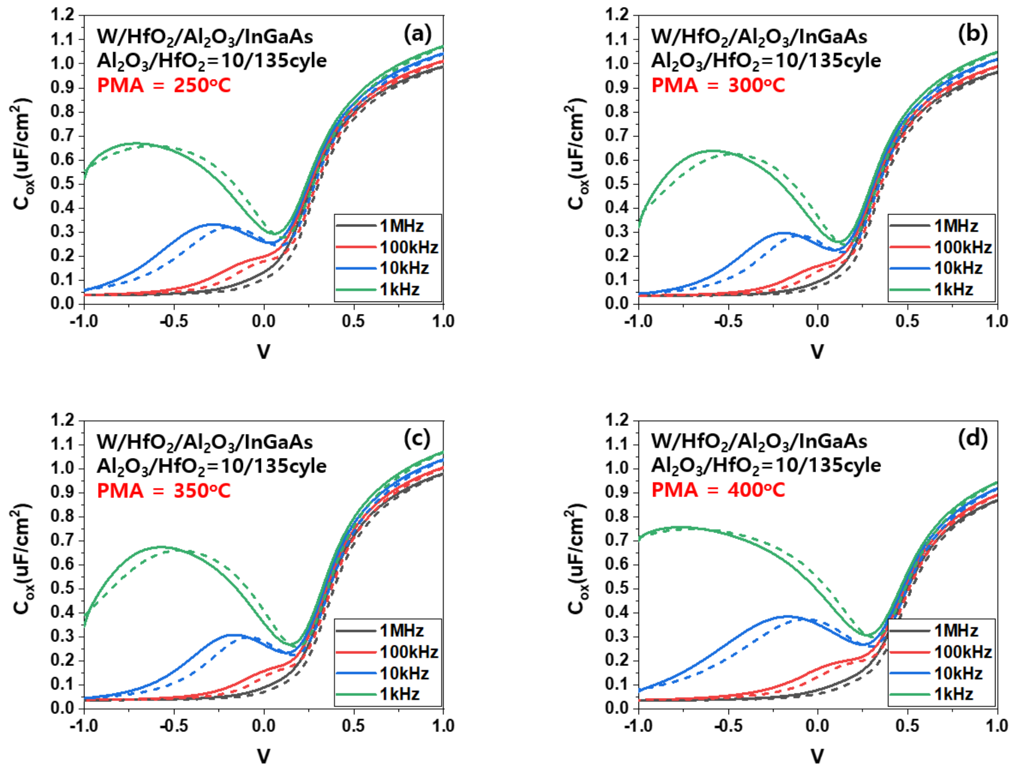

Fig. 3.6 C-V measurement of W/HfO_2/Al_2O_3/$In_{0.53}Ga_{0.47}As$ Capacitor with PMA 10min at (a) 250ºC, (b) 300ºC, (c) 350ºC, and (d) 400ºC.

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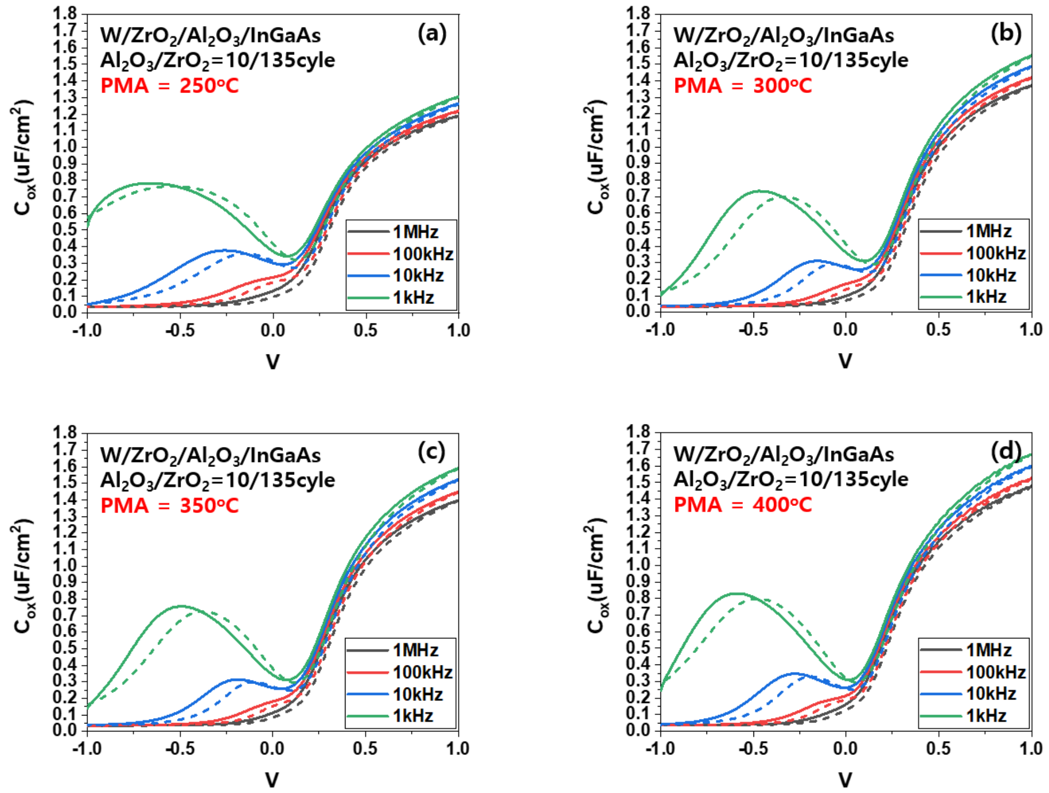

Fig. 3.7 C-V measurement of W/HfO_2/Al_2O_3/$In_{0.53}Ga_{0.47}As$ Capacitor with PMA 10min at (a) 250°C, (b) 300°C, (c) 350°C, and (d) 400°C.

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3.3 Dependence of PDA and PMA Temperature on Interface Trap Density Evaluation by Terman Method

The density of the interface trap and slow trap is an important factor to quantitatively estimate the quality of the MOS interface and gate oxide.

the interface trap is formed by dangling bonds at gate oxide/semiconductor, metal impurity, and defect, etc as shown in fig 3.9 (a). This density contributes to performance degradation of MOSFET such as subthreshold swing and on/off ratio, noise, etc.

Slow trap charges are also formed for the same reasons as the interface trap and are mainly located above the interface, which this is deeper than the interface trap site as shown in fig 3.9 (a). These traps greatly affect the gate oxide reliability due to their influence on time-dependent characteristics.

Therefore, interface trap density and slow trap density must be preferentially evaluated before fabricating the MOSFET device.

the InGaAs MOS interface trap density is measured by the high-frequency method because this method is one of the fast measurement methods. This method is generally useful for measuring interface trap densities of 10^{10} cm^{-2} eV^{-1} and above. For Al_2O_3/InGaAs interface, The hf method is sufficient to measure the D_{it} evaluation because this interface trap density is reported to be over 10^{10} cm^{-2} eV^{-1} in most research groups[12][13][14][15].

`

Although D_{it} does not respond to high frequencies, it responds to variations of DC voltage. Therefore, an additional charge of the gate induces an additional semiconductor charge $Q_G = (Q_b + Q_n + Q_{it})$ for MOS capacitor of depleted or inverted state. for a given surface potential ϕ_s, V_G variation leads to the C–V "stretch-out" when interface traps are present in fig 3.9 (b). This phenomenon causes a difference between ideal C-V and experimental C-V. Therefore, the interface trap charge can be obtained through the following equation since V_G difference indicates an interface trap.

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{dV_G}{d\phi_s} - 1\right) - \frac{C_S}{q^2} = \frac{C_{ox}}{q^2}\frac{d\Delta V_G}{d\phi_s}$$

where V_G = V_G(experimental)–V_G(ideal) is the variation of the experimental from the ideal curve. detailed equations are shown in Figure 3.9(b)[11][12].

Additionally, the reliability of the gate oxide has a great influence on the operation of the MOSFET device. If the MOSFET device has low gate oxide reliability, it can lead to variations in drain current and threshold voltage. For MOSFET reliability, the time dependence of oxide must be evaluated. Time-dependent traps are called slow trap density. This is evaluated by integrating the hysteresis difference of capacitance-voltage (C-V). Detailed equations and explanations are shown in Figure 3.9 (c). Also, the measurement method is presented in chapter 3.4[17][18].

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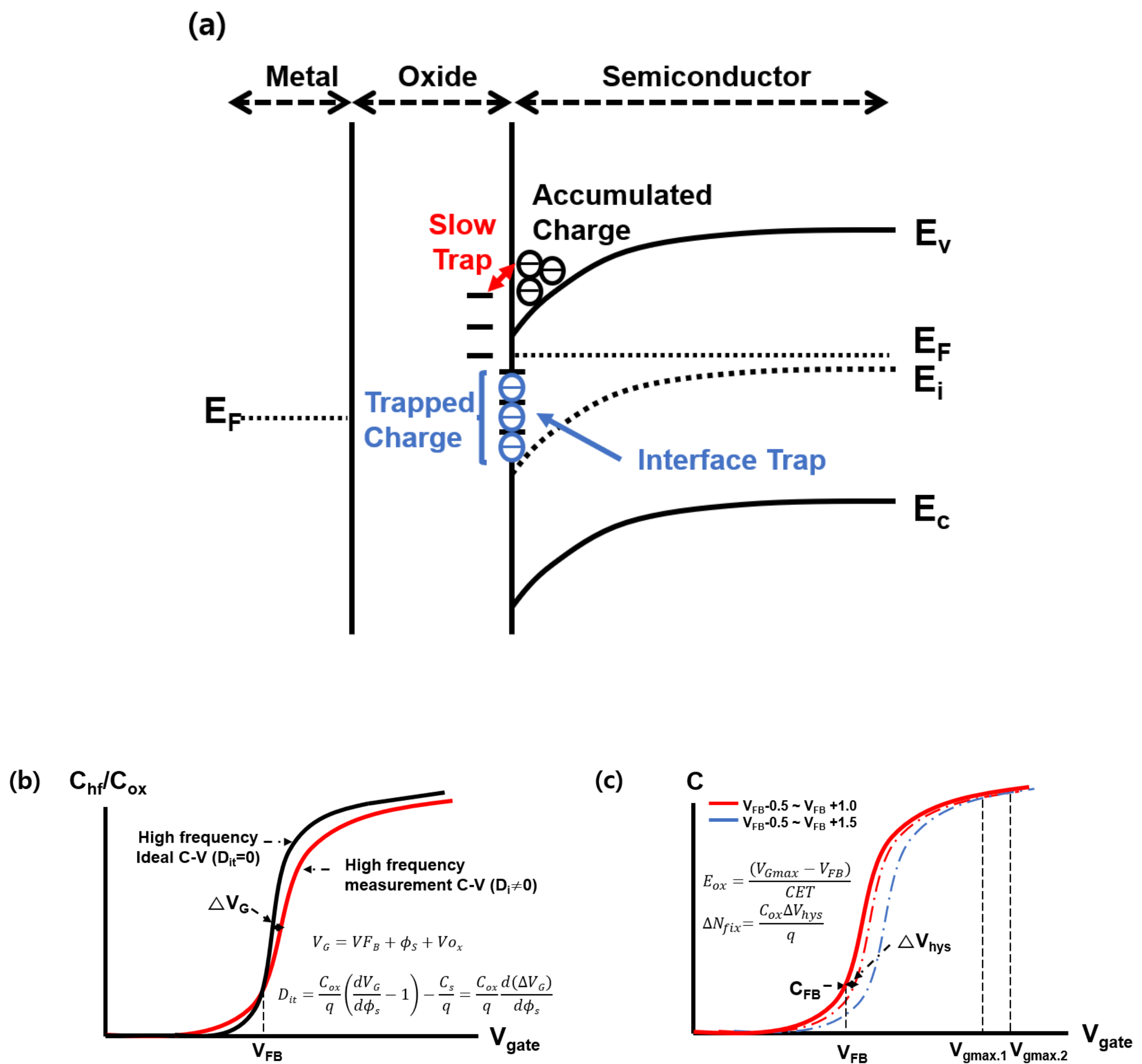

Fig 3.9 (a) interfacer trap charge and slow trap charge (b) evaluation method of interface trap charge using high frequency (terman method) (c) evaluation method of slow trap density

Figure 3.10 (a) and (b) show that D_{it} is decreased in all PMA devices as the PMA temperature is increased from 250°C to 300°C. On the other hand, the capacitor above 300°C PMA shows different characteristics. For the PMA MOS capacitor of Al_2O_3 and ZrO_2/Al_2O_3, The higher the PMA temperature, the slightly lower or no change in the interface trap charge. For the PMA MOS capacitor of HfO_2/Al_2O_3 gate oxide, the D_{it} is increased as the PMA temperature gradually increases as shown in figures (b),(c), and (d). On the other hand, for the PDA MOS capacitor, Dit is seriously unaffected by the increase of PDA temperature as shown in fig 10. Figure 3.11 shows the tendency of Dit depending on PMA and PDA temperature at 0.10eV from midgap

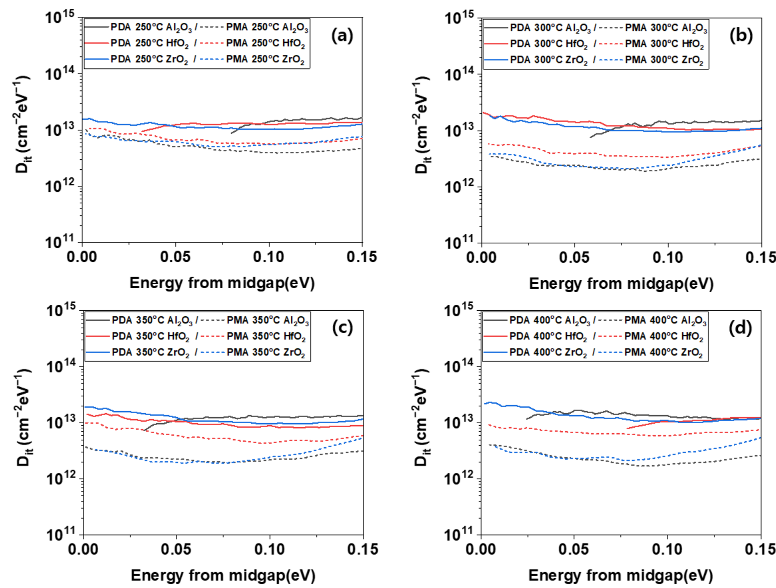

Fig. 3.10 interfacer trap density of Al_2O_3, HfO_2/Al_2O_3, Al_2O_3/ZrO_2 with PDA and PMA process at (a) 250 °C, (b) 300 °C, (c) 350 °C, and (c) 400°C

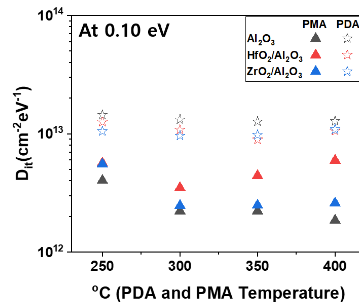

Fig. 3.11 interfacer trap density of Al_2O_3, HfO_2/Al_2O_3, Al_2O_3/ZrO_2 with PDA and PMA process at (a) 250 °C, (b) 300 °C, (c) 350 °C, and (c) 400°C

`

3.4 Dependence of PDA and PMA Temperature on Effective Slow Trap Density Evaluation by V_{start} fixed and V_{end} variated C-V Measurement

The slow trap was estimated by hysteresis in C-V, we first find out flat band voltage for PMA and PDA capacitors depending on gate oxide(Al_2O_3, HfO_2/Al_2O_3, ZrO_2/Al_2O_3) as shown in fig 3.8. Then, we fixed the start voltage(V_{start}) at V_{start} = V_{FB} - 0.5 V, and the end voltage (V_{end}) sweep the various bias, which is the end voltage (V_{end}) = V_{FB} + 1.0 V, 1.5V, 2.0V as shown in fig 3.9 (c) [11][17][18].

the slow trap density was estimated to be calculated the hysteresis of Vend varying C-V at different electric fields. The CET normalized effective electric field (E_{ox}) is defined as

$$E_{ox} = \frac{V_{end} - V_{FB}}{CET}$$

The slow trap density was calculatedd by the following equation

$$\Delta N_{fix} = \frac{V_{\mathrm{hys}} \cdot C_{ox}}{q}, \ V_{hys} = V_{FB.Fowerd} - V_{FB,Reverse}$$

,Where $V_{FB, Forward}$ and $V_{FB, Reverse}$ is V_{FB} of forward sweep and of reverse sweep.respectively. C_{ox} is Capacitance oxide Semiconductor,which is defined for max capacitance at V_{FB} + 1.0 V, Fig 3.13 (a) and (b) show that the slow trap density of W/high-k /InGaAs is compared depending on PDA and PMA temperature, which higk-k is Al_2O_3, HfO_2/Al_2O_3, and ZrO_2/Al_2O_3.

The slow trap density of all capacitors with the PDA process is decreased depending on the increase of PDA temperature. the PMA temperature has no effect on slow trap density, barely. Especially, the slow trap density of Al_2O_3 gate oxide with PMA is about 10 times lower than PDA conditions.

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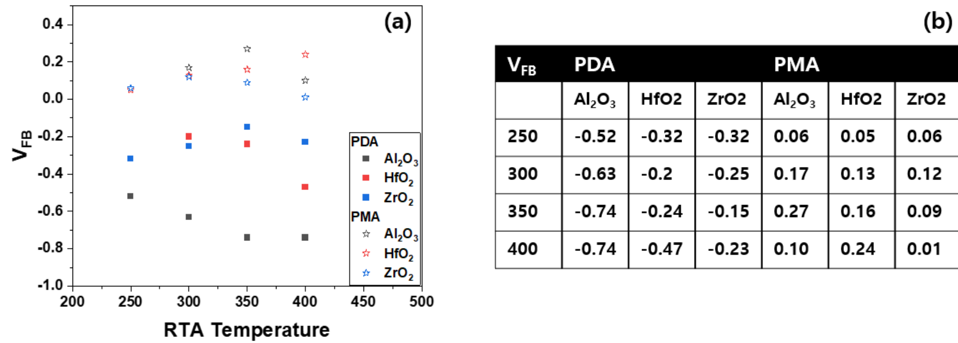
Figure 3.14 shows the slow trap density of 400ºC PDA and PMA under the same voltage sweep condition. both 400ºC PDA and PMA are the highest slow trap density in ZrO_2/Al_2O_3 gate oxide since the electric field dropped on the gate oxide is larger ZrO_2/Al_2O_3 than other gate oxides (HfO_2/Al_2O_3, Al_2O_3).



V_{FB}	PDA			PMA		
	Al_2O_3	HfO2	ZrO2	Al_2O_3	HfO2	ZrO2
250	-0.52	-0.32	-0.32	0.06	0.05	0.06
300	-0.63	-0.2	-0.25	0.17	0.13	0.12
350	-0.74	-0.24	-0.15	0.27	0.16	0.09
400	-0.74	-0.47	-0.23	0.10	0.24	0.01

Fig. 3.12 (a) V_{FB} of Al_2O_3, HfO_2/Al_2O_3, and ZrO_2/Al_2O_3 gate oxide based on C_{FB} calculation and (b) quantitative V_{FB} value depending on PDA and PMA process condition

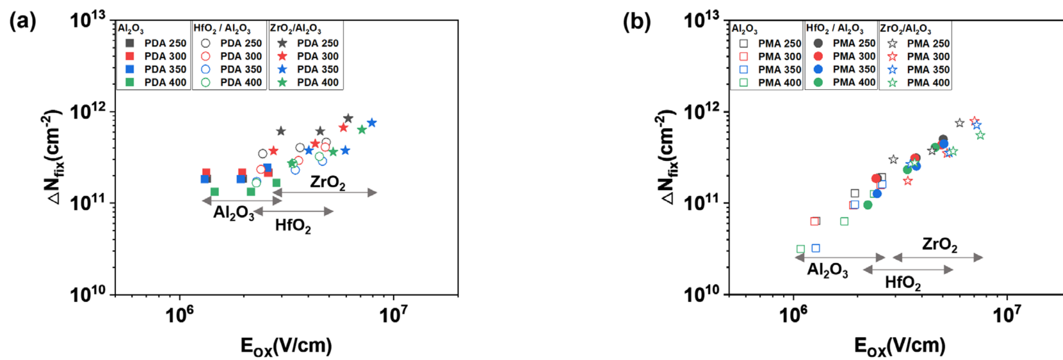


Fig.3.13 Slow trap density of W/high-k /InGaAs comparison depending on (a) PDA and (b) PMA temperature, which higk-k is Al_2O_3, HfO_2/Al_2O_3, and ZrO_2/Al_2O_3

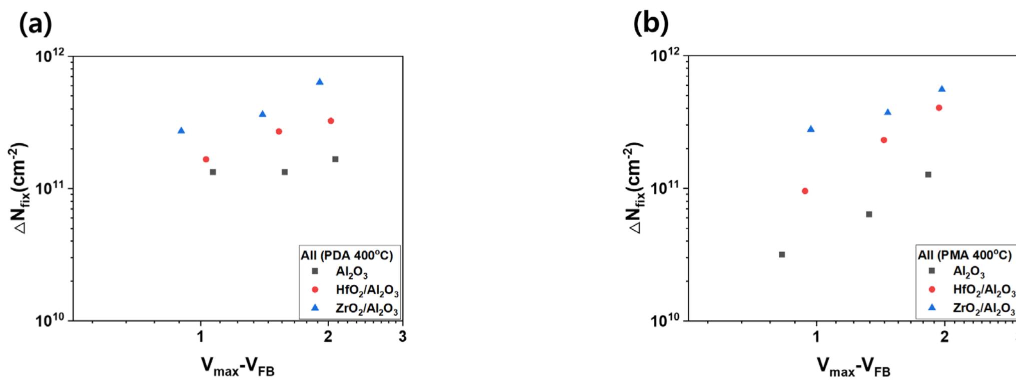


Fig.3.14 (a) Slow trap density of W/high-k /InGaAs comparison at Same voltage depending PDA and PMA at 400ºC

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4. Fabrication of $In_{0.53}$Ga As Photo-FET on Si wafer with High-k Gate Oxides and Electrical and Optical Analysis

4.1 Wafer Bonding Optimization for InGaAs Photo-FET

For high-yield InGaAs/InP/N+InGaAs epi on a Si wafer, optimization of the bonding process before, during, and after preferentially must be performed. The details of the process optimization are as follows:

First, before the bonding process, the optimization of the ALD process for the characteristics of the MOS device and the roughness investigation of the bonding interface[19].

Second, during the bonding process, the optimization of the PDA process removes gas, which is exhausted from gate oxide[20][21].

Third, slow rising and failing annealing process to reduce low-quality epi layer as the difference of thermal expansion coefficient between Si wafer and InP wafer in the bonding process.[22][23].

Fourth, after bonding, optimization of the back etching process to remove the InP substrate.

The optimization process for the four is described in detail in chapters 4.1.1 to 4.1.3

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4.1.1 ALD Process Optimization

ALD (Atomic Layer Deposition) is a so important process for fabricating high-performance MOS devices as it has been used to deposit gate oxide layer. Therefore, the work of understanding and optimizing the ALD process should be preceded.

Figure 4.1 (a) shows the four-step sequence of the ALD process. In Step.1, the precursors(TMA, TEMAHf, TEMAZr) are exposed from the chemical source. and then, this results in self-limiting adsorption onto the wafer. In step.2, the unreacted and weakly adsorbed precursors are removed by Ar purge. . In step.3, the H_2O espoused from the canister is adsorped on the surface and reacted with precursors. this reaction makes thin films such as Al_2O_3, HfO_2, ZrO_2. In step.4, the unreacted and weakly adsorbed H_2O are removed by Ar purge. Figure 4.1 (b) shows the adsorption amount depending on the pulse and purge time of precursor and H_2O. the precursors and H_2O are not sufficiently adsorbed on the surface when the pulse time is shorter saturation time. As a result, a thin film is deposited at a thinner thickness than expected. the unexhausted precursors and H_2O in the chamber are reacted and deposited on the surface in CVD mode when the purge time is shorter than the saturation. This deposited film is unsuitable for the gate oxide layer due to a low quality rather than ALD mode. Figure 4.2 (a) shows a self-limiting film growth range for pulse and purge times, not in CVD mode. Figure 4.2 (b) shows that our grap recipe for pulse and purge time is not CVD mode but ALD mode[19].

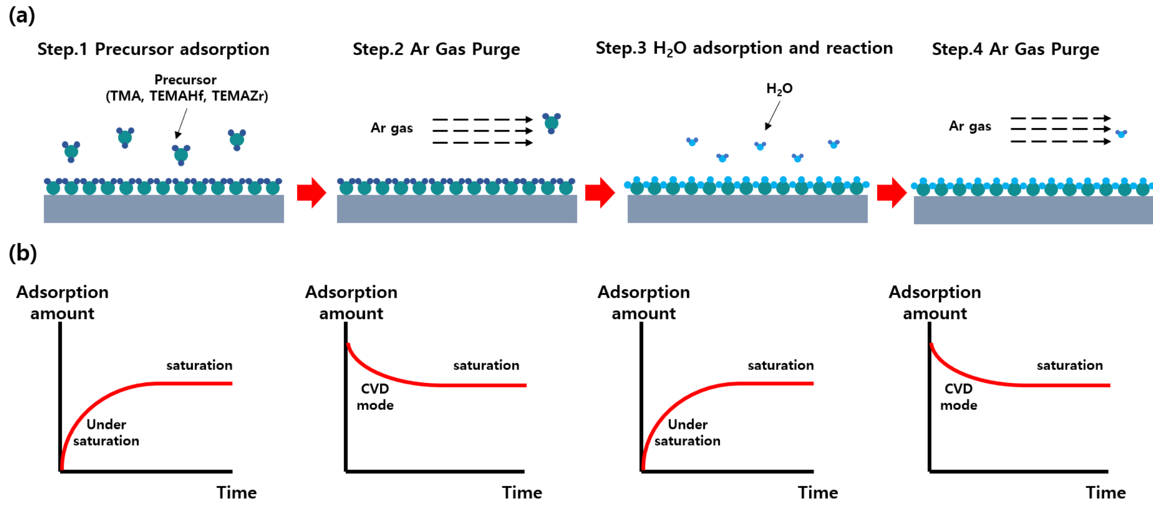
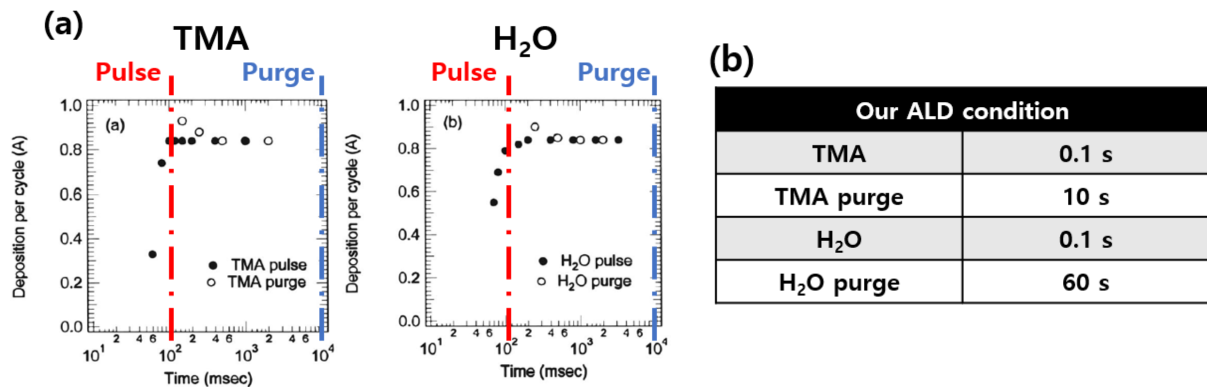


Fig. 4.1 (a) ALD process sequence. Steps Precursor adsorption, Ar Purge, H2O adsorption and reaction, Ar Purge respectively (b) Adsorption amount depending on pulse and purge time



Our ALD condition	
TMA	0.1 s
TMA purge	10 s
H_2O	0.1 s
H_2O purge	60 s

Fig. 4.2 (a) Pulse and purge time for deposition cycle depending on of TMA precursor and H_2O. (b) our group pulse and purge time for TMA and H_2O [19].

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4.1.2 Post-Deposition Annealing for Degassing Suppress

In performing the wafer bonding, the gas emitted from the thin film not only degrades the yield of wafer bonding but also damages the quality of the epi layer, i.e., the performance of the device is able to be degraded. Figure 4.3 (a) shows three types of chemisorption when a precursor is adsorbed on a surface. In the ligand exchange, the precursors are adsorbed on the wafer surface and exchange ligand with surface atom, this reacted by-product is emitted. In the association, the precursors are adsorbed on the wafer surface in the non-exchange state. On the other hand, In the dissociation, both the ligand-dissolved precursor and the dissociated ligand are adsorbed on the wafer surface. Also, this ligand is emitted in a gaseous condition after the annealing process and then, leads to a low-quality epi layer such as a wafer with void[19].

Figure 4.3 (b) shows the outgas mechanism in conventional ALD equipment and ALD + annealing process equipment. The annealing process is an important factor to remove volatile ligands. Figure 4.3 (c) shows the amount of C_2H_4(m/e=28) and C_3H_8(m/e=44) released from the $HfAlO_x$ film through the TDS(Thermal desorption spectroscopy). Additionally, we have confirmed a large number of ligands at 350°C above. Therefore, The annealing process after ALD deposition is an important factor to increase wafer bonding yield[20].

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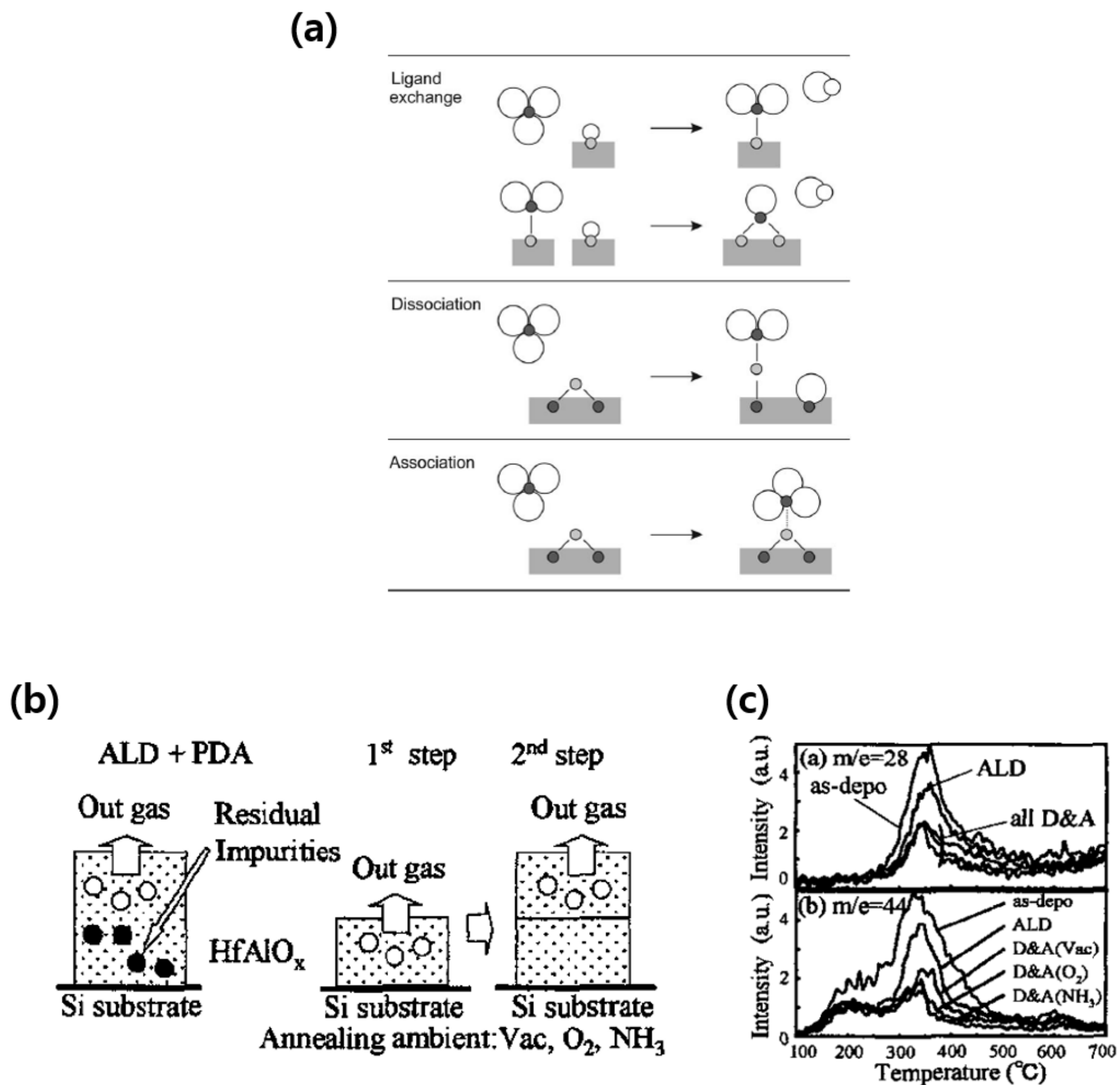


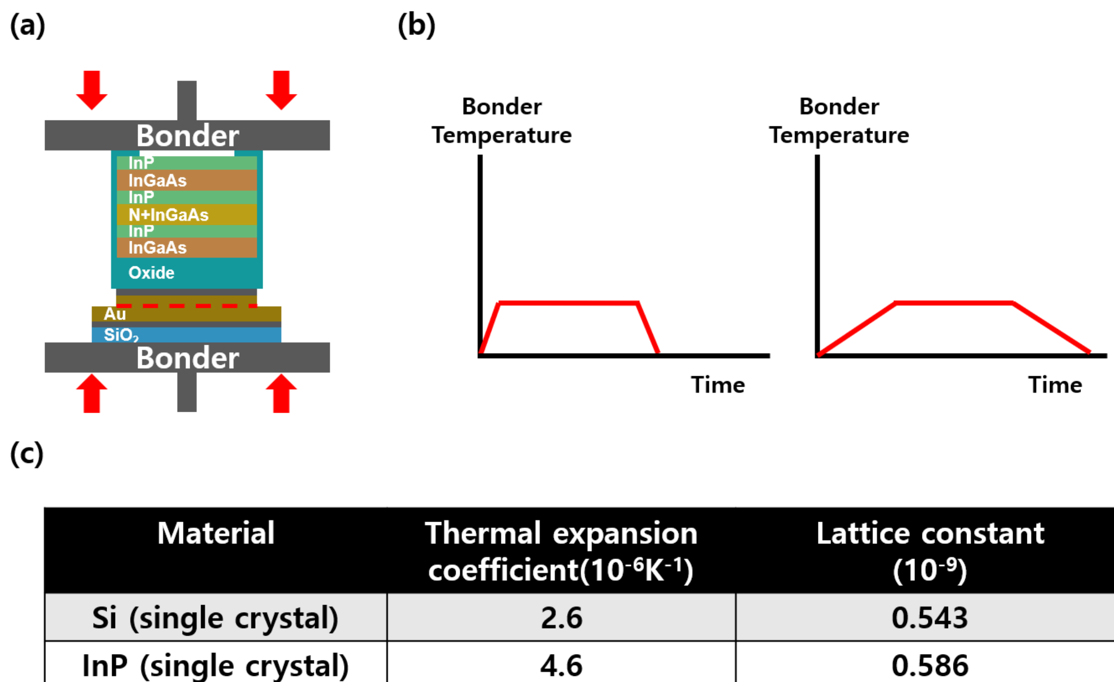
Fig 4.3 (a) chemical adsorption mechanisms identified for ALD top: ligand exchange. middle: dissociation of ML_3 in Surface. Bottom: association of the MLn species on the surface[19]. (b) out gas mechanism from HfAlOx film. (c) TDS spectra of our gas of C_2H_4 and C_3H_8 from $HfAlO_x$ film depending on PDA temperature[20].

4.1.3 Slowly Increase Bonding Temperature

Fig (a) shows the bonding process of Si wafer and InP wafer in high vacuum conditions (1.0×10^{-4} torr) after Ar plasma activation. The bonding surface is Au/W deposited by DC sputter. Bonder surface respectively provides thermal energy to the substrate of InP and Si wafer[22].

Fig (b) shows the rising, saturation, and falling steps of the top and bottom bonder thermal conditions. The left image indicates steep rising and falling conditions, while the right image indicates slow rising and falling conditions. Steps with different rising and falling conditions affect bonding yield due to thermal expansion coefficient.

Fig.(c) shows that silicon and Indium Phosphide have different lattice constants and thermal expansion coefficients[23].



Material	Thermal expansion coefficient($10^{-6}K^{-1}$)	Lattice constant (10^{-9})
Si (single crystal)	2.6	0.543
InP (single crystal)	4.6	0.586

Fig.4.4 (a) Bonding process (b) bonding process Temperature sequence (c) Si (single crystal)and InP(single crystal) thermal expansion and lattice constant

`

4.1.4 Back Eching Process

After the bonding process, back oxide(Al_2O_3, HfO_2/Al_2O_3, ZrO_2/Al_2O_3), which is deposited on the back side during gate oxide deposition, must be removed before etching InP/ InGaAs since making a non-etching layer such as the island and 111 direction stop layer.

Figure 4.5 (a) shows the process of removing the back oxide with BOE or 2% HF solution. The aforementioned process etched the back oxide as well as the side-oxide. On the other hand, Figure 4.5 (b) shows that the back-oxide was removed by the polishing process. This process only etches the back-oxide, not the side-oxide

Then, The InP/InGaAs/InP layer, which does not contribute to device characteristics, has been removed by an etching solution (HCl, H_3PO_4, HCl). Figure 4.5 (a) and (b) show that the device layer of the sample, in which the back etch process was performed by the BOE or HF solution, was attacked by the etching solution (HCl, H_3PO_4, HCl). On the other hand, the device layer of the sample using the polishing process was prevented by the etching solution

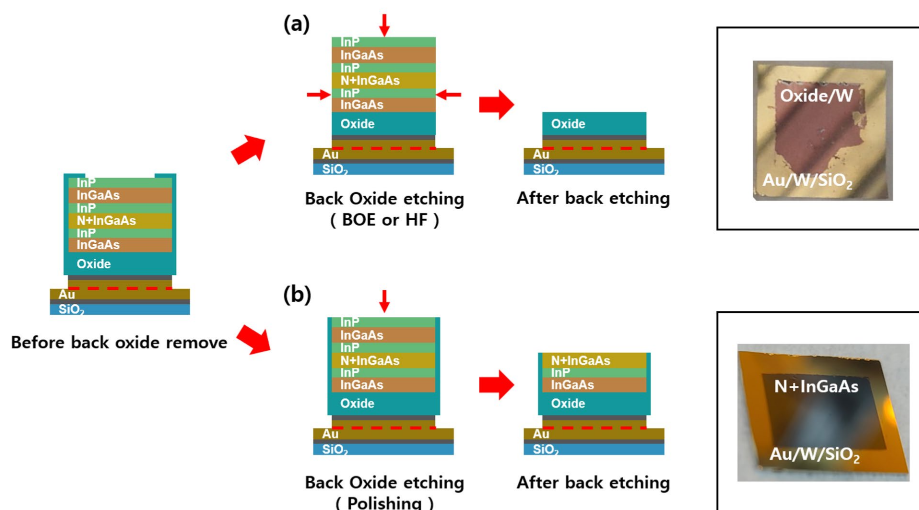


Fig.4.5 Image after bonding process, (a) back etching process flow after back oxide removal with HF or BOE (b) back etching process flow after back oxide removal with polishing

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4.2 Fabrication of Wafer-bonded InGaAs Photo-FET using metal reflector gate

Figure 4.6 shows the fabrication process flow, recipe, and optical Image. To fabricate Si on $In_{0.53}Ga_{0.47}As$, InP wafer and Si wafer were prepared. In the case of the Si wafer, 300 nm SiO2 was grown using a thermal oxidation process. W(10nm) / Au(10nm) was deposited through the DC sputtering equipment.

In the case of InP wafers, InP buffer(30nm)/$In_{0.53}Ga_{0.47}As$(200nm)/InP(50nm)/N+$In_{0.53}Ga_{0.47}As$(50nm) /InP(3nm) using molecular beam epitaxy (MBE) equipment. Then, Frist, the $In_{0.53}Ga_{0.47}As$ surface was cleaned with acetone, methanol, and deionized water step by step. second, $In_{0.53}Ga_{0.47}As$ surface native oxide remove and passivation prior to gate oxide deposition was gradually treated with NH_3OH, $(NH_4)_2S$, deionized water, third, Gate oxide formed, In case of Al_2O_3 Gate oxide, an Al_2O_3(10nm) gate oxide film was grown by using ALD(atomic layer deposition) alternating pulses of TMA (Tri-methyl aluminum) and H_2O precursors at 300◦C substrate. In the case of HfO_2 or ZrO_2 Gate oxide, an Al_2O_3(1nm)/HfO_2(9nm) or Al_2O_3(1nm)/ZrO_2(9nm) gate oxide film was grown by using ALD(atomic layer deposition)alternating pulses of TEMAHf (Tetrakis ethyl methyl amino hafnium) or TEMAZr(Tetrakis ethyl methyl amino zirconium) and H_2O precursors at 300◦C substrate. PDA (post-deposition Annealing) process was carried out for void formation suppression at the bonding process. Fourth, W(10nm)/ Au(10nm) was deposited through the DC sputtering equipment.

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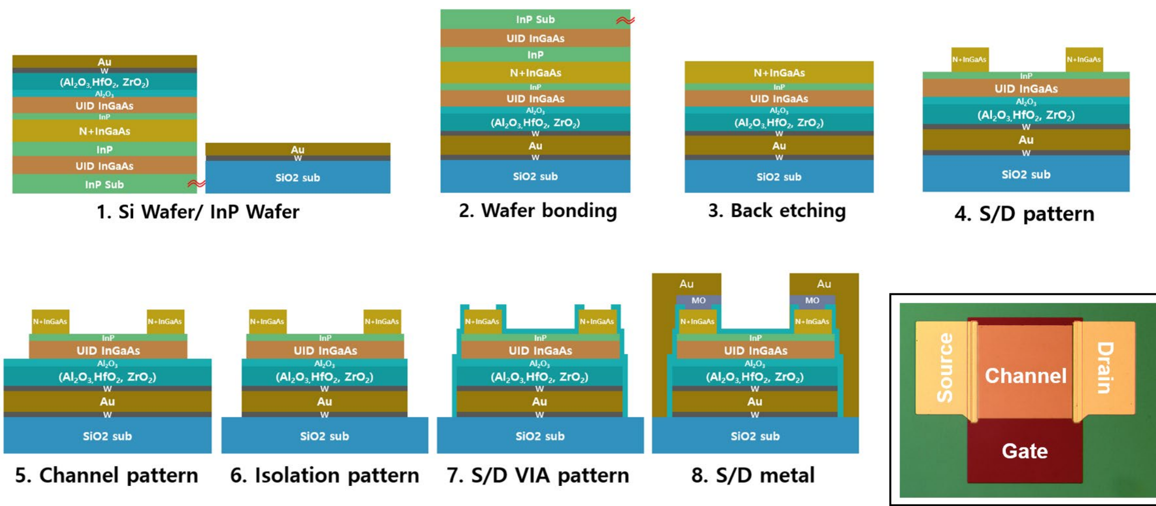
To make the bottom gate MOSFET structure, the surfaces of Si and InP wafers were activated through Ar plasma, and the two wafers were bonded at 200°C for about 1 hour with 25N force. the back oxide, which was generated during the gate oxide deposition with ALD, was removed through the polishing to prevent obstacles to the back etching process. Unused InP-sub/UID InGaAs/InP layers were removed using HCl solution (HCl : H_2O = 1.67 : 1) for about 2 hours , H_3PO_4 solution (H_3PO_4 : H_2O_2 : DI= 1 : 1 : 10) for about 5s, and HCl solution(HCl : H_3PO_4 = 1 : 3) for about 10s, respectively.

From S/D patterning to isolation patterning, the top-down method, which is etching sequentially from the top layer to the bottom layer, was used. First, N+InGaAs were etched using an H3PO4 solution (H3PO4: H2O2: DI= 1: 1: 10) for S/D formation. Second, InP/UID InGaAs were etched using HCl solution (HCl: H_3PO_4 = 1: 3) and H_3PO_4 solution (H_3PO_4: H_2O_2: DI= 1: 1: 10) for Channel formation. Third, in the case of Al_2O_3 gate oxide, Al2O3/W were etched using BOE (buffered Oxide Etchant) solution for 25s and RIE(reactive Ion etching) equipment at CF_4 20sccm, O_2 3sccm condition for 1min. in the case gate oxide of HfO_2 and ZrO_2, HfO_2 or ZrO_2/W was respectively etched using RIE at CF_4 20sccm, O_2 3sccm condition for 10min and 13min. the Au/W layer of all the sample was etched with aqua regia solution made before 30min for 20s. Residual W was etched for 30 seconds under the same conditions with RIE equipment.

Before Al2O3 (30nm) Passivation with ALD, InGaAs native oxide was removed by an HCl solution (HCl: H_2O = 1:10). And then, Al2O3 was etched by BOE solution for 25s to make S/D via.

Mo(20nm)/Au(200nm) was deposited with the e-beam evaporator equipment for S/D contact and pad. PMA was carried out for 1min in a nitrogen atmosphere at 250°C. Finally, the gate pad was opened with BOE solution to remove the Al_2O_3 film deposited during the passivation process.



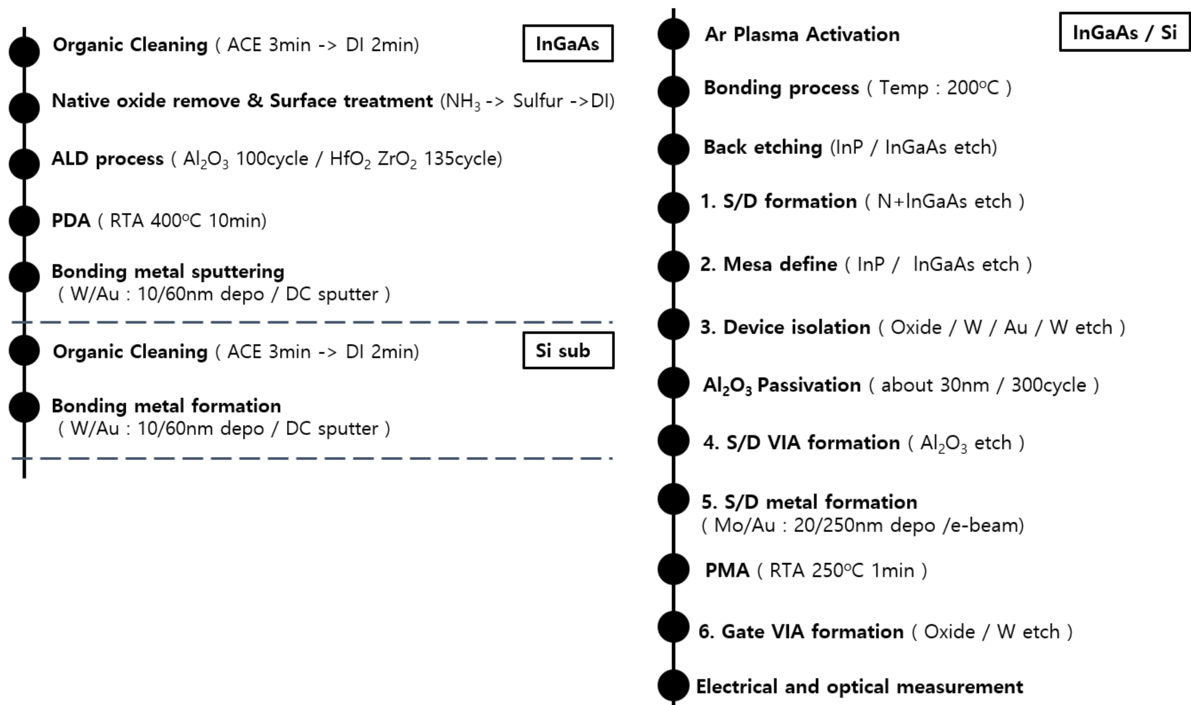


Fig.4.6 Fabrication flow of InGaAs photo-FETs with high-k metal Gate (b) optical microscopy Image of InGaAs Photo-FET

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4.3 Electrical Characteristics of InGaAs Photo-FET

Figure 4.7 shows the electrical characteristics of the gate oxides (Al_2O_3, HfO_2/Al_2O_3, ZrO_2/Al_2O_3) of the InGaAs Photo FET. Figures (a) and (b) show that the data based on I-V measurements and C-V measurements have been extracted[11][16].

Since ZrO_2 has the largest permittivity, InGaAs Photo-FET with ZrO_2 gate oxide has the highest drain current as shown in figure 4.7 (a). I_d is 8.0x10^{-6}, 9.3x10^{-6}, 1.2x10^{-5} A/um, respectively.

The C_{ox}(capacitance oxide) was measured by the split C-V measurement method, which is Ground for S/D and voltage sweep for Gate. the capacitance of two samples, which length and width is respectively 100x100um and 50x100um, were subtracted to eliminate parasitic capacitance as follows

$$C_{total\ (100x100um)} - C_{total\ (50x100um)} = C_{ox\ (50x100um)},\ C_{ox} = \frac{C_{ox\ (50x100um),}}{Area(50x100um)}$$

The calibrated C_{ox} is the largest for InGaAs Photo-FET with the ZrO_2 gate oxide as shown in figure 4.7 (b). C_{ox} is 0.65 1.13 1.88 F/cm^2, respectively.

Figure 4.7 (c) shows S.S(Subthreshold Swing) depending on gate oxide material. S.S have been calculated based on I-V measurement data as follows

$$S.S = \frac{d\,V_G}{d(log\ I_d)}$$

The S.S of InGaAs Photo-FET is the lowest in Al_2O_3 gate oxide as shown in figure 4.7 (c). S.S is 117 146 136, respectively.

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Figure 4.7(d) shows the calculated μ_{eff} (effective mobility) based on the equation:

$$u_{eff} = \frac{I_d L}{W\, C_{ox}(V_g - V_{th})\, V_d}, N_s = \frac{C_{ox}(V_g - V_{th})}{q}$$

Where I_d, L, W, C_{ox}, V_g, V_{th}, and V_d is drain current, channel length, width, capacitance oxide, gate voltage, threshold voltage, and drain voltage, respectively. The μ_{eff} of InGaAs Photo-FET is the highest Al_2O_3 gate oxide as shown in figure 4.7 (d). The peak μ_{eff} is 872, 645, and 475 cm^2/Vs, respectively.

Also, CET(Capacitance Equivalent Oxide) has been calculated with the following equation:

$$CET = \frac{3.9}{C_{ox}}$$

The CET of InGaAs Photo-FET is the lowest ZrO_2 gate oxide as shown in figure 4.7 (c). The CET is 5.28, 3.04, and 1.83 nm, respectively.

The measured and calculated electrical characteristics of InGaAs Photo-FET show well-known high-k material properties. even though all devices have the same interfacial layers such as Al2O3, have different characteristics.

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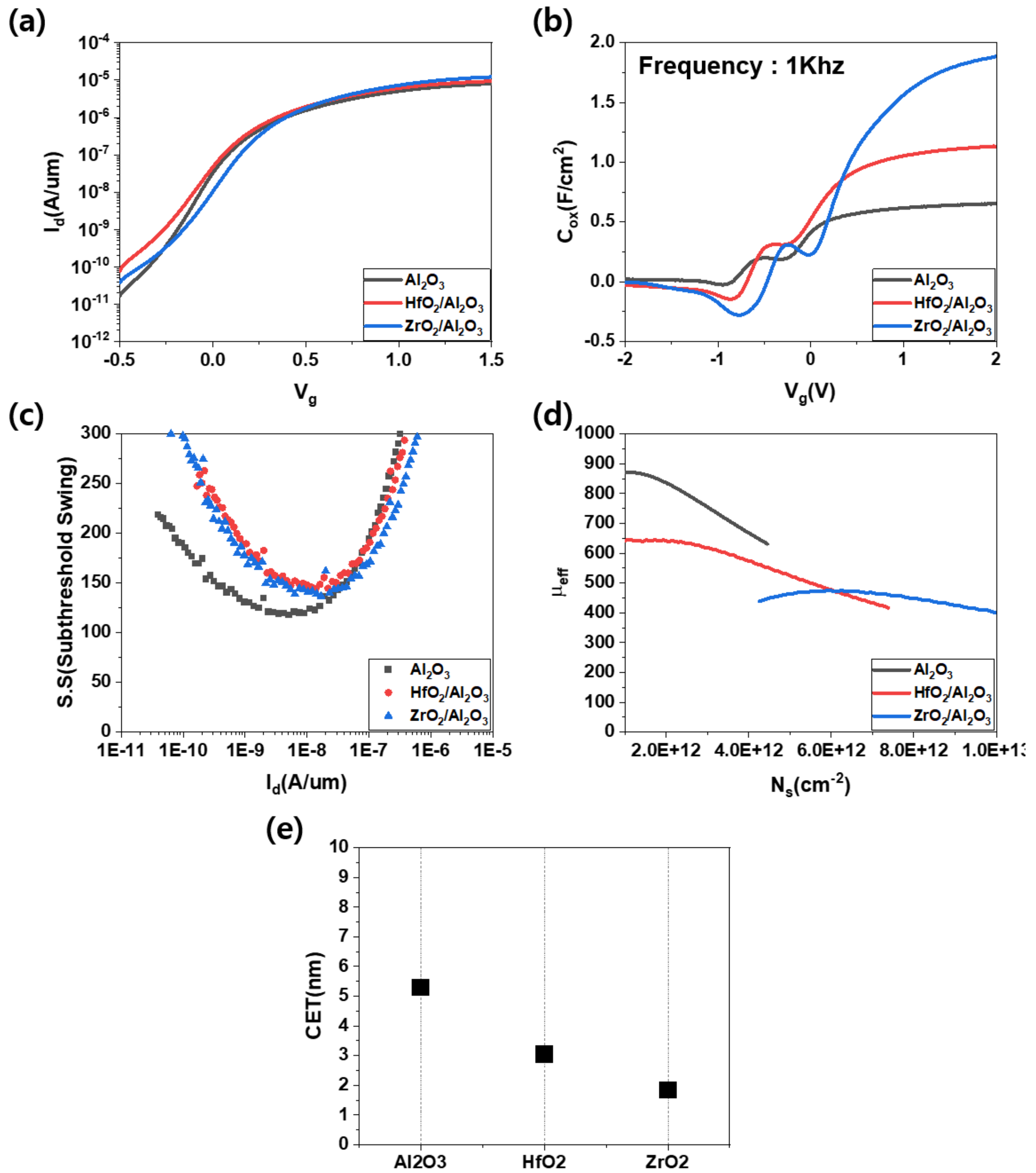

Fig.4.7 Electrical characteristics of InGaAs Photo FET depending on Al_2O_3 HfO_2/Al_2O_3, ZrO_2/Al_2O_3 gate oxide. (a) I_d–V_g, (b) C_{ox}–V_g. (c) S.S(Subthreshold Swing)–I_d. (d) μ_{eff}(effective mobility)-N_s(channel carrier density) (e) CET(Capacitor Equivalent Thickness)

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4.4 Optical Characteristics of InGaAs Photo-FET

4.4.1 Channel and Gate Reflectance Measurement

The reflectance of InGaAs Photo-FET was measured and discussed by VIS(visible) and SWIR(short wave infrared wavelength) microscopic spectroscopy depending on the gate oxide material to confirm the effect of high-k/Al_2O_3/W/Au/Au stack. Figure 4.8 shows the InGaAs MOSFET cross-section for channel and gate region, where gate oxide materials are respectively Al_2O_3, HfO_2/Al_2O_3, and ZrO_2/Al_2O_3. Figure 4.8 (b) shows the measured reflectance spectrum in the range of VIS and SWIR range for the channel of InGaAs Photo-FET, where the channel region is Al_2O_3(30nm)/InP(3nm)/ InGaAs(50nm)/Al_2O_3(1nm)/high-k(9nm)/W(10nm)/Au(120nm)/W(10nm). The measured spectrum for all channel region indicate the lowest reflectance at 1250nm, i e., all device indicate high absorption in the SWIR range. On the other hand, Figure 4.8 (c) shows the measured reflectance spectrum in the range of VIS and SWIR range for the gate region of InGaAs Photo-FET, where the gate is Al_2O_3(31nm)/high-k(9nm)/W(10nm) /Au(120nm)/ W(10nm). The measured spectrum for all gate region indicates the lowest reflectance at 450nm but high reflectance in the SWIR range[9].

Therefore, we have reconfirmed that the channel layer, which is InP(3nm)/InGaAs(50nm), between Al_2O_3(30nm) and high-k(9nm) highly absorb photon in the SWIR range

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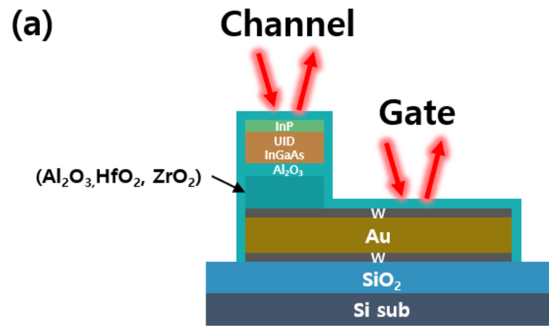

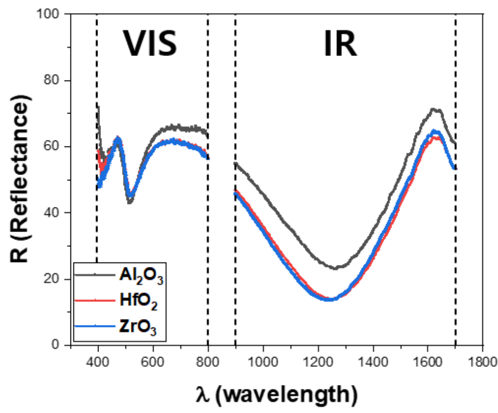

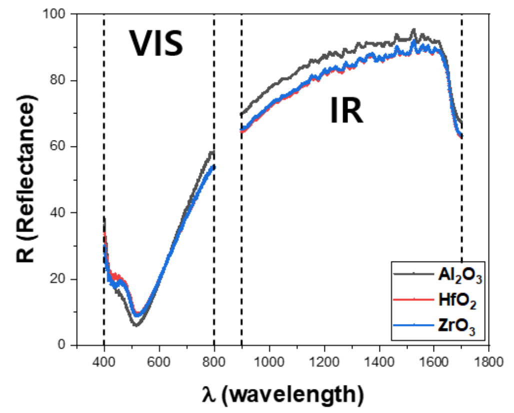

Fig 4.8 (a) The channel and gate of reflectance comparison of InGaAs Photo-FET (b) reflectance for a channel region in the range of VIS and SWIR (c) reflectance for gate region in the range of VIS and SWIR

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4.4.2 Confocal Microscopy System

the additional optical setup is required to detect photocurrent. Figure 4.9 (a) shows the setup for measuring the photocurrent. The light emitted from the laser reaches the attenuator via the optical fiber. the attenuator reduces optical power(e.g loss from 10 to 50dB,and lossless) and then this light is reached at the convex lens. This transfer to the parallel light with compensation of concave and convex lenses. The light sequentially passes through a half mirror, x10 IR lens, and finally reaches the channel of the InGaAs Photo-FET. The reached 1550nm laser source is shown in Figure 4.9 (b).

First, after zero point correction, the optical power was measured with InGaAs detector. The optical power reduced by the attenuator have been presented in figure 4.11[24].

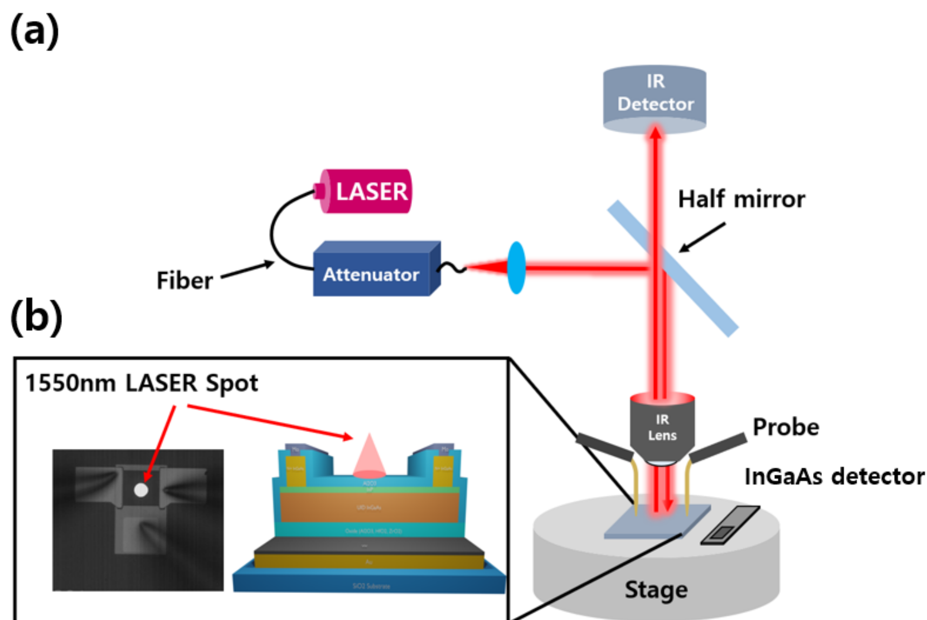

Fig. 4.9 (a) Photocurrent measurement system(confocal microscopy) with 1550nm laser (b) (b) IR image and cross-section of InGaAs Photo-FET injected with 1550 nm light source

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4.4.3 Optoelectrical Characteristics of InGaAs Photo-FET for 50x50um

Figure 4.10 show I_d–V_g characteristic of InGaAs Photo-FET for 50 x 50um under various light power of 1550nm wavelength depending on the gate oxide material (Al_2O_3, HfO_2/Al_2O_3, ZrO_2/Al_2O_3). The optical power was measured with an optical power meter and was 118.78, 11.119, 1.140, 0.1332, 0.013, and 0.13 uW from the dark line to the yellow line, respectively. the I_{light} for Al_2O_3, HfO_2, and ZrO_2 are 4.72x10^{-4}, 5.53x10^{-4}, and 6.75x10^{-4} at V_g=1.5V and P_{in}=118.78 condition, respectively. As expected from the object section, I_{light} indicated the highest at ZrO_2/Al_2O_3 gate oxide in on-state. On the other hand, I_{light} was difficult to estimate the trend due to the insufficient voltage sweep range at the off-state.

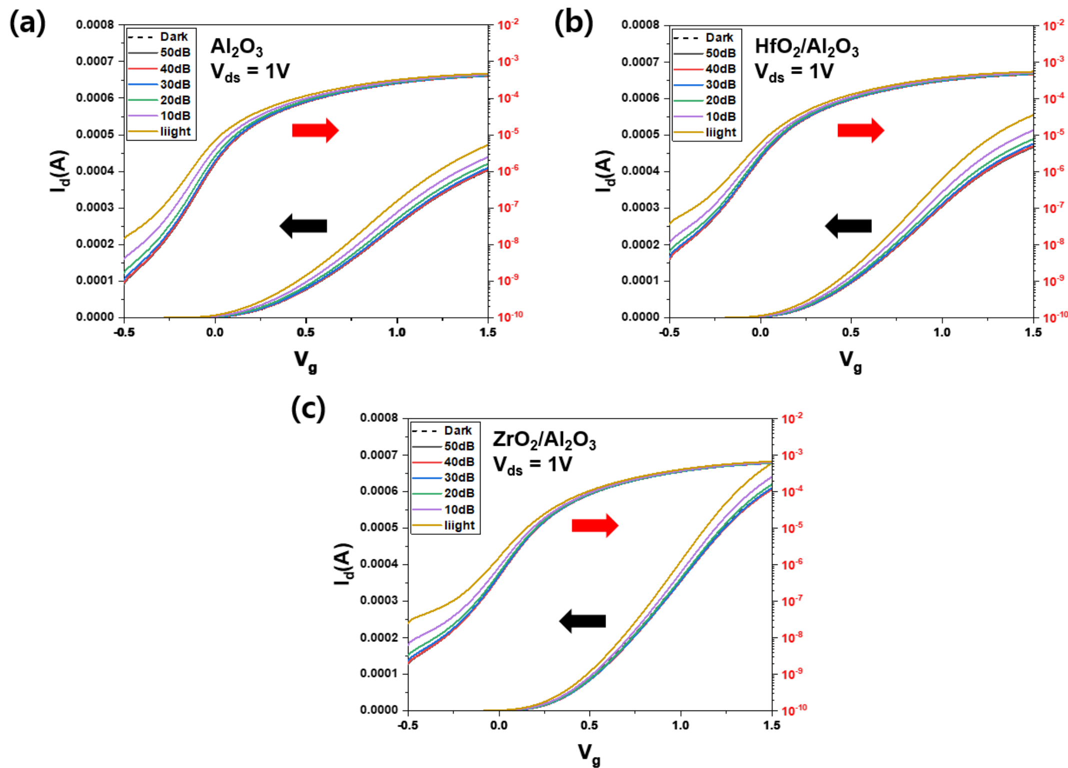

Fig. 4.10 I_d-V_g characteristic of InGaAs Photo-FET for 50x50um under various light power of 1550nm wavelength depending on (a) Al_2O_3 gate oxide (b) HfO_2/Al_2O_3 gate oxide (c) ZrO_2/Al_2O_3 gate oxide

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Figure 4.11 figure shows I_{ph} -V_g characteristics of InGaAs Photo-FET for 50 x 50um with various optical power of 1550nm depending on gate oxide material, which I_{ph} is the photocurrent and can be understand through the following equation :

$$I_{\mathrm{ph}} = I_{\mathrm{light}} - I_{\mathrm{dark}}.$$

Where I_{ph}, I_{light}, and I_{dark} is photocurrent, light current, dark current, respectively. Although the HfO_2/Al_2O_3 gate oxide sample shows higher (I_{ph}) photocurrent than Al_2O_3, ZrO_2/Al_2O_3 shows the lowest photocurrent. This appears different from the aforementioned tendency of I_{ight}. Plus, ZrO_2/Al_2O_3 gate oxide show negative photocurrent under weak light power. This phenomenon was assumed that electron generated by photons have been trapped in the gate oxide. As shown in Chater.3. We confirmed at InGaAs MOS capacitor that ZrO_2/Al_2O_3 material not only dropped the highest E-field in gate oxide under the same voltage but also showed the highest N_{st}(slow trap density).

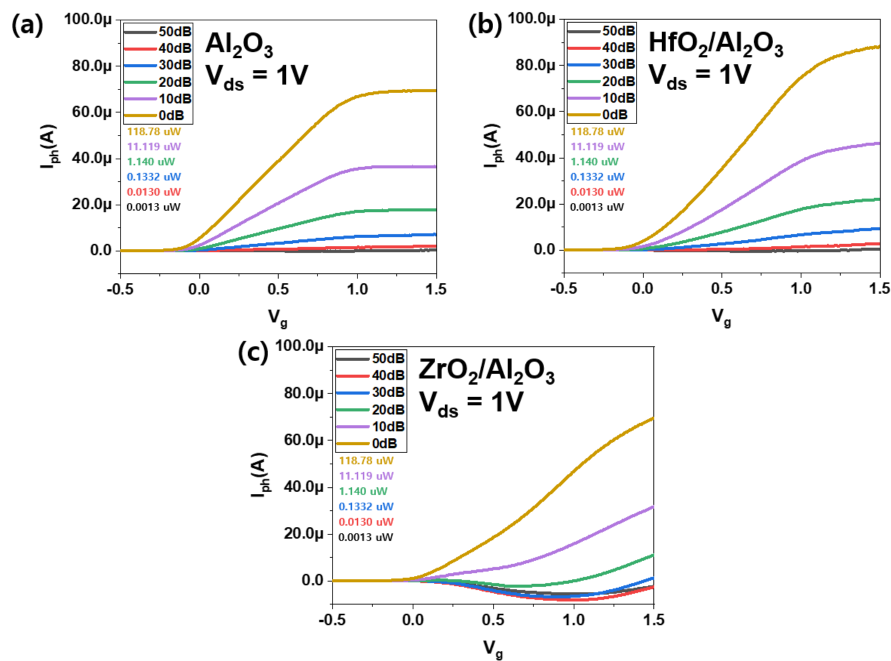

Fig.4.11 I_{ph}-V_g characteristic of InGaAs Photo-FET for 50x50um under various light power of 1550nm wavelength depending on (a) Al_2O_3, (b) HfO_2/Al_2O_3, and (c) ZrO_2/Al_2O_3 gate oxide

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Figure 4.12 shows the R(responsivity) depending on gate oxide materials at V_{gs}=1V + V_{th}, which is Al_2O_3(dark dot), HfO_2/Al_2O_3(red dot), and ZrO_2/Al_2O_3(blue dot), respectively. The R (Reactivity) was calculated using the following equation:

$$R = EQE\left(\frac{q\lambda}{\mathrm{hc}}\right)G = \frac{I_{\mathrm{ph}}}{P_{\mathrm{in}}}.$$

Where EQE, q, λ, h, c, G, I_{ph}, P_{in} are external quantum efficiency, elementary charge, the light wavelength, planck constant, speed of light, photoconductive gain, photocurrent, and optical power, respectively. As expected based on the data confirmed in Figure 4.11, reactivity was also confirmed that the HfO_2/Al_2O_3 gate oxide is higher than that of Al_2O_3 in range of optical power. On the other hand, ZrO_2/Al_2O_3 gate oxide indicate the lowest R in range of optical powers. Especially, it show negative responsivity due to negative photocurrent at weak light power(below 0.1uW)[5][6][9].

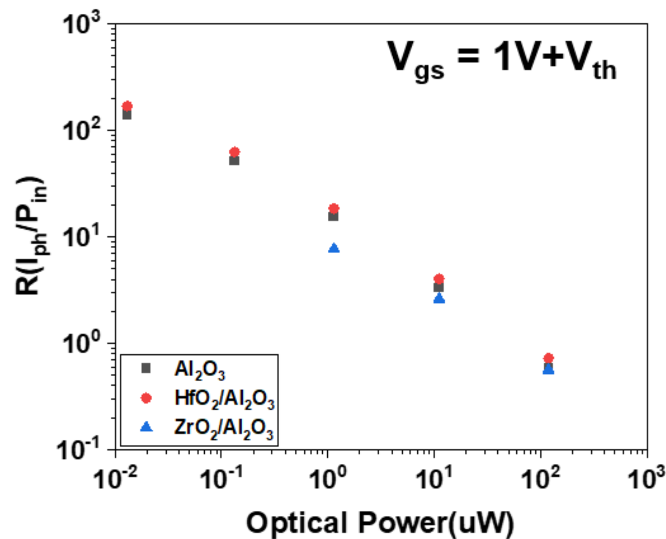

Fig 4.12 Responsivity of InGaAs Photo-FET with various optical power of 1550nm wavelength for InGaAs Photo-FET depending on gate oxide(Al_2O_3, HfO_2/Al_2O_3, ZrO_2/Al_2O_3)

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4.4.4 Optoelectrical Characteristics of InGaAs Photo-FET for 10x50um

Figure 4.13 shows Id-Vg characteristics of InGaAs Photo-FET for length(10um) and width(50um) under on-off-light with 1550nm wavelength depending on gate oxide materials(Al_2O_3, HfO_2/Al_2O_3, ZrO_2/Al_2O_3). the I_{light} for Al_2O_3, HfO_2, and ZrO_2 are $2.24x10^{-3}$, $2.35x10^{-3}$, and $2.59x10^{-3}$ at V_g=1.2V and P_{in}=118.78 condition. As we have discussed in figure 4.10. Also, InGaAs Photo-FET for 10x50um shows the highest I_{light} at ZrO_2/Al_2O_3 gate oxide. Additionally, in negative bias.

In contrast to InGaAs Photo-FET with long channel lengths, we have confirmed a large increase rate of drain current at the short channel lengths. the I_{light} for Al_2O_3, HfO_2, and ZrO_2 are $2.19x10^{-6}$, $3.38x10^{-6}$, and $5.19x10^{-6}$ at V_g=-2.5 and P_{in}=118.78 condition.

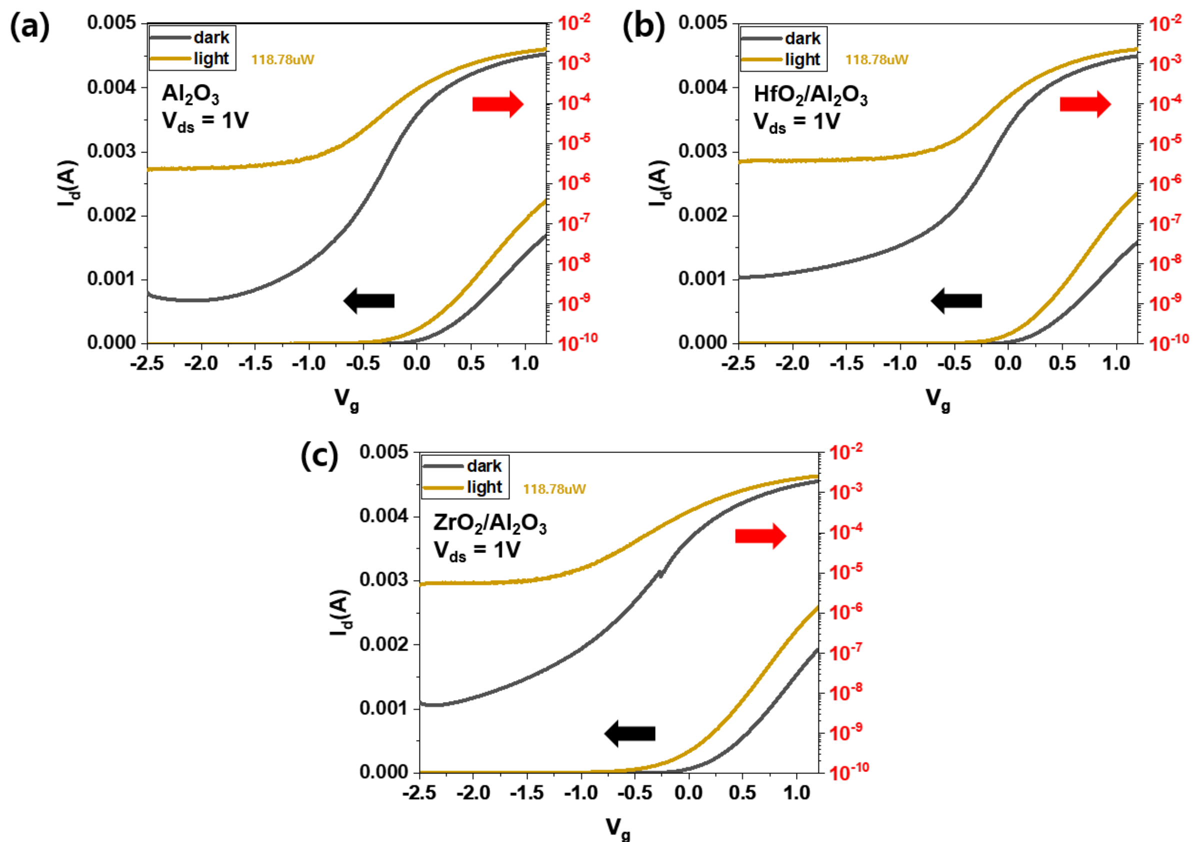

Fig. 4.13 I_{light}, I_{dark} – V_g characteristic of InGaAs Photo-FET 10x10um under various light power of 1550nm wavelength depending on gate oxide material (a) Al_2O_3 (b) HfO_2/Al_2O_3 (c) ZrO_2/Al_2O_3

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4.4.5 Responsivity Comparison for Cannel Lngths of 50um and 10um

We investigate the photocurrent of InGaAs Photo-FET for 50x50um and 10x50um in the previous chapter. In this chapter, we compare the responsivity of the device at V_{ds}=1V depending on the channel length. Figures (a) and (b) show the responsivity of 50um and 10um depending on gate oxide material(Al_2O_3, HfO_2/Al_2O_3, ZrO_2), respectively. The responsivity was calculated using the equation. Figure 4.14 (a) and (b) show that the responsivity of channel length 10um is about 10 times larger than 50um at On-state(Vg above 0.5V). Also, we expect that the responsivity of channel length 10um is about 100 times larger than 50um at off-state(Vg below -0.5V).

These results can be understood based on the following equation:

$$G = \frac{\tau_{lifetime}}{\tau_{transit}} = \frac{\tau_{lifetime}}{L^2}\mu V_{ds}.$$

Where $\tau_{lifetime}$, $\tau_{transit}$, L, μ, V_{ds} is minor carrier lifetime, carrier transit time, channel length, carrier mobility, drain-source voltage, respectively. Based on the R(responsivity) and Gain equations, we confirm that not only the channel length but also the minor carrier lifetime contributes to the gain. Also, the responsivity equation includes this gain parameter[5][6][9].

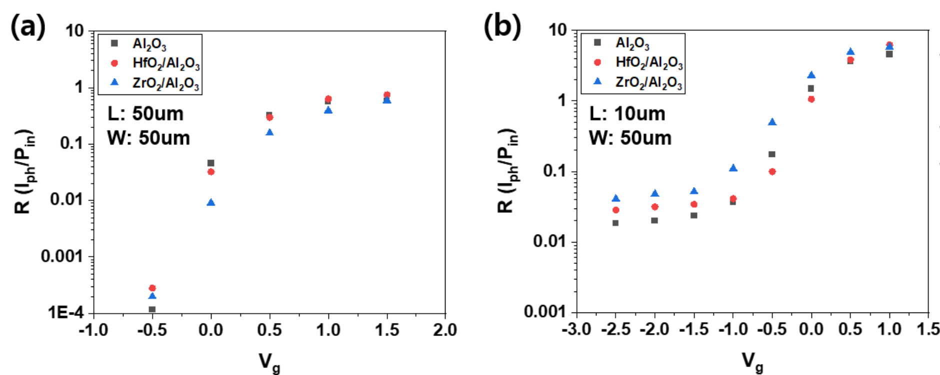

Fig 4.14 Responsivitiy comparison for channel length (a)50um and (b)10um depending on gate oxide material

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5. Conclusion

First, interface trap and slow trap density were evaluated through C-V measurement of W/high-k/Al2O3/InGaAs capacitor. We have confirmed that all PMA condition is lower interface trap and slow trap densities than PDA conditions. However, PDA process is required to optimize the bonding process of InGaAs MOS wafer and Si wafer. In addition, We have also confirmed several papers reporting C_2H_4 and C_3H_8 emissions with annealing condition of 350°C above. Therefore, we fabricated an InGaAs Photo FET on Si wafer with 400oC PDA process conditions. The electrical characteristic of three conditions (ZrO_2/Al_2O_3, HfO_2/Al_2O_3, Al_2O_3) were investigated. The drain current was the highest for ZrO_2/Al_2O_3 gate oxide and the lowest for Al_2O_3 gate oxide. This is because of the difference in dielectric constant of ZrO_2, HfO_2, Al_2O_3.

Additionally, etch gate oxides of optical properties were measured. first, devices have the reflectivity similar in the SWIR wavelength region. second, the photo current was measured the highest in HfO_2/Al_2O_3 and the lowest in ZrO_2/Al_2O_3. This phenomenon is becase gate oxides have different D_{it} and slow trap sites under the same voltage conditions.

Finally, the off-state showed a much higher increase rate of responsivity than the on-state under the decrease of channel length.

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Reference

[1] J.J.S. Huang et al., "Temperature dependence study of mesa-type InGaAs/InAlAs avalanche photodiode characteristics," Advances in OptoElectronics 2017.

[2] F. H. L. Koppens et al., "Photodetectors based on graphene, other two-dimensional materials and hybrid systems," Nat. Nanotechnol 2014.

[3] H. Tsugawa et al., "Pixel/DRAM/logic 3-layer stacked CMOS image sensor technology" 2017 IEEE International Electron Devices Meeting (IEDM)(2017)

[4] S. Manda et al., "High-definition Visible-SWIR InGaAs Image Sensor using Cu-Cu Bonding of III-V to Silicon Wafer" (IEDM)(2019)

[5] Kasap, Safa O. "Optoelectronics and Photonics: Principles and Practices. 2001."

[6] Dominik Kufer et al., "Photo-FETs: Phototransistors Enabled by 2D and 0D Nanomaterials" ACS Photonics (2016)

[7] Takaya Ochiai1 et al, "Ultrahigh-sensitivity optical power monitor for Si photonic circuits Ultrahigh-sensitivity optical power monitor for Si photonic circuits" Arixv (2021)

[8] Yida Li et al, "A flexible InGaAs nanomembrane PhotoFET with tunable responsivities in near- and short-wave IR region for lightweight imaging applications" APL materials (2019)

[9] SOOSEOK KANG et al., "Cavity-enhanced InGaAs photo-FET with a metal gate reflector fabricated by wafer bonding on Si" Optics Express(2021)

[10] Hei Wong et al., "On the scaling of subnanometer EOT gate dielectrics for ultimate nano CMOS technology" Microelectronic Engineering(2015)

[11] SCHRODER, Dieter K. "Semiconductor material and device characterization." John Wiley & Sons, 2015.

`

[12] Paul K. et al., "The Characterization and Passivation of Fixed Oxide Charges and Interface States in the Al2O3/InGaAs MOS System"IEEE TRANSACTIONS ON DEVICE AND MATERIALS RELIABILITY(2013)

[13] Seong Kwang Kim et al., "Fabrication and characterization of Pt/Al2O3/Y2O3/In0.53Ga0.47As MOSFETs with low interface trap density" APPLIED PHYSICS LETTERS (2017)

[14] Seong Kwang Kim et al., "Impact of Ground Plane Doping and Bottom-Gate Biasing on Electrical Properties in In0.53Ga0.47As-OI MOSFETs and Donor Wafer Reusability Toward Monolithic 3-D Integration With In0.53Ga0.47As Channel"IEEE TRANSACTIONS ON ELECTRON DEVICES (2018)

[15] S.-H. Yoon et al., "Re-examination of effects of sulfur treatment on Al2O3/InGaAs metal-oxide-semiconductor interface properties" Journal of Applied Physic(2019)

[16] TAUR, Yuan; NING, Tak H. "Fundamentals of modern VLSI devices." Cambridge university press, 2021.

[17] Mengnan Ke et al., "Slow Trap Properties and Generation in Al2O3/GeOx/Ge MOS Interfaces Formed by Plasma Oxidation Process" ACS Appl. Electron. Mater (2019)

[18] Mengnan Ke et al., "Properties of slow traps of ALD Al2O3/GeOx/Ge nMOSFETs with plasma post oxidation" APPLIED PHYSICS LETTERS (2016)

[19] Riikka L. Puurunena et al., “Surface chemistry of atomic layer deposition: A case study for the trimethylaluminum/ water process” J. Appl. Phys(2005)

[20] T. Nabatame et al., “Design and Proof of High Quality HfAlOx Film Formation for MOSCAPs and nMOSFETs through Layer-by-Layer Deposition and Annealing Process” VLSI (2003)

[21] Jae-Hoon Han., "Study on void reduction in direct wafer bonding using Al2O3/HfO2 bonding interface for highperformance Si high-k MOS optical modulators" Japanese Journal of Applied Physics(2016)

`

[22] Q.-Y. Tong et al., "Low Vacuum Wafer Bonding" Electrochemical and Solid-State Letters (1998)

[23] Donato Pasquariello and Klas Hjort "Plasma-Assisted InP-to-Si Low Temperature Wafer Bonding"IEEE JOURNAL ON SELECTED TOPICS IN QUANTUM ELECTRONICS (2002)

[24] Kazuaki Oishi et al "Spectral Responsivity Characteristics of Front-Side Illumination InGaAs PhotoFETs on Si"Phys. Status Solidi A (2021)

[25] Roda Nur et al., "High responsivity in MoS2 phototransistors based on charge trapping HfO2 dielectrics" COMMUNICATIONS MATERIALS(2020)

[26] Tatsuro Maeda et al., "High and broadband sensitivity frontside illuminated InGaAs photo fieldeffect transistors (photoFETs) with SWIR transparent conductive oxide (TCO) gate" Applied Physics Letters(2021)

[27] Tatsuro Maeda et al., "InGaAs photo field-effect-transistors (PhotoFETs) on half-inch Si wafer using layer transfer technology" Japanese Journal of Applied Physics(2020)

[28] V. Masteika et al., "A Review of Hydrophilic SiliconWafer BondingECS Journal of Solid State" ECS Journal of Solid State Science and Technology (2014)

[29] gerasimos Konstantatos et al., "nanostructured materials for photon detection" nature nanotechnology (2010)

[30] Roda Nur et al., "A floating gate negative capacitance MoS2 phototransistor with high photosensitivity" Nanoscale (2022)

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Abstract (in Korea)

Si 기판 상에 웨이퍼 본딩 기법으로 제조된 $In_{0.53}Ga_{0.47}As$ Photo-FET의 고유전율 게이트 산화물에 관한 연구

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SWIR(Short-wave infrared) 감지기는 Si Photonics, 의료 기기, LiDAR 센서 및 양자 컴퓨팅에 널리 사용되어왔다. 특히 $In_{0.53}Ga_{0.47}As$는 InP 웨이퍼와 격자상수 정합 및 높은 흡수 계수로 인해 SWIR 파장을 감지하는 데 사용되어왔다. PIN 및 APD 구조는 $In_{0.53}Ga_{0.47}As$ 광 검출기에 널리 사용된다. 그러나 PIN은 내부 이득을 제공하지 않고 APD는 과도한 노이즈가 큰 높은 작동 전압으로 인해 약한 빛을 감지하는 데 어려움이 있다[1]. 이러한 문제점을 해결하기 위해 내부 이득이 중간이고 동작 전압이 낮은 Photo-FET가 연구되고 있다. 최근 유기 및 2차원 물질 기반의 Photo-FET 구조에 대한 연구가 활발히 진행되고 있으나, 이 물질들은 이동도가 낮아 SWIR 영역에 적합하지 않다[2].

2장에서는 선행 연구와 본 논문의 목적을 보여준다. 이전 연구에서는 웨이퍼 본딩 기술로 $In_{0.53}Ga_{0.47}As$ 기반의 Photo-FET를 제작하고 P+Si 게이트와 메탈 게이트(W/Au/W) 구조의 광전기적

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특성을 비교하였다. 그 결과, 금속 게이트가 SWIR 파장 범위에서 광학 제한으로 인해 P+Si 게이트보다 2배 더 높은 응답성을 가짐을 확인하였다. 본 연구에서는 InGaAs Photo-FET의 응답성을 향상시키기 위해 CMOS 기술 로드맵에서 게이트 구동성을 높이기 위해 일반적으로 사용되는 방법인 Al_2O_3 게이트 산화물을 고유전율 게이트 산화물(HfO_2/Al_2O_3, ZrO_2/Al_2O_3)로 대체하는 작업을 수행하였다. 또한, Photo FET의 작동 메커니즘이 알아보고 Iph(광전류)에 기여하는 광 전도 및 광 게이팅 효과를 설명한다.

3장에서는 $In_{0.53}Ga_{0.47}As$ MOS 커패시터의 공정 흐름을 먼저 제시하고 PDA 및 PMA 온도 조건에 따라 인터페이스 트랩과 슬로우 트랩을 평가하였다. 이러한 인터페이스 트랩과 슬로우 트랩은 각각 terman 방법과 V_{start} 고정 및 V_{end} 차이를 이용한 C-V 측정 방법으로 평가하였다.

4장에서는 높은 본딩 수율과 양질의 epi를 위한 웨이퍼 본딩 공정의 최적화 조건을 보여주고, InGaAs Photo FET의 전반적인 공정 흐름을 제시한다. 또한, 이 장에서는 Al_2O_3, HfO_2/Al_2O_3 및 ZrO_2/Al_2O_3의 게이트 산화물을 사용한 InGaAs Photo-FET의 공초점 현미경 및 광전기적 평가와 같은 측정 방법을 제시한다. 또한, 채널 길이(10um, 50um)에 따른 소자의 광전기적 특성을 제시한다.

Keywords: $In_{0.53}Ga_{0.47}As$, 포토트랜지스터, 포토FET, MOS 커패시터, MOSFET, M3D, 웨이퍼 본딩, high-k 유전체.