850 nm VCSEL based low-power transmitter for high-speed optical interconnection

Jun-Seo Kim

The Graduate School
Yonsei University
Department of Electrical and Electronic Engineering

850 nm VCSEL based low-power transmitter for high-speed optical interconnection

A Master's Thesis
Submitted to the Department of Electrical and Electronic Engineering
and the Graduate School of Yonsei University
in partial fulfillment of the requirements for the degree of
Master of Science

Jun-Seo Kim

December 2022

This certifies that the master's thesis of Jun-Seo Kim is approved.

_____

Thesis Supervisor: Woo-Young Choi

_____

Tae Wook Kim

_____

Tae-Hwan Jin

The Graduate School

Yonsei University

December 2022

Table of Contents

List of Tables

List of Figures

Abstract

850 nm VCSEL based low-power transmitter for high-speed optical interconnection

Jun-Seo Kim

Dept. of Electrical and Electronic Engineering

The Graduate School

Yonsei University

With the development of cloud services and mobile contents businesses, data traffics to be handled in data centers are increasing every year. Within the data center, optical interconnection is one of the attractive solutions as it has very low channel loss. An 850-nm Vertical-Cavity Surface-Emitting Laser (VCSEL) based short reach optical link is being actively developed because it is inexpensive and can have a relatively high data rate. Non-return-to-Zero method, which is a direct modulation method, has been traditionally used. Recently, Pulse Amplitude Modulation level-4 (PAM4) signaling has been used as a method to increase data-rate. Since VCSEL is a semiconductor laser diode that can be produced on a wafer basis, it has advantages of the price, but has disadvantages such as non-linear properties, processes and temperature variations.

In this paper, I would like to analyze various properties necessary to operate 850 nm VCSEL at high-speed for optical interconnection. The VCSEL model for SPICE simulation was made based on Verilog-A. The s-parameter of VCSEL at various current conditions and Light-Current-Voltage(L-I-V) data were fitted. The VCSEL driver was designed to have low power consumption compared to current-mode(CM) structure by using the

inverter-type voltage-mode (VM) driver as a basic structure. Inverter-type g_m/g_m amplifiers that have low Total Harmonic Distortion(THD) were adopted and it can control output resistance by I^2C. Due to the characteristic that DC curve of VCSEL is a non-linear response, there is a problem that the Level Mismatch Ratio (RLM) may be considerably low when driving PAM-4. To solve this problem, the driver was designed to compensate RLM of optical transmitter through pre-distortion at the driver stage.

Key words: high-speed optical link, 850 nm VCSEL, VCSEL SPICE model, VM Driver, low-power, non-linearity, RLM, pre-distortion

1. Introduction

1.1 High-speed Optical Interconnects

With the development of cloud services and mobile services, the number of data traffic which have to handle in data centers(DC) is increasing every year. The datacom and the telecom markets which provide OTT services, video streaming services in UHD, non-face-to-face business meetings, e-commerce, social networking, and gaming applications will continue to be growing.

Optical interconnection in data centers for Datacom and Telecom is a traditionally promising solution for high-speed data communications. According to market research report in 2022 by Yole Développement [1], a market research company, the market size of optical interconnect is expected to become larger and larger as shown in Fig. 1-1.

There are many types of optical interconnection applied in a data center network architecture. Fig.1-2 shows optical interconnects map for high-speed serial interface. DC-DC, intra-DC, server-server, module-module, chip-chip interconnects are being developed towards optimization in each different conditions.

In the DC, efficient interconnection is achieved through SERDES technology. A lot of low-speed parallel data are serialized into high-speed serial data and transmitted, then the transmitted high-speed serial data are converted back into a lot of low-speed parallel data. Because a large number of links can operate at high speed, the DC has advantages in terms of price by reducing data paths. Nevertheless, since the DC uses a massive parallelism high-speed link, it is reasonable to configure an appropriate optical interconnect according to the reach and purpose considering the total cost. As you can see in Fig.1-3, most of data traffic is within DC [2]. Optical interconnects based on multi-mode fiber (MMF) have been mainly developed as short reach targets up to 300 m. Among them, the optical interconnect based on a Vertical-Cavity Surface-Emitting Laser (VCSEL) which gets a wavelength of 850 nm has been positioned as an attractive solution in terms of cost-effectiveness. Especially, Multi-Mode(MM) VCSEL is the cheapest one. Since it is a type of semiconductor laser diode that can be produced in wafer level, VCSEL can be manufactured as a type of array and has advantages in cost. Additionally, it has relatively good beam quality and make it possible to configure low system size.

Standard of optical interconnects was defined as ‘P802.3ae’ for 10 Gb/s Ethernet over fiber by the Institute of Electrical and Electronics Engineers (IEEE) in 2002. Then it has evolved to 400 Gb/s over parallel multimode fiber as ‘P802.3cm’ which is a standard for 50 Gb/s per channel in 2020. Nowadays, ‘P802.3db’ was defined in 2022 for VCSEL-MMF links using 100 Gb/s (50 Gbaud PAM-4) signaling. Even though standards of optical links were evolved up to 100 Gb/s per lane, there are still many challenges as the optical transmitter in order to obtain both high-speed and optimized performances, such as low power dissipation, improved signal quality. Especially, as an amplitude-based modulation scheme such as PAM-4 is used for high-speed interconnections, the Signal-to-Noise Ratio(SNR) gets worse, so the importance of a well-designed VCSEL driver is growing.

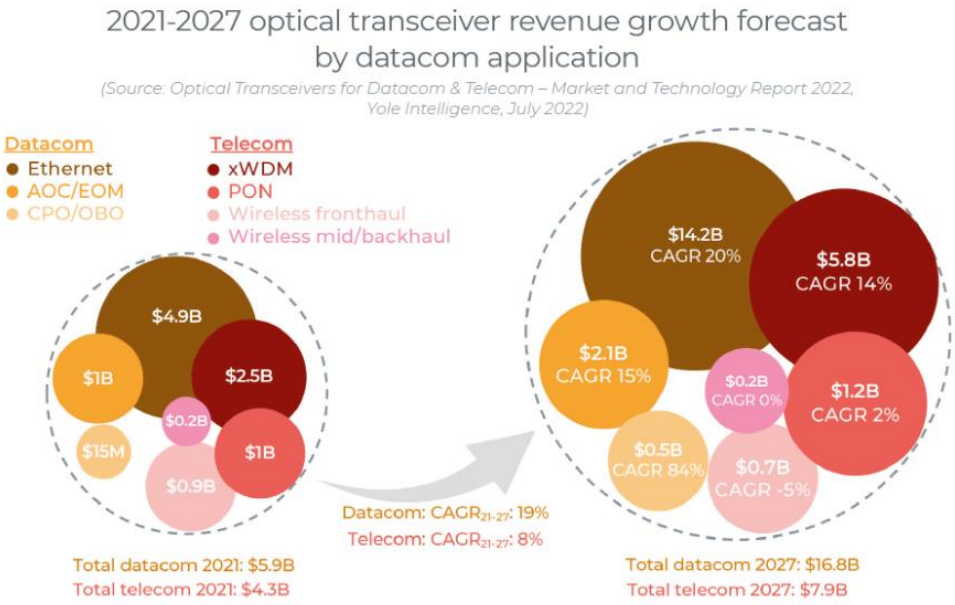


Fig. 1-1. 2021-2027 Market growth forecast of optical transceiver [1]

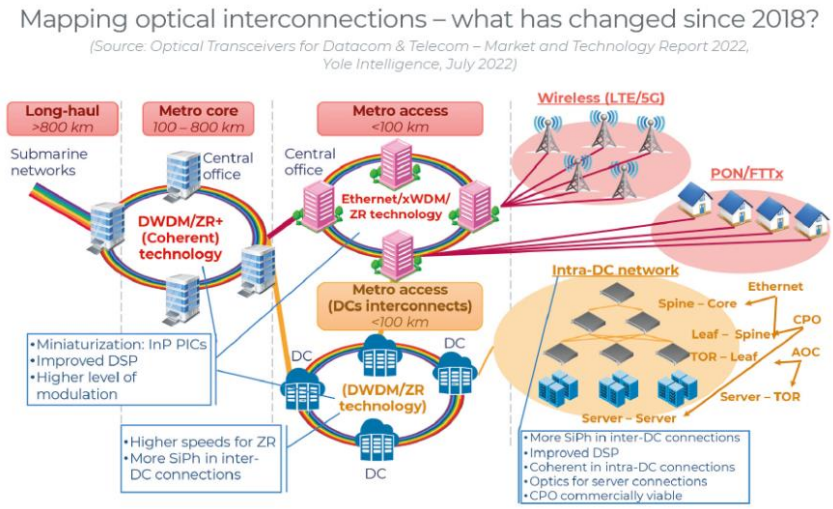


Fig. 1-2. High-speed interconnection map for Datacom & Telecom [1]

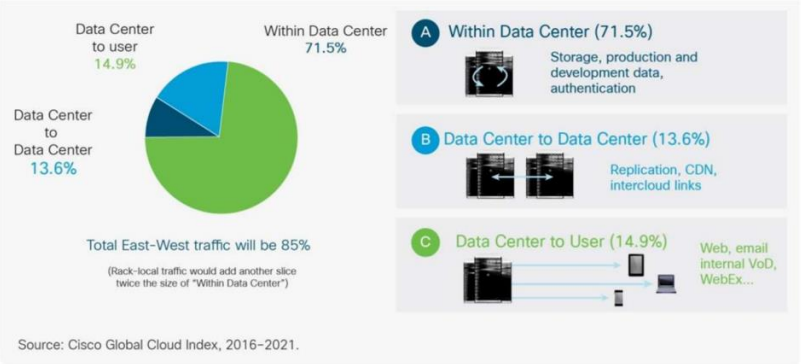


Fig. 1-3 Global data traffic distributions [2]

1.2 Data formats in the optical link

Fig. 1-4 shows two types of representative modulation in high-speed serial interfaces. In the early days, Non-Return-to-Zero(NRZ) signal modulation was popular considering channel frequency and complexity. There are only two levels that consist of ZEROs, ONEs. Therefore, NRZ has relatively low issues about signal processing compared to other signal modulation formats. These days, Pulse Amplitude Modulation level-4 (PAM-4) is preferred in this application for more high-speed interconnection. Because PAM-4 signals have 2-bit information within 1-Unit Interval (UI), Data-Rate(DR) is doubled compared to

NRZ modulation in the same optical channel.

PAM-4 signals have a strong advantage to jack up interconnection speeds, but it is three times more sensitive than NRZ in terms of EYE openings because level-to-level amplitude is become 1/3. Therefore, PAM-4 signaling should be more careful for high SNR even if it is a TX driver which drives large signal amplitude. Various noises, non-linearity, and power-hungry are major considerations. Even since there are non-linear properties that occur in the 850 nm multi-mode(MM) VCSEL, it is important to minimize problems which make SNR worse.

The modulation bandwidth of 850 nm VCSELs have been developed for high-speed optical interconnection and 32.4 GHz is the highest value reported so far in 2022 [3] as you can see Fig. 1-5. Considering the Nyquist frequency in TX driver, it can be confirmed that NRZ modulation can have a DR of 64.8 Gb/s and PAM-4 can have a DR of 129.6 Gb/s. Therefore, in order to satisfy 100 Gb/s per channel in short reach optical interconnect, VCSEL PAM-4 driving is an attractive signal modulation scheme considering the modulation bandwidth of existing VCSELs.

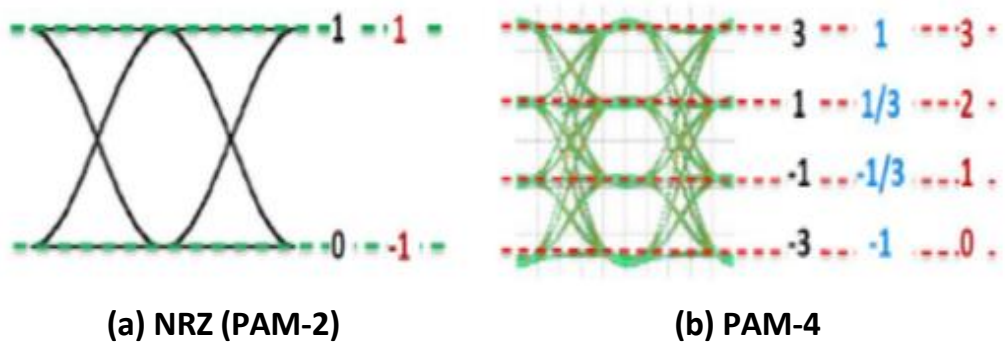


Fig. 1-4. Data formats in high-speed interconnections

(a) NRZ (PAM-2), (b) PAM-4

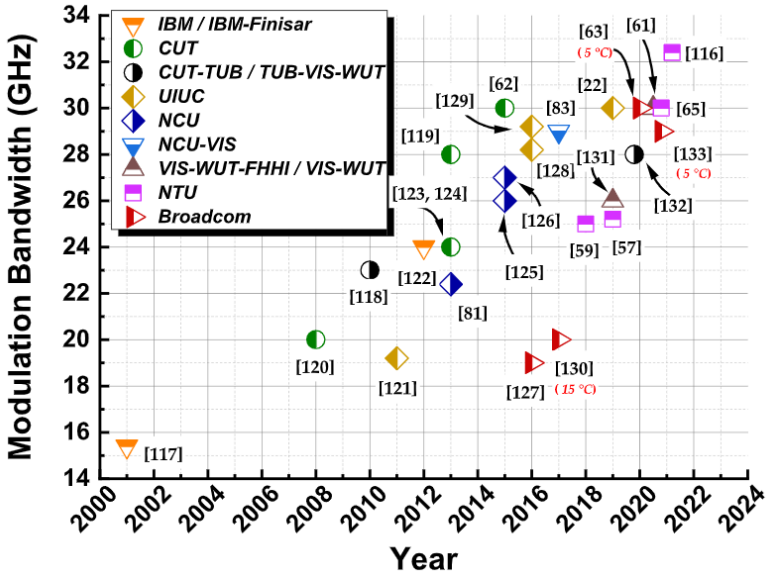


Fig. 1-5. VCSEL modulation bandwidth reports [3]

1.3 Research goals

VCSELs have advantages in modulation bandwidth, system size and cost, but have non-linear issues. When the VCSEL driver is designed, this issue results in EYE closure. Especially for high-order amplitude-based modulations such as PAM-4, it brings about lowering The Level Mismatch Ratio (RLM). Also, EYE degradation due to PAM-4 inner EYE skew which make it difficult to set a decision point at the Receiver. Therefore, VCSEL based optical transmitter have to be designed appropriately for mitigating optical properties causing eye closure for high SNR

Implementing an accurate commercial VCSEL model which has device characteristics, such as S_{11}, S_{21}, DC responses at various current conditions, is also important to optimize the Driver circuit. In most cases, VCSEL industries do not offer specific equivalent SPICE model to users. Therefore, one of the main research goals was to create a model accurately emulating the device characteristics of VCSEL based on S-parameter and DC measurement data. The VCSEL model was built up in Verilog-A language for compatibility with simulator.

Fig. 1-6 Shows a block diagram of high-speed serial interface with optical link. The optical transmitter is positioned at TX driver + VCSEL. There are two VCSEL Drivers proposed which were designed in 28-nm CMOS process and 14-nm FinFET process. Voltage-mode logic was used as a main topology for low power consumption and single-ended structure. Drivers have 50-ohm termination at input side for compatibility with TX Serializer or TX Retimer. An on-chip current source, which is a type of common-mode feedback (CMFB), was employed for sourcing bias current to VCSEL.

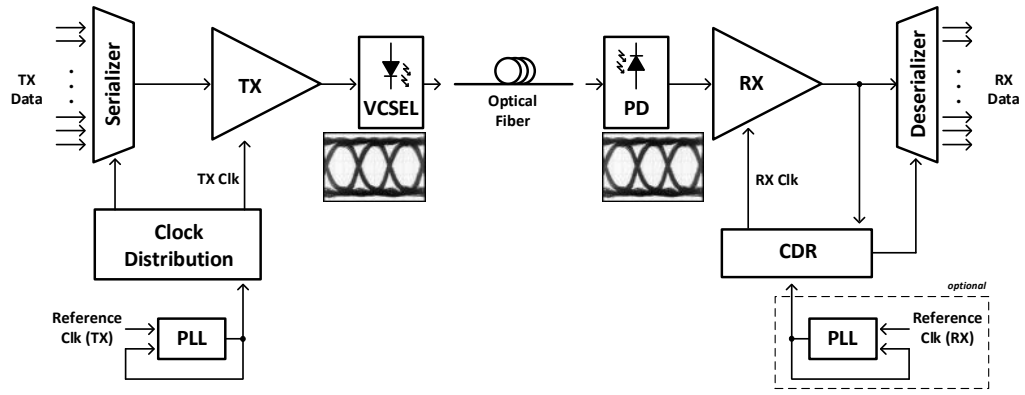


Fig. 1-6. Entire block diagram of SERDES with optical interconnection

The evaluation board design is also important part of this research. There is degradation in SNR due to wire-bond inductance which are generated from the packaging parasitic. evaluation board should be designed to mitigate packaging parasitic that cause Inter-Symbol-Interference(ISI), Supply Switching Noise(SSN) [4].

In this paper, research on NRZ, PAM-4 850 nm MM VCSEL driver will be described. The purpose of this research is designing VCSEL driver which has a low power consumption and high data rate. In order to achieve this research goal, theoretical analyze about electrical-to-electrical responses with packaging parasitic, and electrical-to-optical responses are organized. Additionally, VCSEL equivalent SPICE model, low power circuit architecture for VCSEL driving, and RLM controllable circuits for PAM-4 signaling will be introduced.

2. Background

2.1 Optical links based on Multi-mode VCSEL

It is important to select an optical device to be used for interconnection considering

appropriate performance and cost since optical interconnect accounts for a large portion in data centers. Due to the nature of the data center that uses massively parallelism in link, cost and performance of each optical devices should be compared reasonably for the total cost in DC. Fig. 2-1 shows data communication application space. These are parsed out by transmission reach, fiber type and loss budget for the optical link [5]. MM VCSEL, which has the advantage of high volume by enabling a wafer-level process like mature CMOS technology, is a popular optical device in short reach communications up to 300 m.

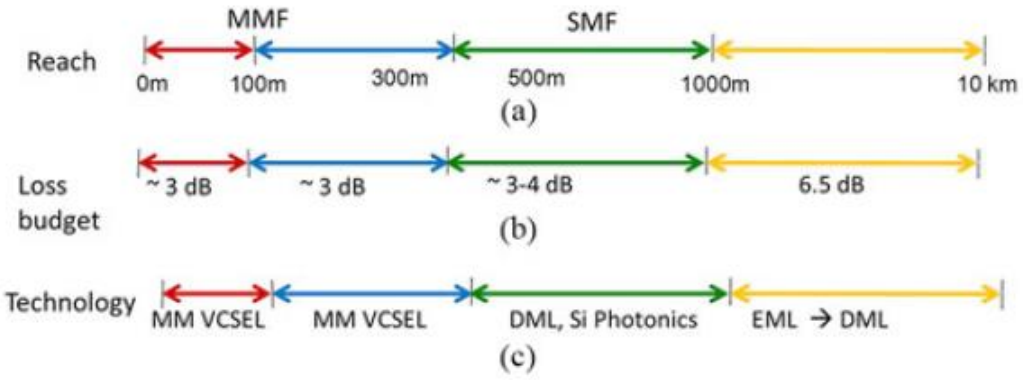


Fig. 2-1. Application space in data centers based on (a) transmission reach and fiber type, (b) loss budget, (c) technology [5]

VCSEL is a Direct Modulated Laser (DML) unlike Si Photonics, which is an Electro-absorption Modulator(EAM) and used as a type of Electro-absorption Modulated Laser (EML). Since VCSEL has a small size configuration which is composed of a single chip, it has the advantage of being able to configure whole system with a more compact design. In addition, the optical signal is modulated by the change of injection current, so it has a low power consumption compared to EML. DML based signal processing goes through the sequences of ONEs and ZEROs on the optical side which are operated by the modulated injection current. However, direct modulation changes laser properties such as refractive index by changes in the injection current, performance degradation may occur due to large chromatic dispersion at long-reach over 10 km.

VCSEL has a small active region and emit light in a perpendicular direction. Using two Distributed Bragg Reflector (DBR) mirrors, the cavity is minimized and the threshold gain is lowered. Because of these advantages, it can be a light source that can be turned on even at very low currents of several 0.x mA.

As shown in Fig. 2-2, VCSEL has an active region between two DBR mirrors, and each

type of DBR is connected to the contact on the top of the VCSEL die. DBR mirrors are preferred structure because of their advantage in the ease of monolithic fabrication. DBR pairs in the wavelength band of 850 nm to 980 nm are made of the Al_xGa_yAs series which are III-V compound semiconductors. DBR pairs in the 1300-1550 nm band are made by more complex compounds such as InP/AlGaInAs or InP/InGaAsP [3].

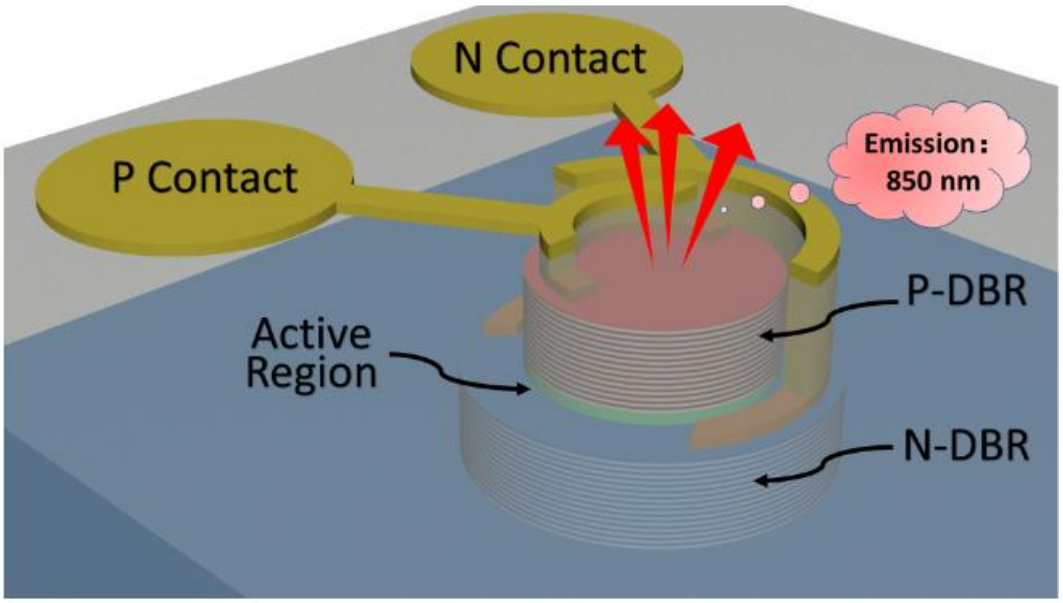


Fig. 2-2. Example of VCSEL structure [3]

There are several advantages and disadvantages when VCSEL is used as an optical device in the optical interconnection. The biggest advantage is that it is possible to produce large quantities with 2-D arrays because it is a semiconductor laser diode that can be manufactured in wafer-level processes. In addition, there are advantages for high-speed interconnects because VCSEL has high modulation bandwidth and relatively good beam quality. However, there are disadvantages that the output optical power is low due to small cavity. Since it has high thermal resistance and capacitance, it can be a challenge when designing VCSEL driver circuit. Additionally, non-linearity issue is also an important problem when driving VCSEL.

VCSEL has two non-linearities: static non-linearity and dynamic non-linearity. In PAM-4 signal processing, EYE degradation as shown in Fig. 2-3 can be confirmed as a result of including these characteristics. Static non-linearity, refers to a non-linear property in DC that occurs in the light-current (L-I) curve characteristic. The static non-linearity directly results in decreasing in RLM of PAM-4. Unlike NRZ, it is a critical issue because PAM-4 signal has four levels of data and linearity degradations lead to inner EYE opening

closure which means Bit-Error Rate (BER) degradation. The dynamic non-linearity represents that the s-parameter properties are changed by current flowing through VCSEL. Generally, VCSEL has properties that higher bandwidth at higher bias current and more peaking responses at low bias current [6]. EYE Skew issues between three inner EYEs of PAM-4 can be possible and data-dependent EYE degradation may occur because the bandwidth at a low current is lower than the bandwidth at a high current. These characteristics are fatal problems that result in low SNR. These problems have been compensated by some methods such as pre-emphasis [7] - [9], n-tap feedforward equalizer (FFE) [10] - [12], and asymmetric FFE [13] - [15]. However, equalization techniques for improved optical EYE opening accompany additional power consumption, so decision of employing equalization technique should be carefully decided considering energy efficiency and BER.

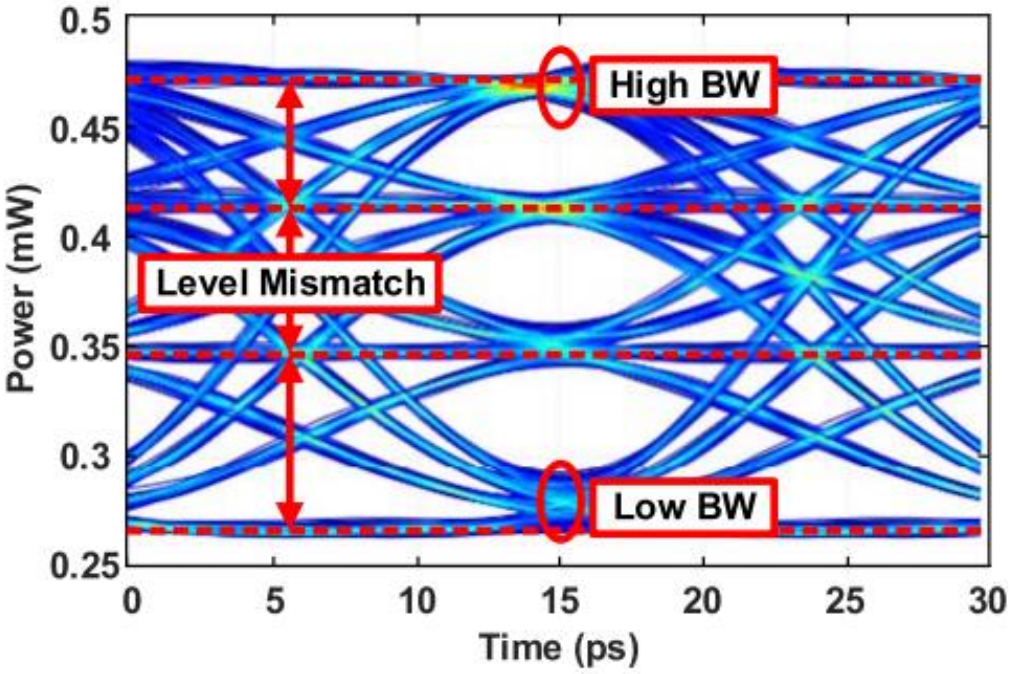


Fig. 2-3. Feature of Static and Dynamic non-linearity in EYE diagram [16]

2.2 Data transmission through VCSEL

Generally, electrical channels which made in copper have frequency dependent losses due to skin effect and dielectric losses. However, optical fiber has extremely low losses such as 0.2 dB losses per 1 km. In addition, MM VCSEL is used for short-reach optical interconnections (under 300 m) so it is not critical to modal dispersion. Therefore, the main

consideration is driving a VCSEL in suitable conditions for high-speed interconnection. Section 2.2 will deal with impedance properties and transfer function of VCSEL.

The VCSEL is a direct modulated laser which converts injected current to optical power. Therefore, data transmission process is operated by summation of static bias current (I_{bias}) and dynamic current swing (I_{mod}), which represents modulation current, injected into PN junction in VCSEL and it is converted into optical power by transfer function of VCSEL. As you can see in Equation (2.1) - (2.3), important elements to represent transfer function of VCSEL can be expressed as follows. VCSEL transfer function can be obtained from rate equation that has been organized by [6].

$$H_{\text{int}rinsic}(f) = \frac{P_{optical}(f)}{I_{junction}(f)} = A \cdot \frac{f_R^{\,2}}{f_R^{\,2} - f^2 + j(f/2\pi)\gamma} \tag{2.1}$$

$H_{intrinsic}(f)$ = VCSEL intrinsic Electrical-to-Optical transfer function

$I_{junction}(f)$ = Current through PN junction (active region) of VCSEL

$P_{optical}(f)$ = Output optical power which are emitted from the surface of VCSEL

$$f_R = D\sqrt{I_{VCSEL} - I_{th}} \tag{2.2}$$

$$\gamma = Kf_R^{\,2} + \gamma_0 \tag{2.3}$$

f_R = the resonance frequency

γ = damping factor

A, D, K = VCSEL design-specific parameters

As you can see in Equation (2.1), VCSEL intrinsic electrical-to-optical response consists of second-order transfer function. ‘A’, ‘D’, ‘K’ factors are design specific parameters. The f_R is the resonance frequency of VCSEL. Basically, f_R is proportional to square root of I_{VCSEL}-I_{th} (= I_{bias}+I_{mod}-I_{th}). The γ represents a damping factor that is proportional to I_{VCSEL}-I_{th} and square of f_R. Therefore, transfer functions of E-O conversion are various with injected current. Importantly, the closer the current is to I_{th}, the more pronounced the non-linearity caused by the VCSEL transfer function. As it was mentioned at Section 2.1, the dynamic non-linearity results in data dependent EYE degradation and various transfer functions of VCSEL E-O conversion are attributed to this characteristic.

There are more ringing and bandwidth degradation at low bias current. However, VCSEL driver is preferred setting low static I_{bias} to reduce total power consumption. For these reasons, there are certain challenges to design optimized low power system in the VCSEL based optical transmitter. Although commercial VCSELs have been developed aiming high data rate and have various VCSEL properties due to material properties, a non-linear 2^{nd}-order transfer function can be applied. Therefore, it is a common problem to be considered in terms of optimization of optical transmitter no matter which VCSEL having any modulation bandwidth is used. Considering typical modulation bandwidth of a VCSEL, using a low bias current is efficient in terms of power consumption when operating at a low-speed, and operating at a high bias current is advantageous in terms of bandwidth when high-speed mode.

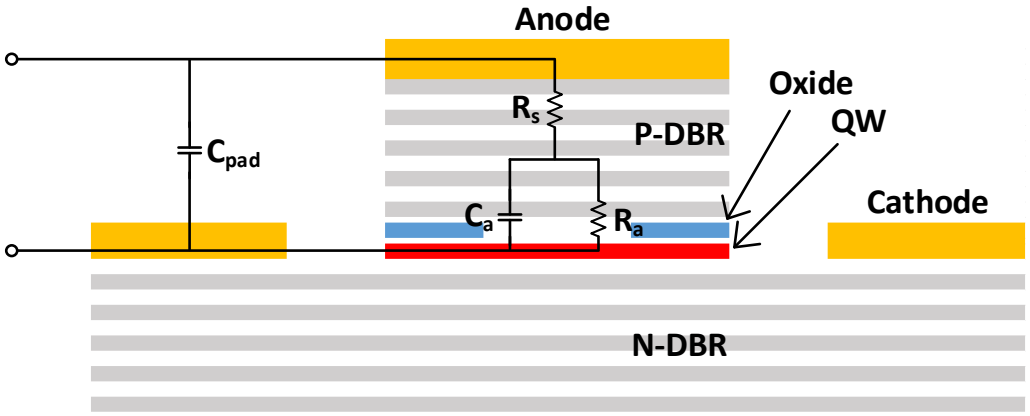


Fig. 2-4. VCSEL Electrical elements: 2nd-order equivalent model

Fig. 2-4 shows 2nd-order equivalent model overview of VCSEL that consists of four elements. This circuit model is commonly used for representing VCSEL input impedance [17], [18]. VCSEL major elements can be represented as PAD capacitance (C_{pad}) and series resistance (R_s) from contact to active region, active capacitance (C_a) and active resistance (R_a) in active region. S_{11} properties of VCSEL varies according to current injections because C_a and R_a values are changed by injected current. Therefore, various S_{11} of VCSEL at each current are used as a Tx Driver load. Values of each circuit elements are calculated by measurement data of S_{11} at various bias current conditions. Also, these are used to design electrical part of VCSEL equivalent SPICE model.

2.3 Driver environments with VCSEL load

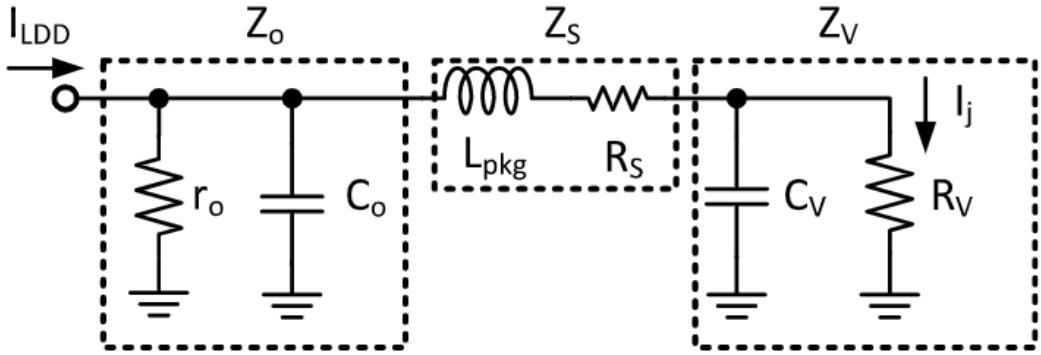


Fig. 2-5. Block diagram of Driver to VCSEL electrical network [19]

Z_O = Output impedance of VCSEL Driver

Z_S = Packaging bond-wire inductance and VCSEL series resistance

Z_V = Parallel capacitance and resistance of VCSEL 1st-order equivalent model

Fig. 2-5 shows overall conceptual current driving network for the transfer function of input laser diode driver current (I_{LDD}) to output junction current (I_j). The simple impedance model of VCSEL consists of 4 elements (C_{pad}, R_s, C_a, R_a) as a 2nd-order model. This electrical model can be simplified into the first-order model because typically $C_{pad} < C_a$ and $R_s << R_a$. Therefore, the entire system can be interpreted as a 3rd-order system shown in equation (2.4) [19].

$$H_{electrical}(s) = \frac{I_{junction}(s)}{I_{LDD}(s)}$$
$$= \frac{Z_o Z_V}{Z_o + Z_S + Z_V} \cdot \frac{1}{R_V} \tag{2.4}$$
$$= \frac{r_o / (r_o + R_V)}{1 + s(r_{||}(C_o + C_V) + \frac{L_{pkg}}{r_o + R_V}) + s^2 \frac{L_{pkg}(\tau_o + \tau_V)}{r_o + R_V} + s^3 L_{pkg} r_{||} C_o C_V}$$

$$\tau_o = r_o C_o \tag{2.5}$$

$$\tau_V = R_V C_V \tag{2.6}$$

$$r_{||} = r_o R_V / (r_o + R_V) \tag{2.7}$$

$$\omega_{real} \approx \frac{1}{r_{||}(C_o + C_V)} \tag{2.8}$$

$$\omega_{LC} \approx \sqrt{\frac{C_o + C_V}{L_{pkg} C_o C_V}} \tag{2.9}$$

If $R_s = 0$, there are one real pole and two complex conjugate poles. Equation (2.8) shows an approximated real pole. It is important to know that the real pole is independent of the packaging bond-wire inductance. Unlike the real pole, the resonance frequency of

complex poles shown in equation (2.9) is strongly dependent on packaging inductance. If $0 < R_s < R_V$, it decreases Q factor of resonance poles. Unfortunately, L_{pkg} is difficult to use as a design parameter. Therefore, VCSEL Driver designer has to optimize electrical-electrical signaling by using appropriate output impedance of Driver. For that reason, output resistance of Driver is preferred to be optional which can be controlled by I^2C.

VCSEL has structure of two ports which are Anode contact and Cathode contact. Therefore, various driving methods have been tried for the necessary purpose. Typically, three types of methods to drive VCSEL have been reported, such as Anode driving (Common cathode) [8], [20], Cathode driving (Common anode) [21], [22], and Differential push-pull driving [4]. There are many kinds of commercial VCSEL in the markets. Even if each characteristic is different, a constant forward bias voltage must be applied to both ends making VCSEL turn-on state. The processes using high voltage used common cathode method applying ground to the cathode. However, as the process scaled down, the driving voltage of the MOSFET was lowered, which caused voltage headroom issues. Therefore, there were popular to use both high-voltage and low-voltage supply or adopting bias-tee

topology by using an on-chip AC coupling cap and applying external VCSEL bias voltage [4], [19]. Nevertheless, Supply Switching Noise(SSN) issue is critical and on-chip ac coupling capacitors generate large amounts of parasitic capacitance, which is not suitable for high-speed applications. For these reasons, recently, the method of applying negative bias voltage to the VCSEL cathode and implementing dc-coupled anode driving has been preferred [11], [12]. Therefore, packaging the Driver with VCSEL in consideration of SSN and ground bounce has become more important issues which have to be mitigated. The wire-bonding inductances (L_{pkg}), which connect the Cathode contact of VCSEL die and port of Evaluation Board (EVB) for negative voltage source, are known to create data dependent SSN and ISI [4]. This is a more fatal problem in PAM-4 signaling which is more sensitive to EYE opening. So, it is essential employing on-chip decoupling capacitors to mitigate unwanted inductance.

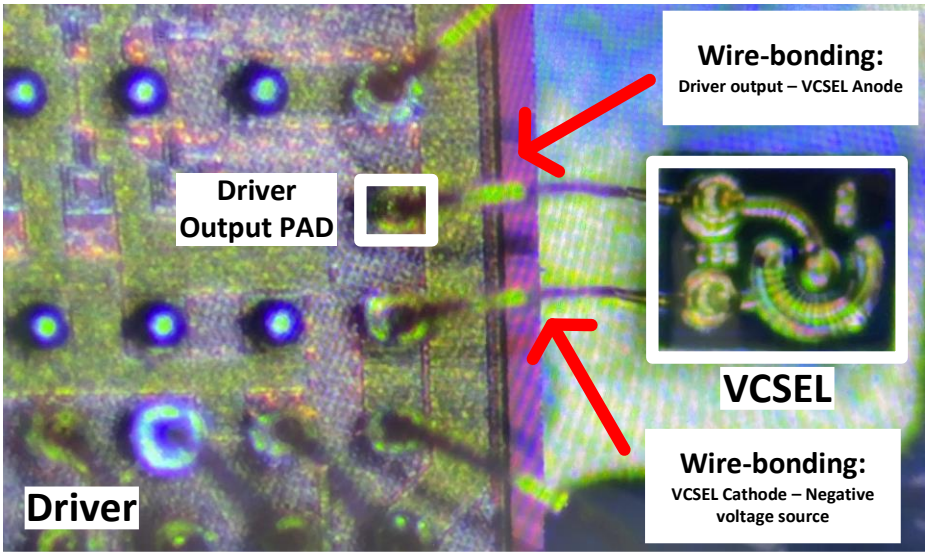


Fig. 2-6. Figure of packaging parasitic example

In order to have an optimum driver bandwidth, it is efficient to get an equalizing effect from appropriate L_{pkg}. However, since the value of L_{pkg} is typically outside of control, it is more important to find optimum bandwidth point by adjusting the value of other parameters with predetermined L_{pkg}. The low output resistance (r_o) of the driver has the effect of increasing the real pole frequency and lowering the Q-factor of the complex pole, but if the value itself is too low, the modulation current flowing into the VCSEL decreases. Therefore, it is considered an optimal value to lower the value of r_o to have enough BW according to the target data rate.

3. VCSEL equivalent SPICE model

3.1 VCSEL model design

Before designing VCSEL driver, VCSEL equivalent SPICE model is needed as a load for circuits optimization. It is common for VCSEL model to build-up an impedance model that includes rate equation (E-O conversion) through Verilog-A language for SPICE simulation with circuits. It is possible to model parameters of VCSEL rate equation, but since it is the 2nd-order system, it can be possible to make a model with variable passive elements, such as current dependent resistors, inductors, and capacitors. Fig. 3-1 shows a circuit that presents the impedance model and rate equation of VCSEL.

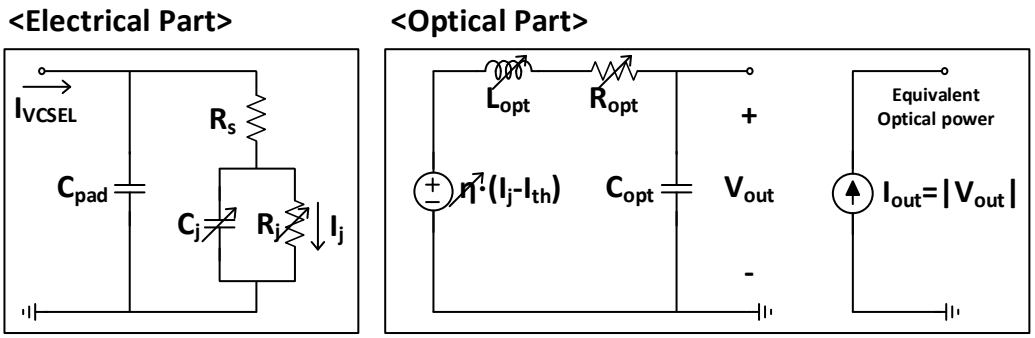


Fig. 3-1. Circuit of VCSEL equivalent SPICE model

3.2 Verilog-A based SPICE model

The s-parameter data of the commercial VCSEL was measured by Lightwave Component Analyzer (LCA) equipment. Fig. 3-2 shows a block diagram of test bench set-up for measuring s-parameter of commercial VCSEL. The data used in modeling are S_{11} and S_{21} responses at various bias current values. Fitting variables for each bias current were carried out as shown in Equation (3.2). Additionally, DC data, which represents L-I-V curve, was extracted by measurement setup as you can see in Fig. 3-3. VCSEL input forward bias voltage was swept by Semiconductor Parameter Analyzer and VCSEL output

optical power was extracted by lensed fiber and Optical Power Meter.

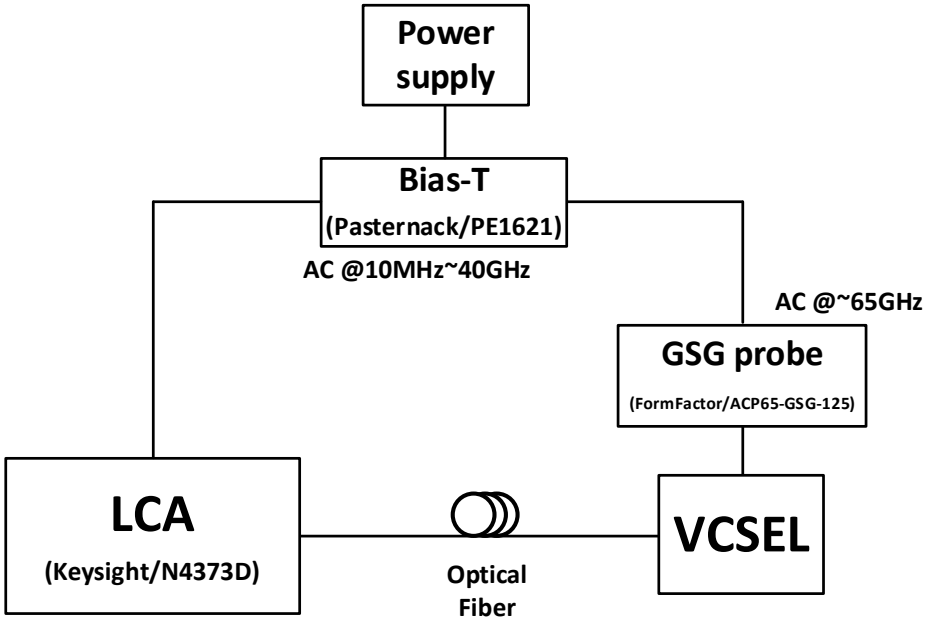


Fig. 3-2. VCSEL s-parameter measurement set-up

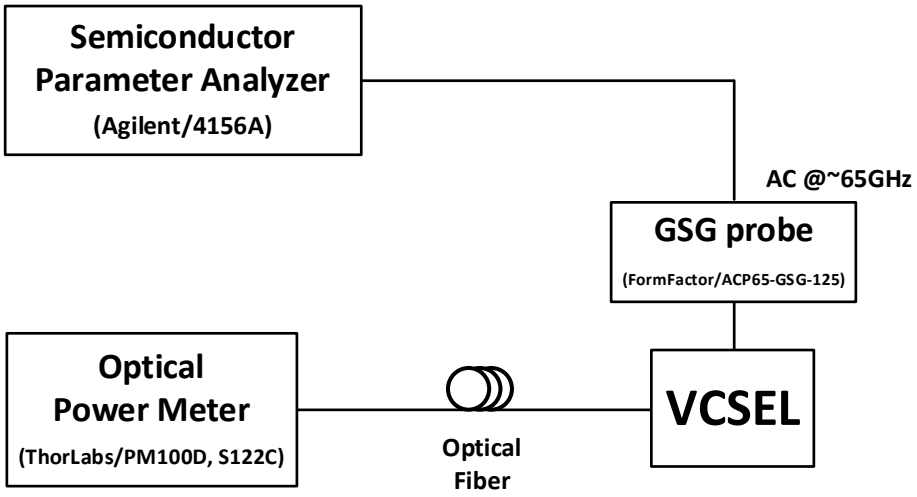


Fig. 3-3. VCSEL DC measurement setup

VCSEL equivalent SPICE model consists of two main parts. The first part is impedance modeling of VCSEL which represents electrical characteristics of VCSEL. Impedance of electrical part provides the loading effect of VCSEL during simulation. Values of C_j, R_j elements are changed according to current through VCSEL in active region. The result of comparing measured S_{11} data with the fitted model can be confirmed as Fig. 3-4 (a). The second part is modeling VCSEL rate equation, which represents E-O responses. Current-Controlled Voltage Source (CCVS) was employed to have values which are multiplied operating current (I_j-I_{th}) and slope efficiency (η). Basically, E-O response is 2^{nd}-order

transfer function and there is an equivalent system as you can see in equation (3.1). L_{opt} and R_{opt} values were set as variables for I_j to fit S_{21} response for each operating current. Fig. 3-4 (b) shows well matched results of S_{21}. L-I-V curve, which represents DC characteristic, was fitted in consideration of compatible with other fitting operations. I-V curve is based on VCSEL resistance that is series resistance of R_s and R_j. Also, current to light conversion is based on measured L-I curve data and it is applied by a variable for slope efficiency (η). Fig. 3-5 shows accurate fitted result of L-I-V curve.

There are five elements based on variables which are R_j, C_j, η, L_{opt}, R_{opt}. They are fitted by 4th-order polynomials as you can see in equation (3.2). The functions, which determine value of each parameter, are designed to reduce the amount of computation for time-domain simulation by not using very high-order polynomials. Polynomial fitting results can be identified as Fig. 3-6, Fig. 3-7.

$$\frac{I_{out}}{\eta \cdot \left(I_j - I_{th} \right)} = \frac{1}{L_{opt} C_{opt} \cdot s^2 + R_{opt} C_{opt} \cdot s + 1} \tag{3.1}$$

$$f(x) = a_4 x^4 + a_3 x^3 + a_2 x^2 + a_1 x^1 + a_0, \; x = I_j, \; I_{opt} \tag{3.2}$$

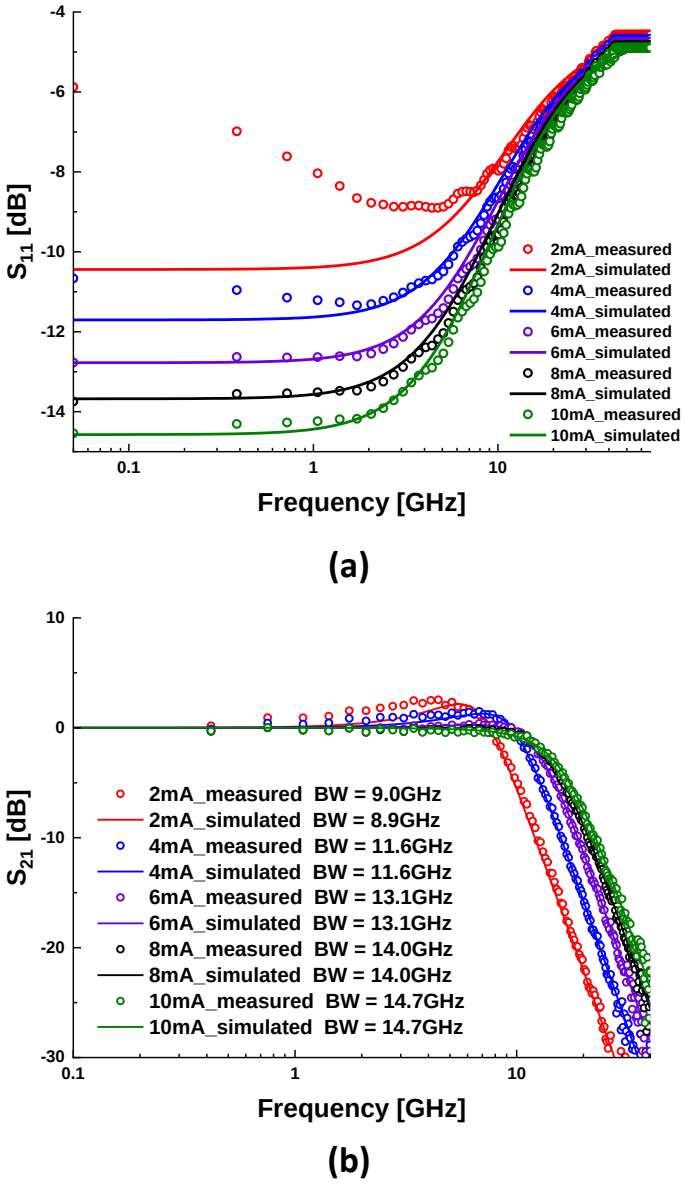


Fig. 3-4. VCSEL SPICE model fitting results of (a) $S_{11,}$ (b) S_{21}

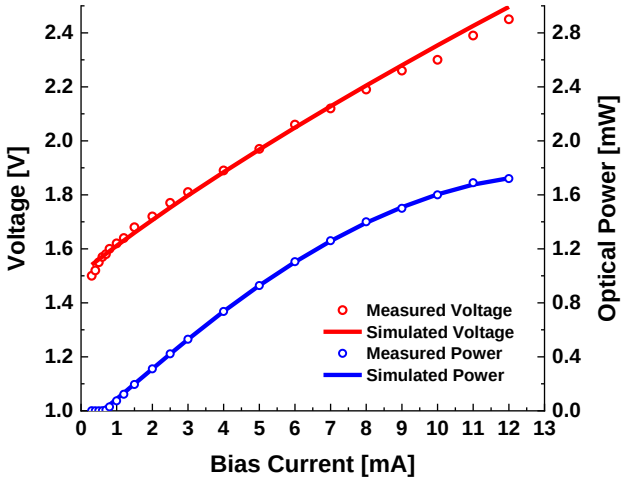


Fig. 3-5. L-I-V curve of VCSEL: comparison about measured results and simulation results

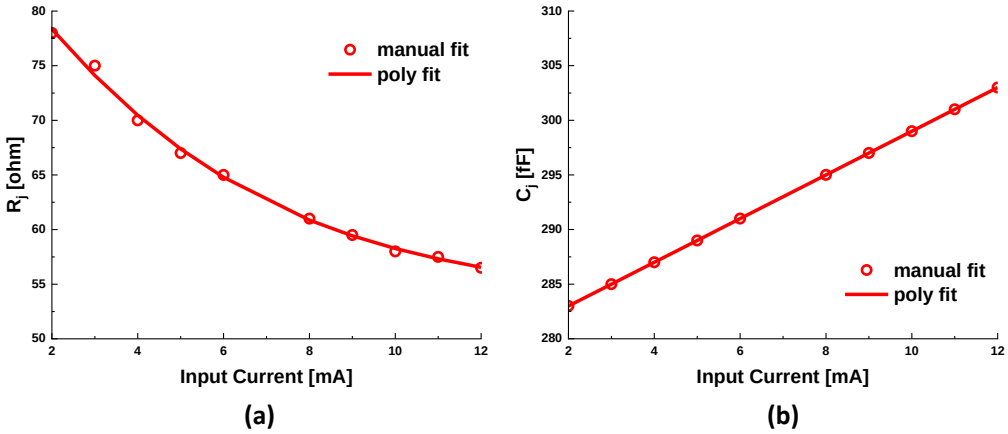


Fig. 3-6. 4th-order polynomial fitting based on input junction current (I_j) of (a) junction resistance, (b) junction capacitance

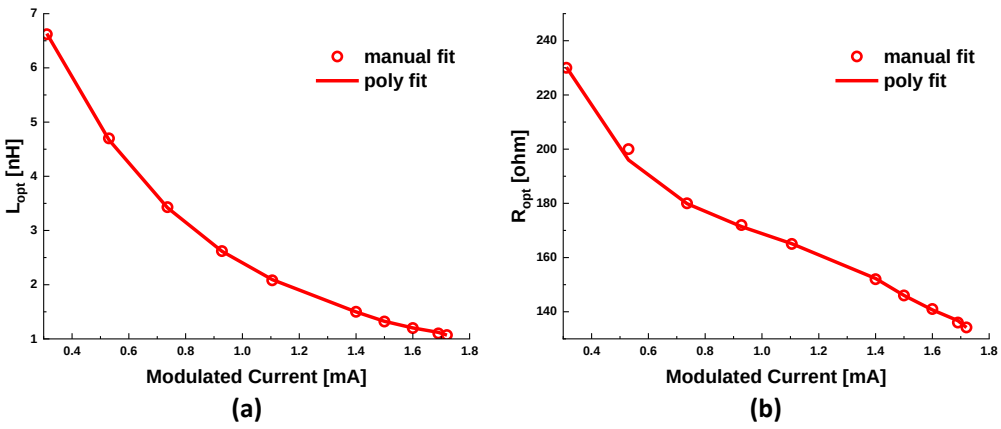
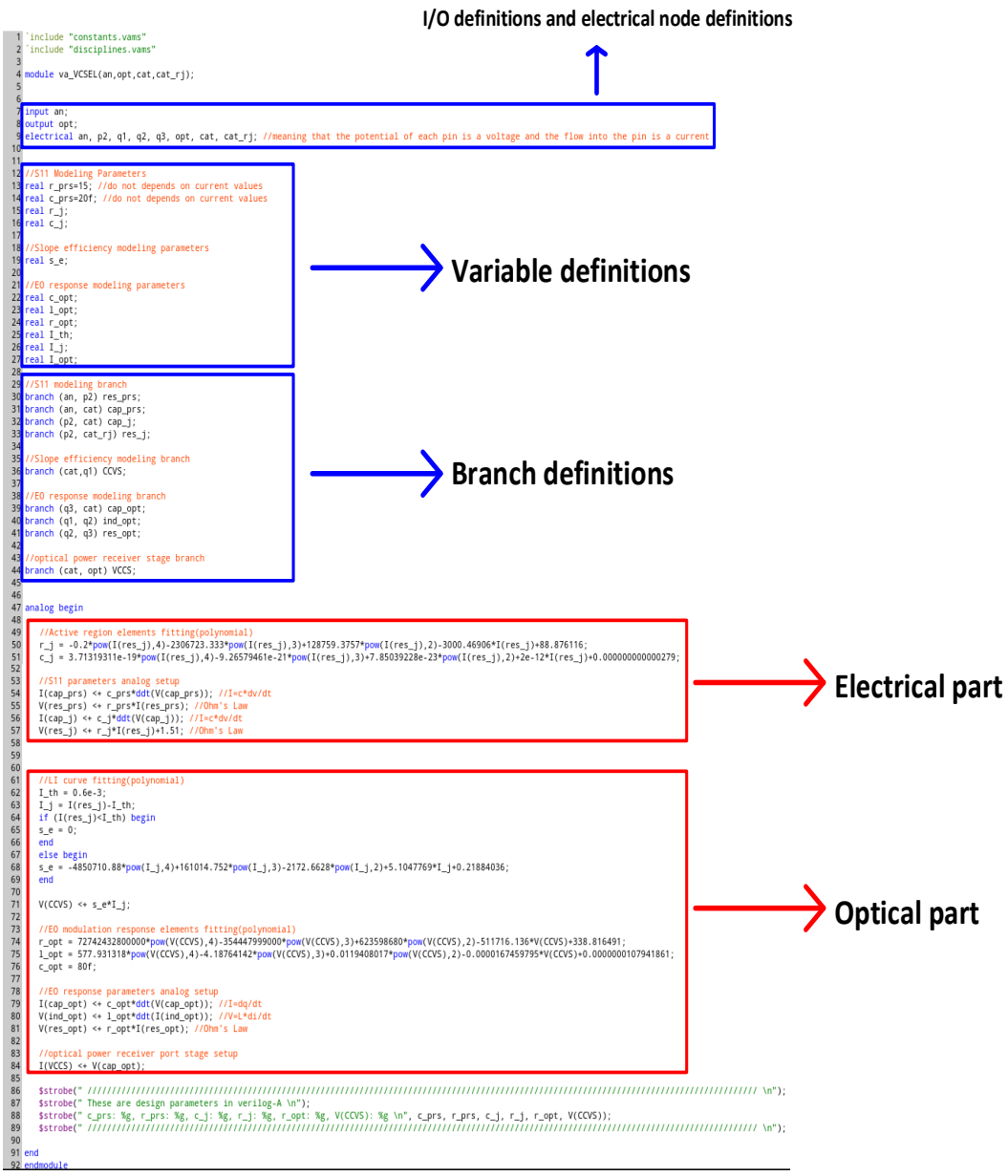


Fig. 3-7. 4th-order polynomial fitting for optical elements.

(a) inductance, (b) resistance

Basically, analog properties in Verilog-A language is operated by Ohm's law. All electrical elements are needed definition that represents electrical responses. Also, if you want to create custom analog elements, such as passive elements based on variable, a node-to-node electrical definition has to be multiplied with the custom function. Verilog-A based VCSEL equivalent model can be confirmed as Fig. 3-8. It is used for small signal and large signal simulation with VCSEL driver. It is accessible and easy to check electrical characteristics because it can call an instance in the form of a symbol. The values

corresponding to junction current and optical power are mainly checked from the model. This type of modeling technique has the advantage that it can be easily applied in the same way even if other commercial VCSEL devices are used.




```
`include "constants.vams"
`include "disciplines.vams"

module va_VCSEL(an,opt,cat,cat_rj);


input an;
output opt;
electrical an, p2, q1, q2, q3, opt, cat, cat_rj; //meaning that the potential of each pin is a voltage and the flow into the pin is a current


//S11 Modeling Parameters
real r_prs=15; //do not depends on current values
real c_prs=20f; //do not depends on current values
real r_j;
real c_j;

//Slope efficiency modeling parameters
real s_e;

//EO response modeling parameters
real c_opt;
real l_opt;
real r_opt;
real I_th;
real I_j;
real I_opt;

//S11 modeling branch
branch (an, p2) res_prs;
branch (an, cat) cap_prs;
branch (p2, cat) cap_j;
branch (p2, cat_rj) res_j;

//Slope efficiency modeling branch
branch (cat,q1) CCVS;

//EO response modeling branch
branch (q3, cat) cap_opt;
branch (q1, q2) ind_opt;
branch (q2, q3) res_opt;

//optical power receiver stage branch
branch (cat, opt) VCCS;


analog begin

  //Active region elements fitting(polynomial)
  r_j = -0.2*pow(I(res_j),4)-2306723.333*pow(I(res_j),3)+128759.3757*pow(I(res_j),2)-3000.46906*I(res_j)+88.876116;
  c_j = 3.71319311e-19*pow(I(res_j),4)-9.26579461e-21*pow(I(res_j),3)+7.85039228e-23*pow(I(res_j),2)+2e-12*I(res_j)+0.000000000000279;

  //S11 parameters analog setup
  I(cap_prs) <+ c_prs*ddt(V(cap_prs)); //I=c*dv/dt
  V(res_prs) <+ r_prs*I(res_prs); //Ohm's Law
  I(cap_j) <+ c_j*ddt(V(cap_j)); //I=c*dv/dt
  V(res_j) <+ r_j*I(res_j)+1.51; //Ohm's Law


  //LI curve fitting(polynomial)
  I_th = 0.6e-3;
  I_j = I(res_j)-I_th;
  if (I(res_j)<I_th) begin
  s_e = 0;
  end
  else begin
  s_e = -4850710.88*pow(I_j,4)+161014.752*pow(I_j,3)-2172.6628*pow(I_j,2)+5.1047769*I_j+0.21884036;
  end

  V(CCVS) <+ s_e*I_j;

  //EO modulation response elements fitting(polynomial)
  r_opt = 72742432800000*pow(V(CCVS),4)-354447999000*pow(V(CCVS),3)+623598680*pow(V(CCVS),2)-511716.136*V(CCVS)+338.816491;
  l_opt = 577.931318*pow(V(CCVS),4)-4.18764142*pow(V(CCVS),3)+0.0119408017*pow(V(CCVS),2)-0.0000167459795*V(CCVS)+0.0000000107941861;
  c_opt = 80f;

  //EO response parameters analog setup
  I(cap_opt) <+ c_opt*ddt(V(cap_opt)); //I=dq/dt
  V(ind_opt) <+ l_opt*ddt(I(ind_opt)); //V=L*di/dt
  V(res_opt) <+ r_opt*I(res_opt); //Ohm's Law

  //optical power receiver port stage setup
  I(VCCS) <+ V(cap_opt);

   $strobe(" ////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////// \n");
   $strobe(" These are design parameters in verilog-A \n");
   $strobe(" c_prs: %g, r_prs: %g, c_j: %g, r_j: %g, r_opt: %g, V(CCVS): %g \n", c_prs, r_prs, c_j, r_j, r_opt, V(CCVS));
   $strobe(" ////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////////// \n");

end
endmodule
```

Fig. 3-8. Verilog-A based VCSEL equivalent SPICE model

4. Systems and Circuits design

4.1 Driver topology

Fig. 4-1 shows two types of VCSEL driver topology. Generally, VCSEL drivers have been studied using the Current Mode Logic (CML) [7] - [11], [13] – [15]. In the case of using CM topology, it has more benefits in bandwidth than Voltage Mode Logic(VML). CML with differential push-pull driving has an advantage in speed because the loading effect of the pre-driver is relatively reduced. Additionally, it is an obvious advantage that the modulation current and driver output impedance can be adjusted independently. However, since VCSEL driver has to be single-ended output, dummy load should be employed at the another side of CML driver output as a VCSEL equivalent load. VCSEL have various impedances depending on junction current so it is difficult to create an accurate equivalent dummy with a passive element which has a specific value. This constraint results in poor compatibility with various commercial VCSELs. Secondly, there is a disadvantage that it cannot be power efficient because it consumes half of total power

on the dummy load. In contrast to CML, inverter-type VML driver is relatively power efficient and there is no additional power consumption on dummy load. There are challenges in bandwidth and it is burdensome from a driver optimization point of view that output impedance and modulation current are dependent.

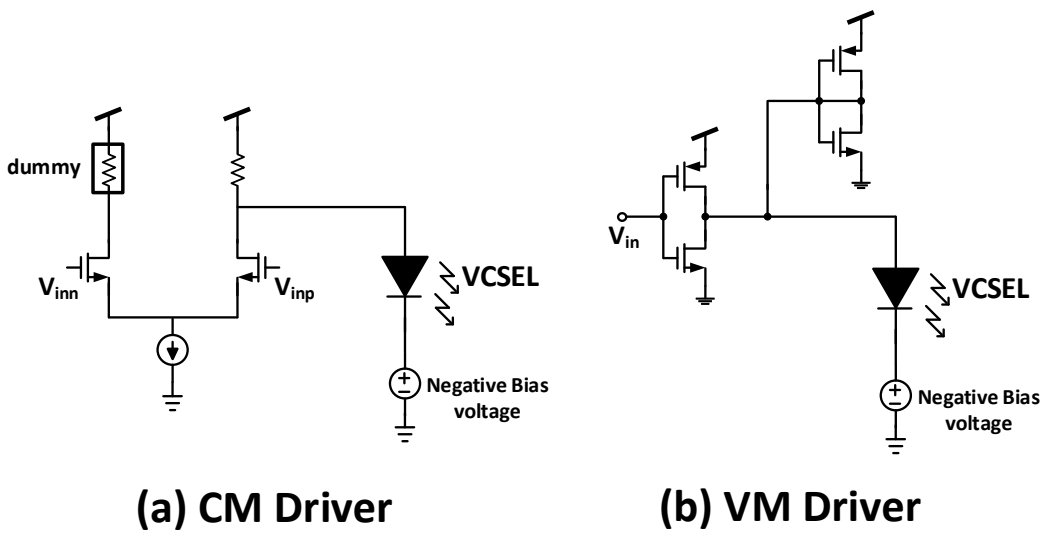


Fig. 4-1. Two types of VCSEL driver (a) CML driver, (b) VML driver

4.1.1 Inverter-type g_m/g_m amplifiers

Among various inverter-type amplifiers, g_m/g_m amplifiers are reported to have a small Total Harmonic Distortion (THD) and simple implementation for controlling gain, output impedance [23]. Fig. 4-2 and Fig. 4-3 show the results of comparing THD of various inverter-type amplifiers. The g_m/g_m amplifiers are widely used to design low noise inverter-type TIA in optical receiver, but it can be used in Laser Diode Driver (LDD) as a low THD topology for driving PAM-4 signals. Additionally, output impedance can be easily controlled by adjusting one over g_m cells.

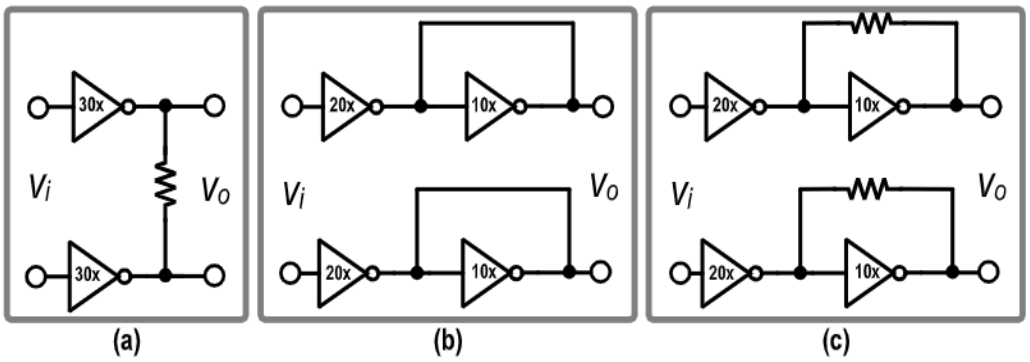


Fig. 4-2. Various Inverter-type amplifiers

(a) Resistive load, (b) g_m/g_m, and (c) TAS-TIS [23]

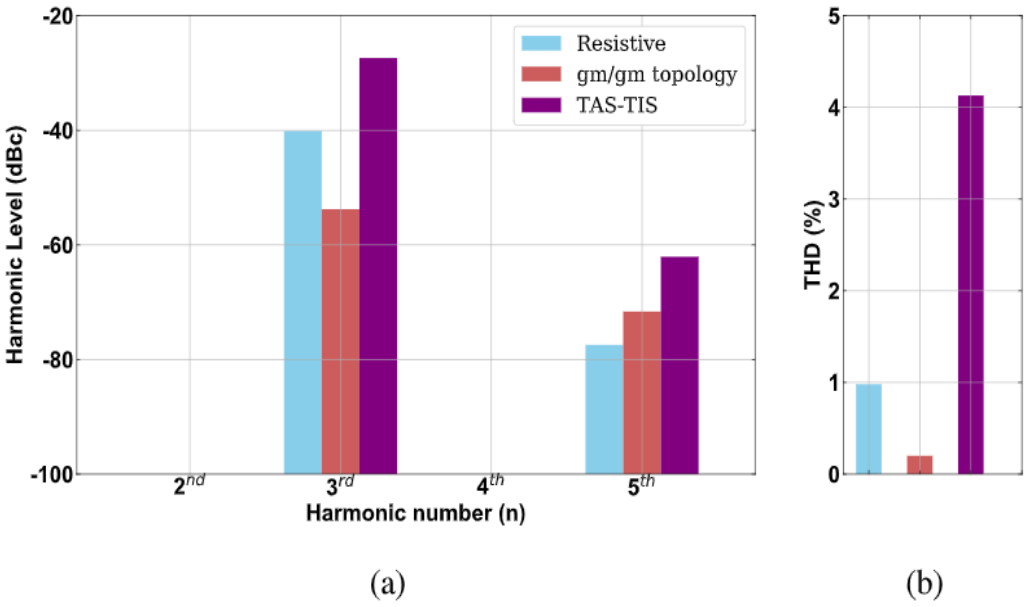


Fig. 4-3. THD comparison about three types of amplifier [23]

If there is a low wire-bond inductance, which connects Driver output PAD and VCSEL contact, electrical network of Driver to VCSEL is dominated by real pole in 3rd - order system (According to what was discussed in Section 2). In this regard, output resistance of inverter-type g_m/g_m amplifiers structure can be easily adjusted by selecting multiple slices of driver output $1/g_m$ cells through controlling I^2C. Also, adjustment of the driver's load can be seen as essential in terms of compatible for various VCSEL.

4.1.2 Shunt peaking technique

As Equation (4.1) shows, the transfer function of a g_m/g_m amplifier is determined by multiplying the transconductance of the inverter and the load impedance. Shunt peaking is one of the bandwidth boosting techniques that can be applied to inverter type g_m/g_m amplifiers. Fig. 4-4 show structures of g_m/g_m amplifier with shunt peaking is applied. It can serve as Continuous-Time Linear Equalization(CTLE) in voltage mode type topology. Basically, CTLE in this structure is operated by inserting a zero term into the load. Fig. 4-4 (a) shows a shunt peaking structure with a passive inductor. As you can see in an Equation (4.2), it consists of 2 zero and 1 pole impedance system when a passive inductor was employed. Although this approach has strong advantages from a CTLE designing point of view, the on-chip spiral inductors occupies a large area so there are restrictions on using multiple inductors. Fig. 4-4 (b) is a structure using a shunt peaking impedance which consists of 1 zero and 1 pole, and it has a benefit on area because it does not need large area for equalization. Equation (4.3) shows an equivalent shunt peaking impedance.

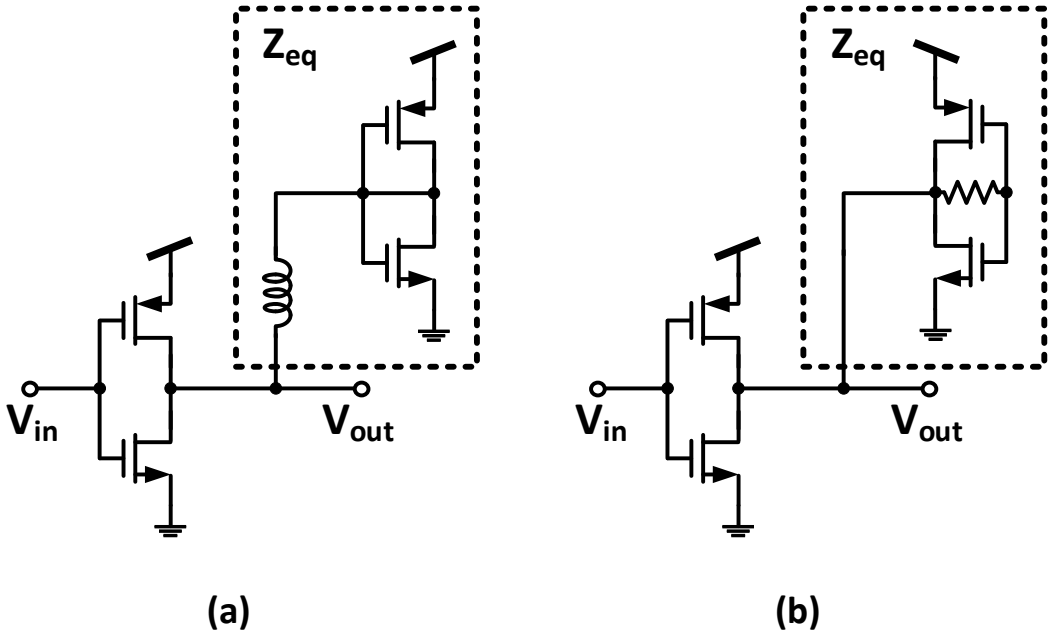


Fig. 4-4. Shunt peaking equalization in g_m/g_m amplifiers using

(a) passive inductor, (b) shunt peaking impedance

$$A = \frac{V_{out}}{V_{in}} = G_m \cdot Z_{eq} \tag{4.1}$$

$$Z_{eq} = \frac{1}{g_m} \cdot \left(\frac{1 + sg_m L + s^2 LC_{gs}}{1 + s\,{}^{1}\!/_{g_m} C_{gs}}\right) \tag{4.2}$$

$$Z_{eq} = \frac{1}{g_m} \cdot \frac{(1 + sRC_{gs})}{(1 + s\,{}^{1}\!/_{g_m} C_{gs})} \tag{4.3}$$

Considering the design area, VCSEL driver was designed by adopting a structure using a passive inductor. The Self Resonance Frequency (SRF) of the inductor was designed to be located at more than twice the Nyquist frequency in consideration of the target data rate. High frequency boosting is designed not to exceed 1.5 dB in the frequency domain. This is because having excessive high frequency boosting shows ringing in a large signal and hinders EYE opening by generating a group delay issues.

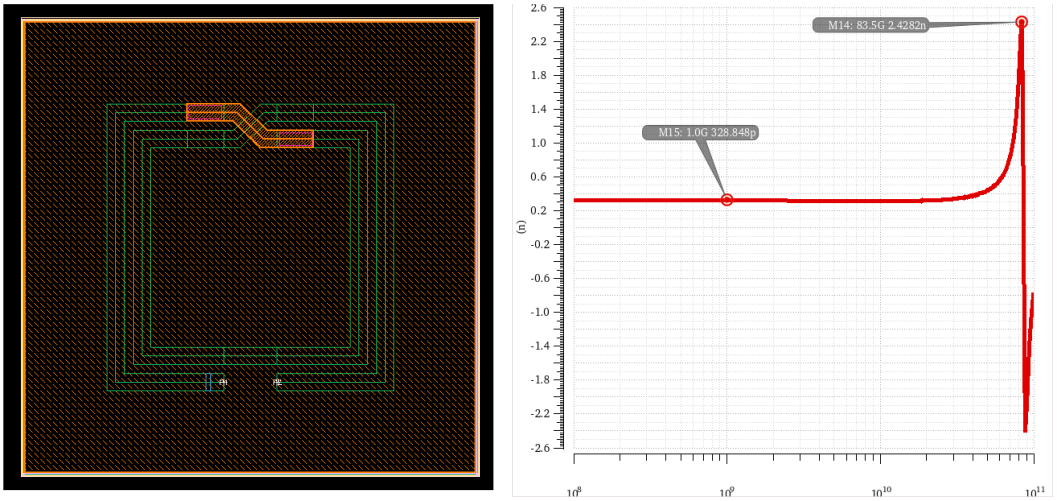


Fig. 4-5. Example of an on-chip spiral inductor

(a) inductor layout, (b) inductance simulation

4.1.3 Common-mode feedback

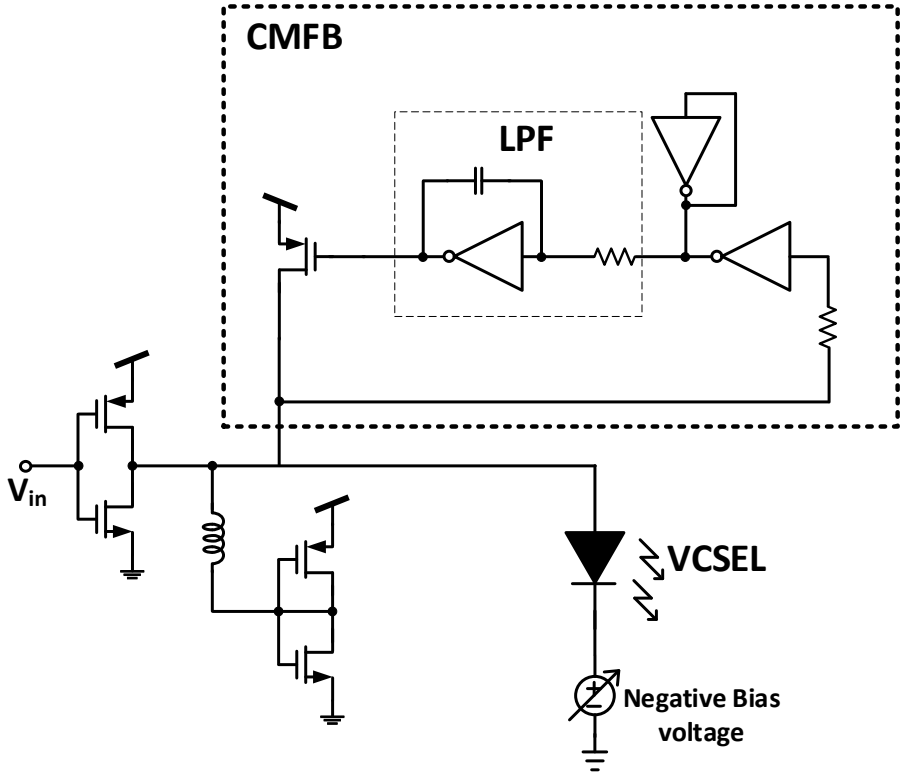


Fig. 4-6. The Block diagram of Common-mode feedback circuit

To drive the VCSEL for high-speed optical interconnect, a stable bias current must be sourced. At the same time, in order for VM driver to operate linearly, the output DC voltage must be applied to half of the VDD. The common-mode feedback(CMFB) architecture was

used to satisfy these two conditions. It is a negative feedback structure and plays a role in holding output DC voltage to VDD/2 even when various negative bias voltages are applied to cathode of VCSEL. There is an inverter type low-pass filter in which a resistor and a capacitor are employed in the loop. Also, a g_m/g_m amplifier was used to control the loop gain. The phase margin is designed to exceed 70 degrees for stability, and it has a loop gain equivalent to this. Detailed simulation results will be covered in Sections 4.2.

4.2 Inverter-type VCSEL CMOS Driver

4.2.1 Proposed architecture

Fig. 4-7 shows a block diagram of proposed VCSEL driver. Architecture is based on g_m/g_m structure and shunt peaking technique using the inductor. Degenerated PMOS and NMOS switch were used in order to control strength of g_m at each block as Fig. 4-8 (b). I^2C digital control bits are buffered with inverter as Fig. 4-8 (a).

Input and output stages have T-coils to compensate for bandwidth degradation caused

by ESD protection. Programmable $1/g_m$ loads are placed at input stage for 50-ohm termination and self-bias voltage with half of VDD. According to process, voltage and temperature variations, size of $1/g_m$ cells are controlled by 3-bit I^2C code for impedance matching. Signal Buffer (SB) is used for pole splitting between the input stage and the main driver. SB, the pre-driver of the Programmable Gain Amplifier (PGA), provides a pole splitting effect by separating input matching block and T-coil & ESD protection network from the large gate cap. Fig. 4-9 shows a structure of main driver. PGA and programmable $1/g_m$ loads are used to control the amount of modulation current flowing through VCSEL. After determining output resistance of the VCSEL driver by 3-bit I^2C code, modulation current is adjusted by 4-bit I^2C code in the PGA. A common-mode feedback (CMFB) loop is employed to source DC current, and the amount of DC current can be controlled by adjusting negative bias voltage of cathode.

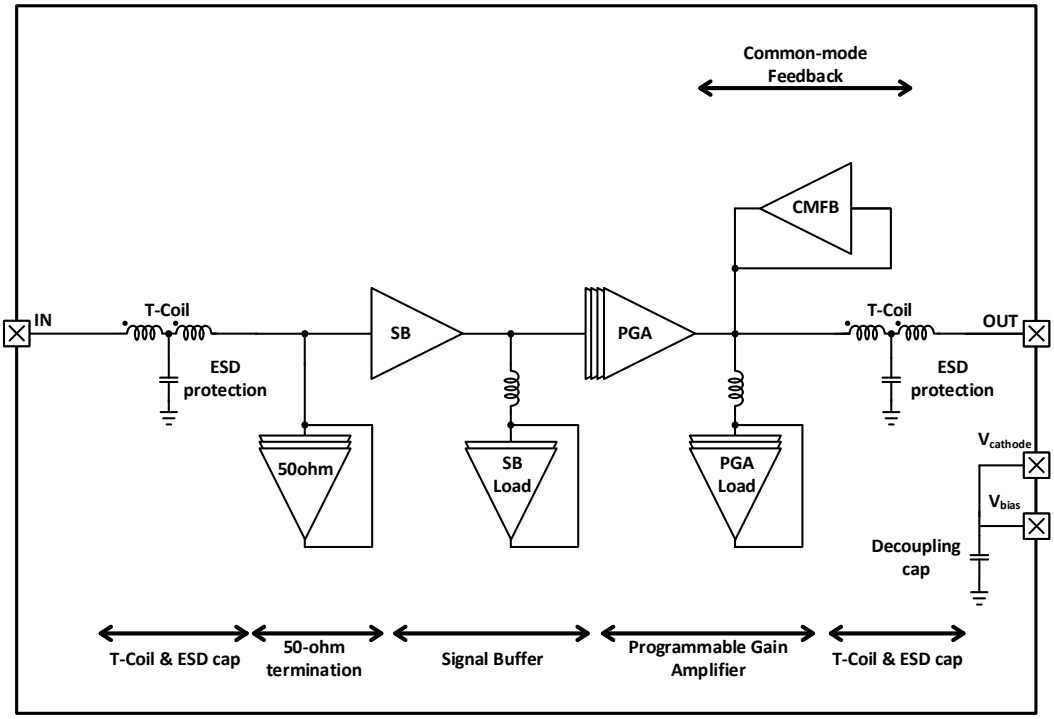


Fig. 4-7. Proposed architecture of VCSEL driver

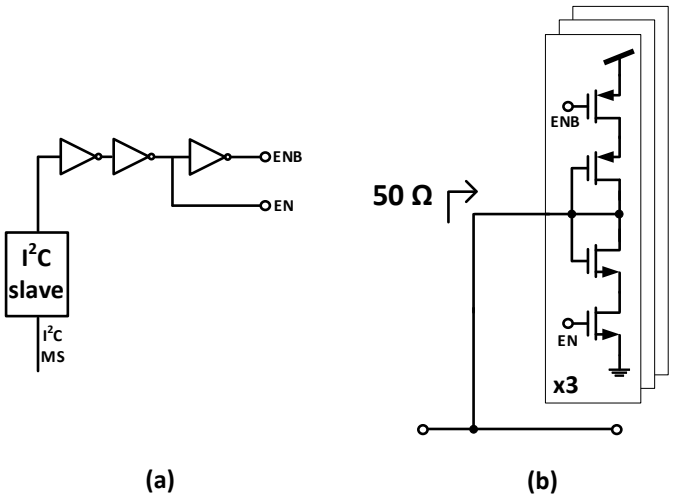


Fig. 4-8. (a) Digital block for I^2C, (b) $1/g_m$ cells for 50-ohm termination

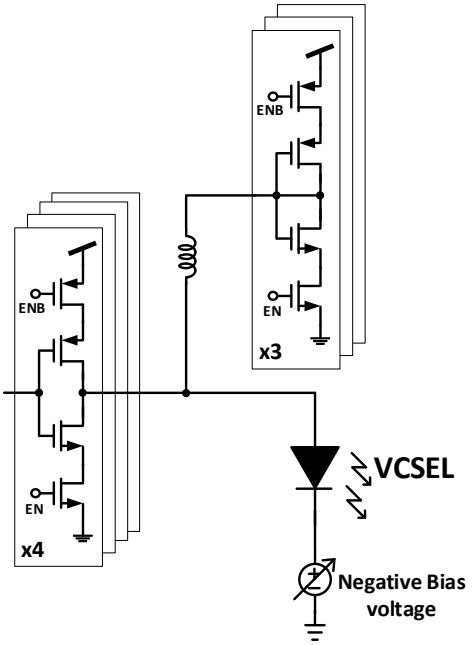


Fig. 4-9. Main driver structure with shunt peaking

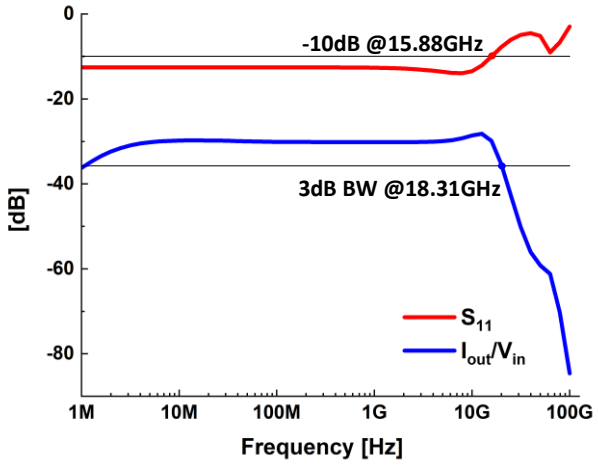


Fig. 4-10. Simulation results of small signal response

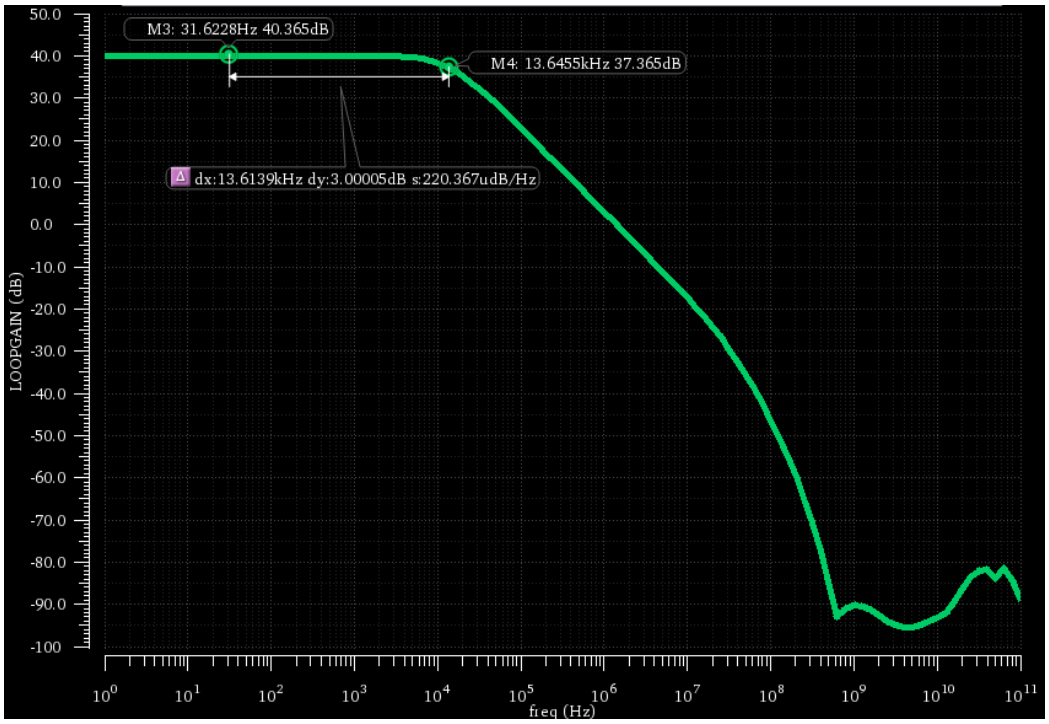


Fig. 4-11. Simulation result of CMFB loop gain

Fig. 4-10 shows post-layout simulation results of small signal responses. Driver bandwidth is 18.31 GHz. Fig. 4-11 shows a CMFB loop gain simulation result. Loop gain is a 40 dB and bandwidth is 13.65 KHz.

4.2.2 Measurement results

A micrography of entire chip is shown in Fig. 4-12. The circuit was designed in 14-nm FinFET technology. It consists of VCSEL driver, driver replica for electrical test, I^2C slave circuits, decoupling cap and bias port for sourcing negative bias voltage to VCSEL cathode. Fig. 4-13 and Fig. 4-14 show the measurement setup for optical transmitter test.

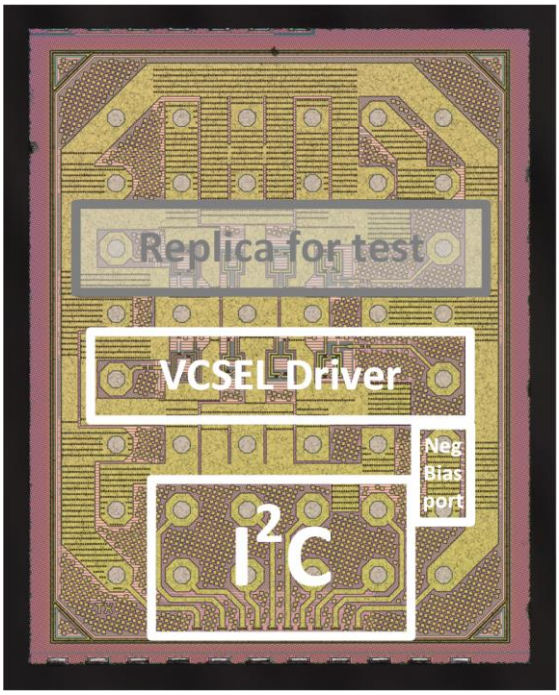


Fig. 4-12. A micrography of the Tx VCSEL Driver

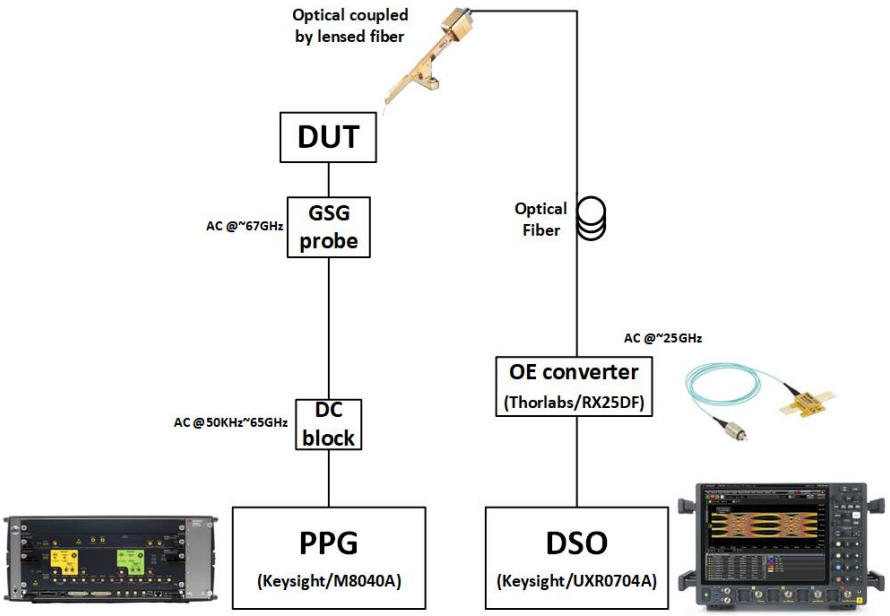


Fig. 4-13. The block diagram of measurement setup

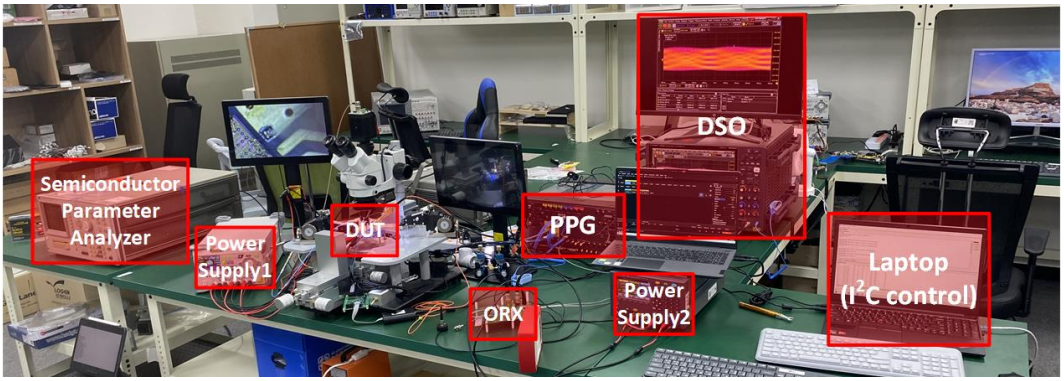


Fig. 4-14. Photo of the measurement setup

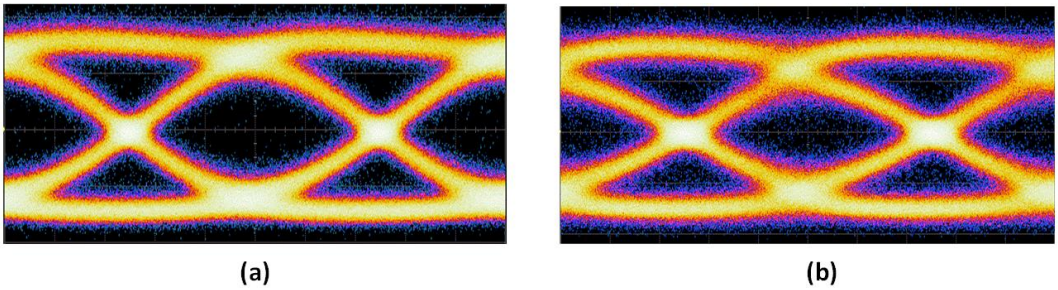


Fig. 4-15. Measured optical NRZ EYE at PRBS31 (a) 25 Gb/s and (b) 30 Gb/s

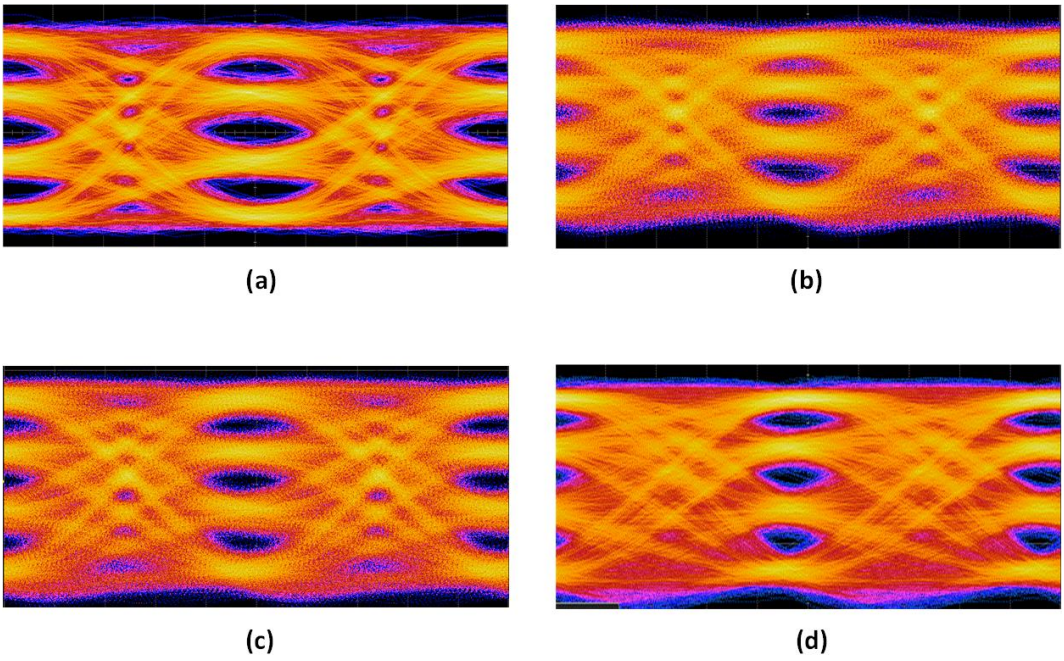
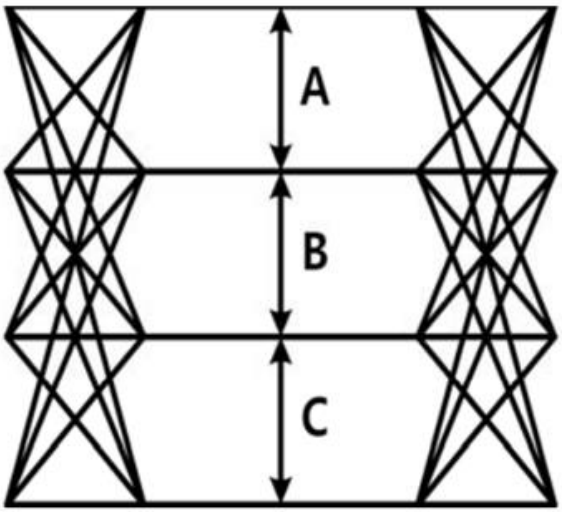


Fig. 4-16. Measured optical PAM-4 EYE at PRBS7 (a) 30 Gb/s, (b) 40 Gb/s, (c) 40 Gb/s with RLM calibration, (d) 50 Gb/s with RLM calibration and Rx FFE

Fig. 4-15 shows NRZ optical EYE measurement results and Fig. 4-16 shows PAM-4 optical EYE measurement results. Bias current is 6 mA and modulation current is 5 $mA_{p\text{-}p}$. The NRZ signal does not have significant signal degradation due to the VCSEL non-linear issue, and signal quality is dominant in the bandwidth of Driver and VCSEL.



$$RLM = \frac{\min(A,B,C)}{(A+B+C)/3}$$

Fig. 4-17. The definition of RLM

The definition of RLM can be confirmed through Fig. 4-17. Unlike the NRZ, the PAM-4 signal is vulnerable to the characteristics of the VCSEL. Fig. 4-16 (a), (b) show different inner EYE openings. Because of the static non-linearity issue of VCSEL and the Driver linearity, RLM of optical PAM-4 EYEs are lowered. Since a large bias current is used and the modulation current is not large, there is no inner EYE skew due to the dynamic non-linear issue of the VCSEL. Fig. 4-16 (c) shows a result when pre-distortion of PAM-4 level was performed in PPG. Comparing Fig. 4-16 (b) and (c), it can be interpreted that the technique for RLM calibration is necessary in the VCSEL driver. Fig. 4-16 (d) shows a result when FFE is performed in Rx.

The transmitter consumes 38.7 mW including bias current sourcing to the VCSEL. Even though the overall size was greatly increased since the control using I^2C was used, it can be confirmed that it has a small power consumption by using the VML structure.

4.3 RLM controllable Driver for PAM-4 signaling

In the previous circuit design, the control function for the level of the PAM-4 signal was treated as necessary from the VCSEL driver design point of view. In addition, it was experimentally confirmed that the function could be achieved through PAM-4 level pre-distortion in the Tx. Because the VCSEL is driven at high bias current, even though the dynamic non-linearity issue does not seriously affect the EYE quality, the static non-linearity issue is fatal to the eye opening.

4.3.1 Proposed architecture

Fig. 4-18 shows a block diagram of proposed RLM controllable VCSEL driver. This is fabricated in CMOS 28-nm process. The previous g_m/g_m structure, shunt peaking structure using an inductor, and CMFB structure are used, and a main driver design to control the RLM is proposed. A large number of adjustable I^2C control blocks were eliminated, and they were made to have an appropriate size for driving 50 Gb/s PAM-4 signals.

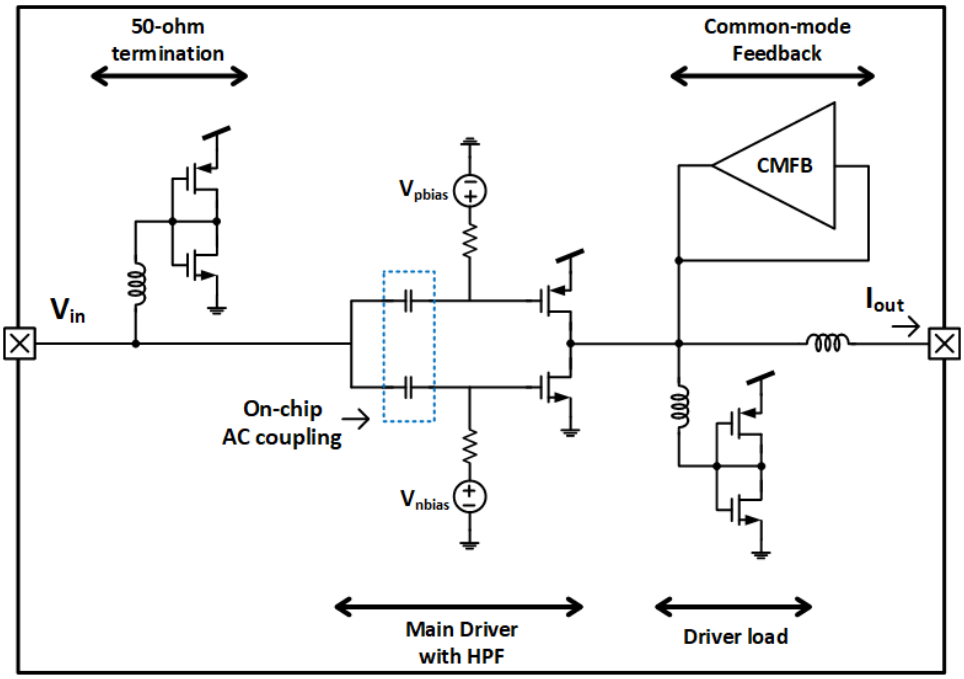


Fig. 4-18. The block diagram of proposed VCSEL driver

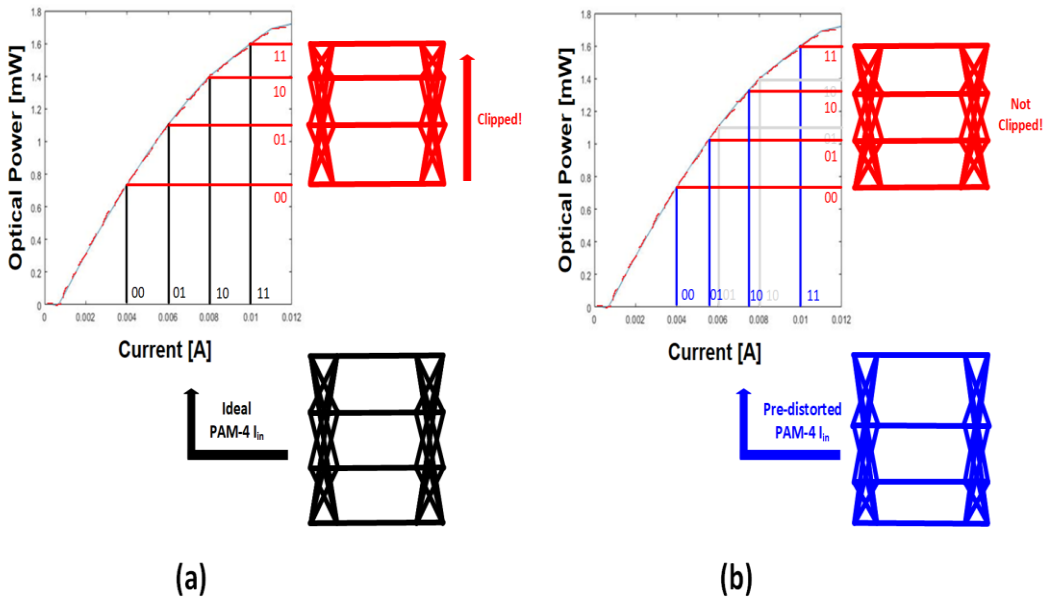


Fig. 4-19. The feature of VCSEL optical EYE in PAM-4 signals

with (a) ideal levels of input, (b) pre-distorted levels of input

Before explaining the proposed RLM controllable driver, I would like to point out the problem that occurs through the static non-linearity issue of VCSEL. As can be seen in Fig. 4-19 (a), when PAM-4 inputs with ideal levels are applied to the VCSEL, each level of the optical EYE is clipped. To compensate this response, a method using pre-distortion can be used as shown in Fig. 4-19 (b).

Before summing the MSB signals and LSB signals in the Serializer, it can be solved by adjusting each amplitude, but the '01' and '10' levels can only be adjusted symmetrically from the mid-point of EYE when using this method. Because it can only do limited pre-distortion, it is not good as an RLM compensation strategy. From the viewpoint of the VCSEL driver, a method capable of flexible level pre-distortion according to the VCSEL's bias current and modulation current control is the appropriate solution.

Fig. 4-20 and Fig. 4-21 show comparison of the original g_m/g_m buffer and proposed structure. In the proposed structure, the gate DC voltage of NMOS and PMOS can be controlled externally by employing each AC coupling capacitor as shown in Fig. 4-20 (b). The previous g_m/g_m has a large signal response as Fig. 4-21 (a), but the proposed structure can control transition curve as Fig. 4-21 (b). Controlling the large signal curve in the proposed structure is achieved by $(\alpha+\beta)$ [V] applied to V_{biasn} and $(\alpha-\beta)$ [V] applied to V_{biasn} shown in Equation (4.4). The α factor controls the degree of movement of the transition curve from original curve, and the β factor controls the gain characteristics.

Let's say $V_{biasn}=\alpha+\beta$, $V_{biasp}=\alpha-\beta$ like Equation (4.4). If both NMOS and PMOS are in the saturation region, the input voltage value x that makes the output voltage equal to VDD/2 is obtained as follows. As a condition for the output of the inverter to be half of VDD, the drain current flowing from NMOS and PMOS can be confirmed through Equation (4.5). Assuming that the channel length modulation term is the same and $k_n=k_p$, Equation (4.6) can be established. As shown in Equation (4.7), making the output voltage VDD/2 is dependent with α and independent with β. The simulation result controlling α and β can be checked in Fig. 4-22 and Fig. 4-23. In order to distort the level of PAM-4 signals, a non-linear response can be used as Fig. 4-24.

$$\begin{aligned} V_{IN} &= x \\ V_{OUT} &= VDD/2 \\ V_{biasn} &= \alpha+\beta \\ V_{biasp} &= \alpha-\beta \end{aligned} \tag{4.4}$$

$$
\begin{aligned}
I_{D,N} &= \frac{1}{2}\mu_N C_{ox}\left(\frac{W}{L}\right)_N \left(V_{GS}-V_{th,N}\right)^2\left(1+\lambda_N V_{DS}\right) \\
&= k_N\left((x+\alpha+\beta)-V_{th,N}\right)^2\left(1+\lambda_N V_{DS}\right) \\
-I_{D,P} &= \frac{1}{2}\mu_P C_{ox}\left(\frac{W}{L}\right)_P \left(V_{SG}+V_{th,P}\right)^2\left(1+\lambda_N V_{SD}\right) \\
&= k_P\left(VDD-(x+\alpha-\beta)+V_{th,P}\right)^2\left(1+\lambda_N V_{SD}\right)
\end{aligned}
\tag{4.5}
$$

$$
(x+\alpha+\beta-V_{th,N})^2 = (VDD-(x+\alpha-\beta)+V_{th,P})^2 \tag{4.6}
$$

$$
\therefore x = VDD/2 + \frac{V_{th,N}+V_{th,P}}{2} - \alpha \tag{4.7}
$$

Since using the AC coupling capacitor in high-speed lines involve a large amount of parasitic capacitance, it is important to employ appropriate size of capacitors. However, in order to prevent DC wander which causes ISI, the cut-off frequency of the high pass filter was set at 6.5 MHz in consideration of the data-rate and pattern. If the target data rate is set to 28 Gbaud and the PRBS15 pattern is taken as an example, the longest run length degrades the subsequent bit level by 0.19 dB on the calculation. Considering the amount of droop and speed, the high-pass corner frequency was determined as above.

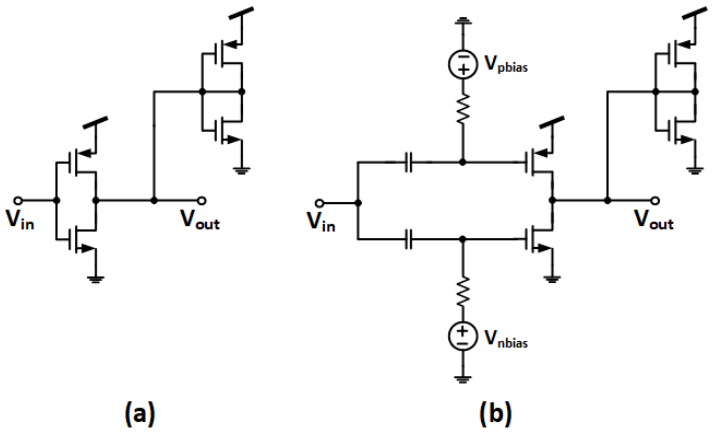


Fig. 4-20. The block diagram of inverter based (a) g_m/g_m buffer, (b) proposed RLM controllable g_m/g_m buffer

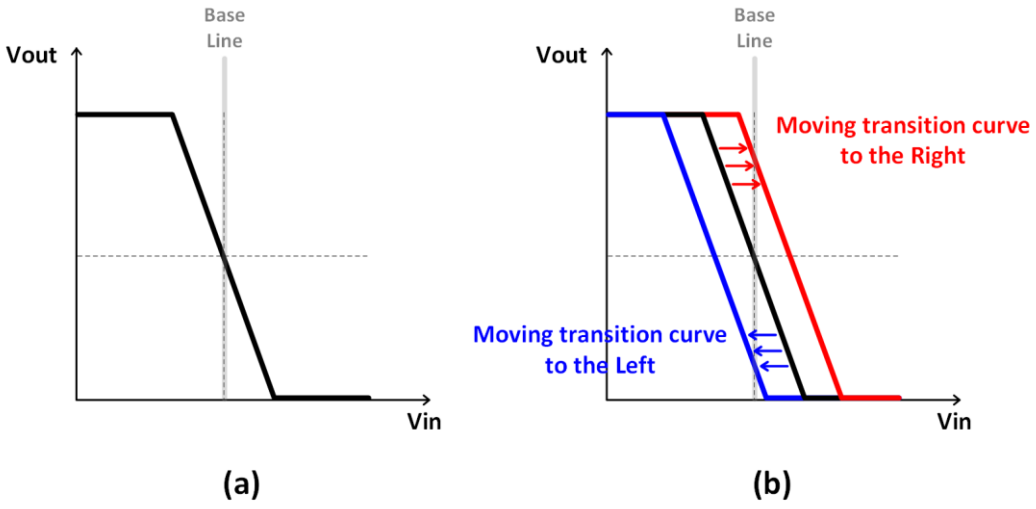


Fig. 4-21. The large signal responses of (a) g_m/g_m buffer, (b) proposed buffer

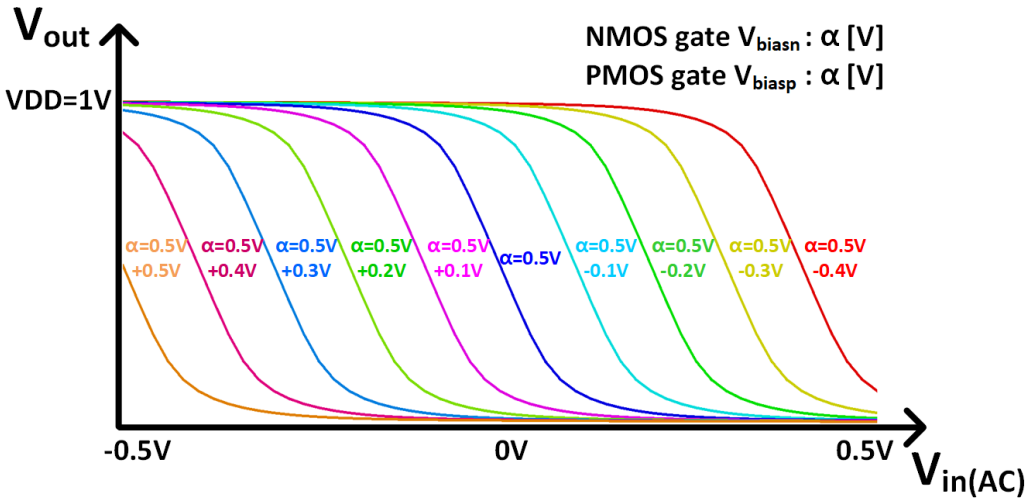


Fig. 4-22. The behavior simulation result of moving transition curve with α factor

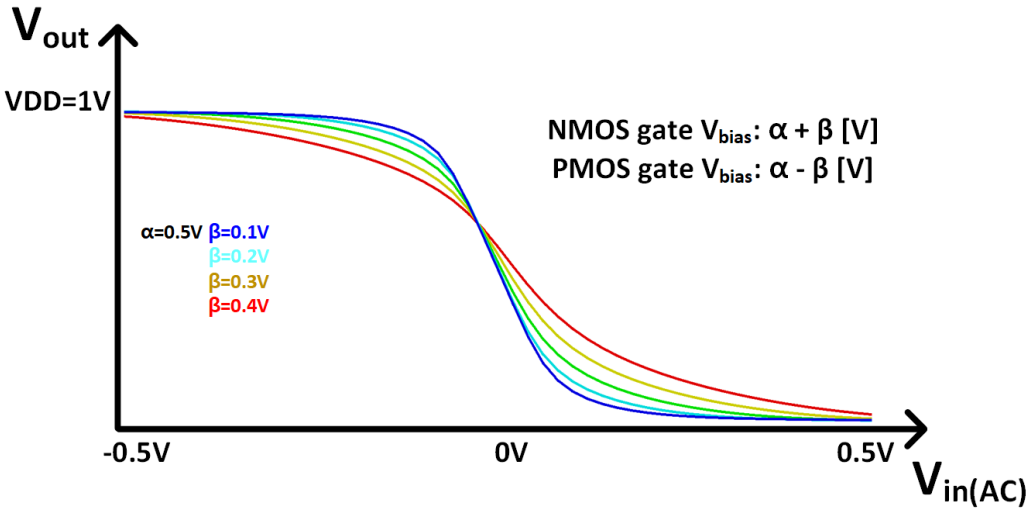


Fig. 4-23. The behavior simulation result of large signal responses with β factor

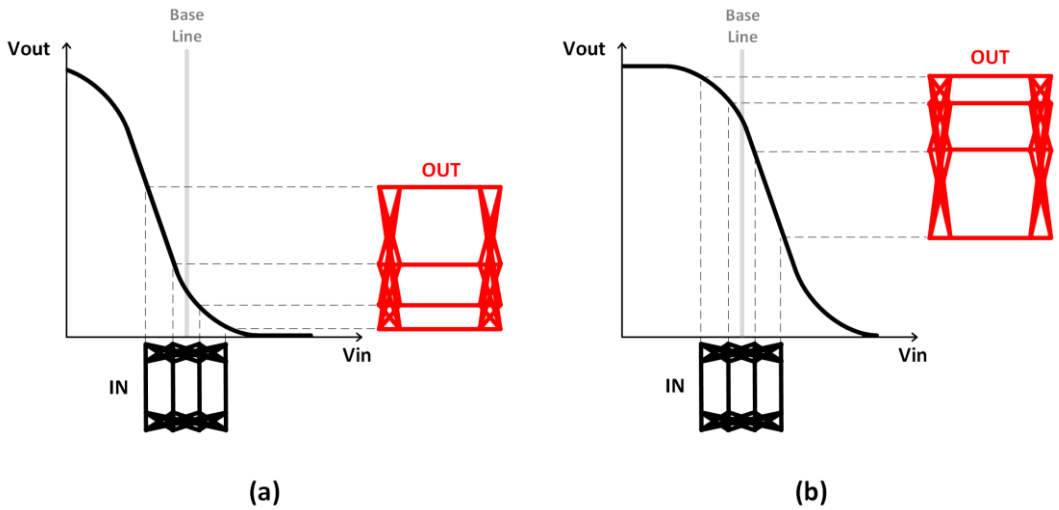


Fig. 4-24. The example of RLM control scheme with proposed structure (a) pre-distortion for downside clipping, (b) pre-distortion for upside clipping

This approach for pre-distortion scheme has two advantages. First, flexible control of each level is possible. It is an effective solution because PAM-4 RLM optimization can be performed according to various applications to be applied. Second, if the above structure is used at the last stage of the driver, the burden of the non-linearity problems occurring in previous circuits are relieved. When receiving PAM-4 signals at Tx driver or Rx as input, the swing size is limited considering non-linearity occurring in the circuit. However, if proposed buffer is used at the back end of entire architecture, there are no restrictions on

the size of the swing because PAM-4 level distortion issues are mitigated. Fig. 4-25 show behavior simulation results of RLM control buffer.

Fig. 4-25. PAM-4 50 Gb/s simulation results for behavior of RLM control buffer with (a) downside clipping, (b) upside clipping

4.3.2 Measurement results

Fig. 4-26 shows a micrography of proposed RLM controllable driver. As you can see in the picture, a top metal with a length of about 200-um was used on the input and output sides. Considering the total area of the chip and the size of the core block, line inductance can only be seen on the input or output side of the driver. In this design, inductive lines are appropriately placed at the input and output.

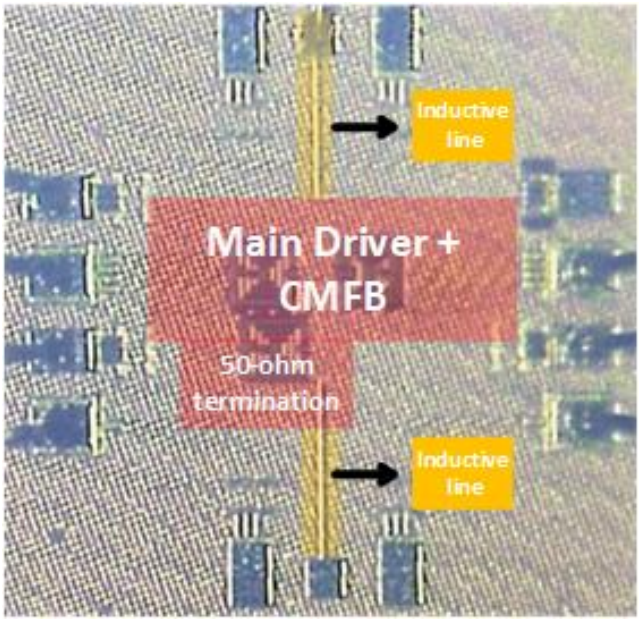


Fig. 4-26. A micrography of proposed VCSEL driver

Fig. 4-27 shows the measurement setup and measurement result can be confirmed in Fig. 4-28. The size control of EYE corresponding to MSB and LSB was confirmed. The changes in swing size were achieved by adjusting V_{biasp} and V_{biasn}. It contains the results for each of the three control setup environments. The '--' state means a bias setup in which only α value exists and β has no value. Then, 'V_{biasn}: ↑ ' , 'V_{biasp}: ↓ ' means the relative size of the amplitude in which β is formed. The y-axis scale was captured identically for all three EYE results. As can be seen from the results of the experiment, it is confirmed that the voltage swing can be adjusted by adjusting the range of V_{biasp} and V_{biasn} when a 25 Gb/s PRBS15 input signal is given. The static power consumption is 13-mW. Post layout simulation results for RLM optimization along with the VCSEL equivalent model can be confirmed through Fig. 4-29.

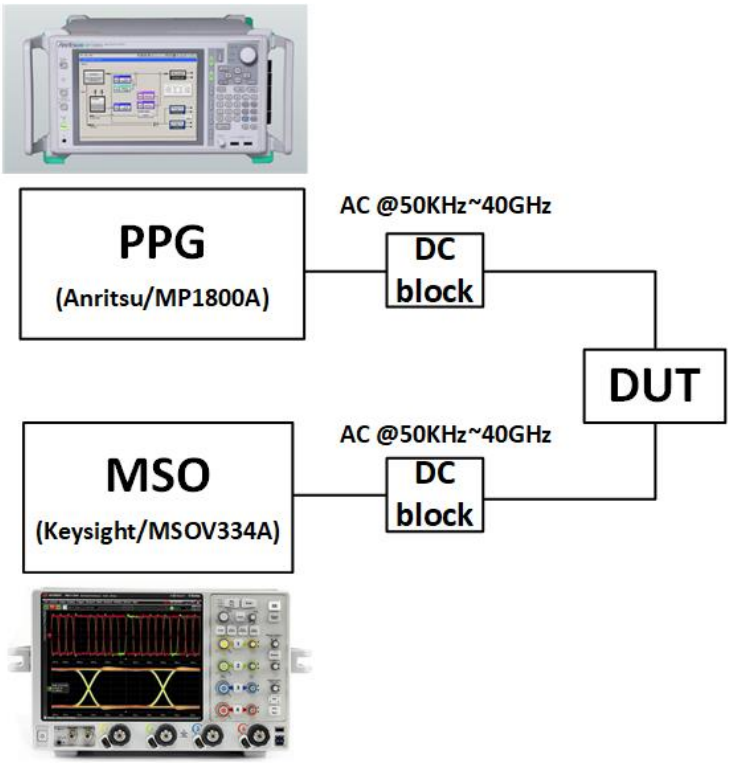


Fig. 4-27. Measurement setup for electrical test

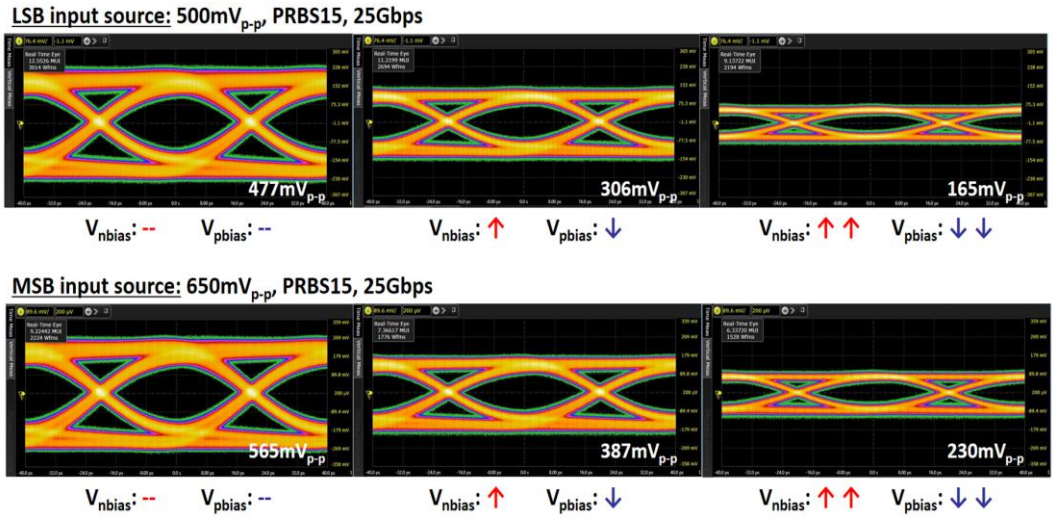


Fig. 4-28. Measurement electrical EYE results for the level pre-distortion.

(a) LSB equivalent, (b) MSB equivalent

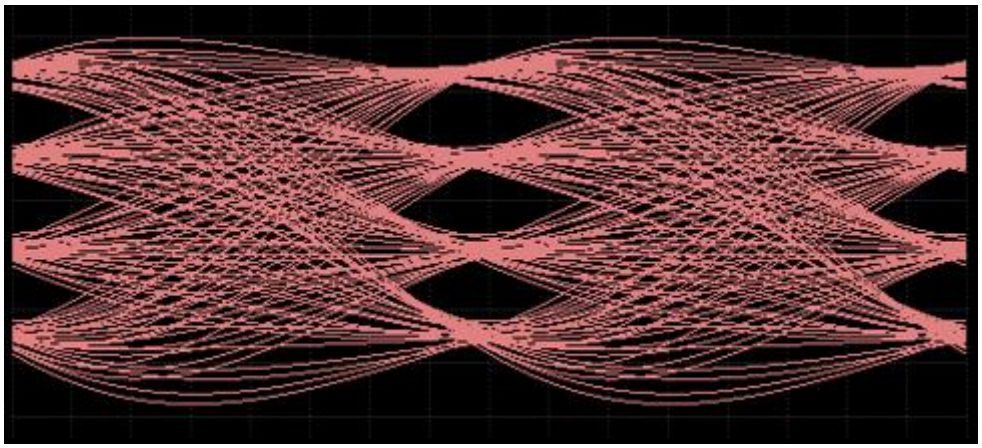


Fig. 4-29. Post layout simulation result of 50 Gb/s pre-distorted PAM-4 optical EYE with VCSEL SPICE model

5. Conclusions

This paper described VCSEL properties and its driving circuits for high-speed optical link targeting short reach. A VCSEL equivalent model was employed for using in SPICE simulation during circuit design. It is made based on the Verilog-A language, and includes the S_{11} and S_{21} responses for each bias current of VCSEL, and the L-I-V curve, which is a DC characteristic, is modeled.

In order to design a low-power, high-speed circuit, a voltage mode driver was adopted as the basic structure. The g_m/g_m buffer, which operates by employing a $1/g_m$ load in the inverter, was used as a basic structure, and bandwidth boosting was performed using the inductor shunt peaking technique. Demo data rate is NRZ 35 Gb/s, PAM-4 40 Gb/s. It was confirmed that it is a low-power VCSEL driver with static power consumption of 38.7 mW and energy efficient of 0.9675 pJ/b.

As a result of the first VCSEL driver, it was experimentally confirmed that compensation for the static non-linearity of the VCSEL is necessary when driving PAM-4

signals. Therefore, a circuit capable of controlling the RLM of PAM-4 was proposed. It is a method to move transition curve of inverter while separately adjusting the gate bias of the inverter's NMOS and PMOS by using high-pass filtering for each signal path, and the results of this were confirmed by post layout simulation and experiments.

	15' JSCC	'16 JLT	'17 JSSC	'18 JSSC	22' JSSC	*This Work*
Process	65-nm CMOS	0.25-um InP DHBT	130-nm SiGe BiCMOS	14-nm FinFET	28-nm CMOS	14-nm FinFET
Modulation	NRZ	PAM-4	NRZ	NRZ	NRZ	NRZ, PAM-4
Demo. data-rate	15Gb/s	56Gb/s	50Gb/s	45Gb/s	56Gb/s	30Gb/s, 40Gb/s
Output stage	VM, SE	CM, SE	CM, SE	CM, SE	VM, SE	VM, SE
EQ type	2-tap FFE	No EQ	Asymmetric 3-tap FFE	2-tap FFE	Pulse-shaping, Shunt peaking, 3-tap FFE	Shunt peaking
VCSEL BW (GHz)	7.5	24	18	20	25	17
Energy Efficiency (pJ/bit)	2.0	3.7	3.8	1.81	1.28	1.23, 0.925

Table. 5-1. Performance comparison for VCSEL Driver

Bibliography

[1] YOLE, “Optical Transceivers for Datacom & Telecom 2022”

[2] Cisco, “Cisco Global Cloud Index: Forecast and Methodology, 2016–2021”

[3] Cheng H-T, Yang Y-C, Liu T-H, Wu C-H. Recent Advances in 850 nm VCSELs for High-Speed Interconnects. Photonics. 2022; 9(2):107.

[4] A. S. Ramani, S. Nayak and S. Shekhar, "A Differential Push-Pull Voltage Mode VCSEL Driver in 65-nm CMOS," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 11, pp. 4147-4157, Nov. 2019.

[5] D. Mahgerefteh et al., "Techno-Economic Comparison of Silicon Photonics and Multimode VCSELs," in Journal of Lightwave Technology, vol. 34, no. 2, pp. 233-242, 15 Jan.15, 2016.

[6] P. V. Mena, J. J. Morikuni, S. . -M. Kang, A. V. Harton and K. W. Wyatt, "A simple rate-equation-based thermal VCSEL model," in Journal of Lightwave Technology, vol. 17, no. 5, pp. 865-872, May 1999.

[7] D. Kucharski et al., "A 20 Gb/s VCSEL driver with pre-emphasis and regulated output impedance in 0.13 μm CMOS," ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005., 2005, pp. 222-594 Vol. 1.

[8] K. Ohhata, H. Imamura, Y. Takeshita, K. Yamashita, H. Kanai and N. Chujo, "Design of a 4 x 10 Gb/s VCSEL Driver Using Asymmetric Emphasis Technique in 90-nm CMOS for Optical Interconnection," in IEEE Transactions on Microwave Theory and Techniques, vol. 58, no. 5, pp. 1107-1115, May 2010.

[9] Y. Tsunoda, M. Sugawara, H. Oku, S. Ide and K. Tanaka, "8.9 A 40Gb/s VCSEL over-driving IC with group-delay-tunable pre-emphasis for optical interconnection," 2014 IEEE International Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2014, pp. 154-155.

[10] S. Palermo, A. Emami-Neyestanak and M. Horowitz, "A 90 nm CMOS 16 Gb/s Transceiver for Optical Interconnects," in IEEE Journal of Solid-State Circuits, vol. 43, no. 5, pp. 1235-1246, May 2008.

[11] M. M. Khafaji, G. Belfiore, J. Pliva, R. Henker and F. Ellinger, "A 4 x 45 Gb/s Two-Tap FFE VCSEL Driver in 14-nm FinFET CMOS Suitable for Burst Mode Operation," in IEEE Journal of Solid-State Circuits, vol. 53, no. 9, pp. 2686-2695, Sept. 2018.

[12] M. Mansuri et al., "A Scalable 32–56 Gb/s 0.56–1.28 pJ/b Voltage-Mode VCSEL-Based Optical Transmitter in 28-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 57, no. 3, pp. 757-766, March 2022.

[13] M. Raj, M. Monge and A. Emami, "A Modelling and Nonlinear Equalization Technique for a 20 Gb/s 0.77 pJ/b VCSEL Transmitter in 32 nm SOI CMOS," in IEEE Journal of Solid-State Circuits, vol. 51, no. 8, pp. 1734-1743, Aug. 2016.

[14] A. Tyagi et al., "A 50 Gb/s PAM-4 VCSEL Transmitter With 2.5-Tap Nonlinear Equalization in 65-nm CMOS," in IEEE Photonics Technology Letters, vol. 30, no. 13, pp. 1246-1249, 1 July1, 2018.

[15] U. Hecht et al., "Non-Linear PAM-4 VCSEL Equalization and 22 nm SOI CMOS DAC for 112 Gbit/s Data Transmission," 2019 12th German Microwave Conference (GeMiC), 2019, pp. 115-118.

[16] H. Li et al., "A 3-D-Integrated Silicon Photonic Microring-Based 112-Gb/s PAM-4 Transmitter With Nonlinear Equalization and Thermal Control," in IEEE Journal of Solid-State Circuits, vol. 56, no. 1, pp. 19-29, Jan. 2021.

[17] R. Michalzik, Ed., VCSELs: Fundamentals, Technology and Applications of Vertical-Cavity Surface-Emitting Lasers. New York, NY, USA: Springer, 2013.

[18] J. Gao, "High Frequency Modeling and Parameter Extraction for Vertical-Cavity Surface Emitting Lasers," in Journal of Lightwave Technology, vol. 30, no. 11, pp. 1757-1763, June1, 2012.

[19] V. Kozlov and A. Chan Carusone, "Capacitively-Coupled CMOS VCSEL Driver Circuits," in IEEE Journal of Solid-State Circuits, vol. 51, no. 9, pp. 2077-2090, Sept. 2016.

[20] A. A. Ciubotaru and J. S. Garcia, "An integrated direct-coupled 10-Gb/s driver for common-cathode VCSELs," in IEEE Journal of Solid-State Circuits, vol. 39, no. 3, pp. 426-433, March 2004.

[21] J. E. Proesel, B. G. Lee, C. W. Baks and C. L. Schow, "35-Gb/s VCSEL-Based optical link using 32-nm SOI CMOS circuits," 2013 Optical Fiber Communication Conference and Exposition and the National Fiber Optic Engineers Conference (OFC/NFOEC), 2013, pp. 1-3.

[22] D. M. Kuchta et al., "A 71-Gb/s NRZ Modulated 850-nm VCSEL-Based Optical Link," in IEEE Photonics Technology Letters, vol. 27, no. 6, pp. 577-580, 15 March15, 2015.

[23] K. R. Lakshmikumar et al., "A Process and Temperature Insensitive CMOS Linear TIA for 100 Gb/s/λ PAM-4 Optical Links," in IEEE Journal of Solid-State Circuits, vol. 54, no. 11, pp. 3180-3190, Nov. 2019

Abstract (In Korean)

고속 광 상호 연결을 위한 850 nm VCSEL 기반의 저전력 송신기

클라우드 서비스 및 모바일 컨텐츠 사업이 발달 하면서 데이터센터에서 감당해야할 데이터 트래픽의 수는 매년 기하급수적으로 증가하고있다. 데이터 센터 내에서 광 상호 연결은 매력적인 solution 중 하나이다. 850-nm Vertical-Cavity Surface-Emitting Laser(VCSEL) 기반의 short reach optical link 는 값이 저렴하고 비교적 높은 data rate 을 가질 수 있다는 장점 때문에 활발히 연구가 진행중이다. Direct modulation 방법인 Non-return-to-Zero 방식이 전통적으로 사용되어져 왔으며, 최근에는 Pulse Amplitude Modulation level-4 (PAM4) 방식의

signal processing 이 data-rate 을 높이기 위한 방법으로 사용되고 있다. VCSEL 은 wafer 단위로 생산 가능한 semiconductor laser diode 이기 때문에 값이 저렴하고, beam quality 가 좋다는 장점이 있지만, low optical power, non-linear properties, processes and temperature variations 등의 단점이 존재한다.

본 연구에서는 VCSEL 을 high-speed 에서 동작 시키기 위하여 필요한 various properties 들에 대해 소개하고자 한다. SPICE 기반에서 Driver 와 함께 simulation 하여 driver 설계를 최적화 하기 위한 VCSEL model 을 Verilog-A 기반으로 만들었다. VCSEL 의 bias current 별 s-parameter 와 L-I-V data 를 측정하여 4 차 polynomial 로 fitting 하였다. 인버터 타입의 앰프를 기본적인 구조로 사용하여, CML 구조 대비 low power consumption 을 갖도록 Driver 를 디자인 하였다. 또한, I^2C 를 사용하여 Driver 의 output resistance 를 조절 할 수 있도록 하였다. VCSEL 의 DC curve 가 비선형성을 갖는 다는 특징 때문에, PAM-4 를 driving 하는 경우에 the level mismatch ratio(RLM)가 상당히 낮게 나올 수 있다는 문제점이 있다. 이를 해결하기 위해 driver 단에서 pre-distortion 을 통해 VCSEL driver 의 RLM 을 높일 수 있도록 driver 를 설계 하였다.

핵심 단어: 광 상호 연결, 850 nm VCSEL, VCSEL model, VM Driver, low power, NRZ, PAM-4, 비선형성, RLM, pre-distortion