Analysis on Static Noise Margin and Single Event Upset of C-SRAM for Radiation Tolerance

Eunju Jo

The Graduate School

Yonsei University

Department of Electrical and Electronic Engineering

Analysis on Static Noise Margin and Single Event Upset of C-SRAM for Radiation Tolerance

A Master's Thesis

Submitted to the Department of Electrical and Electronic Engineering

and the Graduate School of Yonsei University

in partial fulfillment of the requirements for the degree of

Master of Science

Eunju Jo

August 2022

This certifies that the master's thesis of Eunju Jo is approved.

Thesis Supervisor: Prof. Woo-young Choi

Prof. Seong-Ook Jung

Ph.D. Inyong Kwon

The Graduate School

Yonsei University

August 2022

감사의 글

학부 시절부터 시작 된 “전기전자공학과” 학문의 길을 석사를 끝으로 대학원 생활을 마무리 짓게 되었습니다. 길다면 길고 짧다면 짧을 수 있는 7년 반의 시간 동안 많은 분들의 도움을 통해 다양한 경험을 할 수 있었고 학문적 지식을 쌓을 수 있었습니다. 때로는 불안감으로 가득했던 지난 날들을 같이 손잡아 주고 격려해주신 모든 분들께 이번 기회를 통해 감사의 인사를 전해 드립니다. 먼저, 초고속 회로 및 시스템 연구실에서 석사 생활을 할 수 있게 해주시고 한국원자력연구원에서 연구할 수 있도록 많은 배려를 해주신 최우영 지도교수님께 진심을 담아 감사드립니다. 갑작스러운 코로나 유행으로 인해 많이 찾아 뵙지 못했음에도 연구 진행에 있어 많은 조언과 격려를 해주신 덕분에 무사히 대학원 생활을 잘 마무리 지을 수 있었습니다. 그리고 학위 논문 심사를 위해 바쁘실 텐데도 귀중한 시간을 내주신 정성욱 교수님께도 감사 인사를 전해 드립니다. 교수님의 조언을 통해 보다 더 완성도 있는 논문을 작성할 수 있었습니다. 그리고 권인용 박사님, 처음 뵈었을 때가 엊그제 같은데 벌써 4년의 시간이 흘렀습니다. 박사님께서 ICR Lab의 일원으로 받아주셔서 제가 지금의 자리까지 올 수 있었습니다. 많이 부족한 학생 임에도 불구하고 많은 조언과 격려를 해주시고, 다양한 설계를 해볼 수 있도록 많은 기회를 주셔서 감사드립니다. 마지막으로, 항상 저의 의견을 존중해주고 묵묵히 뒷바라지 해준 가족들에게도 감사의 인사를 전합니다. 모든 분들이 있었기에 제가 무사히 대학원 생활을 마무리 지을 수 있었습니다. 진심으로 감사드립니다.

2022 년 8 월 조은주 올림

Table of Contents

Reference

국문요약

List of Figures

List of Tables

Abstract

Analysis on Static Noise Margin and Single Event Upset of C-SRAM for Radiation Tolerance

Eunju Jo

Dept. of Electrical and Electronic Engineering

The Graduate School, Yonsei University, Seoul, Korea

This thesis is about the analysis on static noise margin (SNM) and single event upset (SEU) of capacitor-static random access memory (C-SRAM) for radiation tolerance. In the space environment, a common problem in memory semiconductors such as a static random access memory (SRAM) is soft errors. These soft errors cause a bit flip and this event is referred to as a SEU.

Many radiation-hardened SRAM cells such as a Quatro SRAM, we-Quatro SRAM, and DICE SRAM cell have been reported for years. However, these designs have the disadvantage of taking up more area than the 6T SRAM cell. The

Quatro SRAM cell uses 10 transistors. Likewise, the DICE SRAM cell and we-Quatro SRAM cell consist of 12 transistors.

I propose a new radiation hardened SRAM cell design named as C-SRAM. The C-SRAM is simply added a capacitor to a conventional 6T SRAM. It was designed to mitigate radiation effect using a conservation law of electrical charge. Moreover, a cell size is the same as the conventional 6T SRAM cell.

SNMs, which are indicators of operational stability, are equal to the conventional 6T SRAM values in 530mV (hold mode), 220mV (read mode), and 860mV (write mode). In the simulation test of the SEU, the result is 4.761x better than the conventional 6T SRAM with the value of 247.494 fC. In addition, an irradiation experiment also confirmed that the C-SRAM cell is better than the 6T SRAM. The conventional 6T SRAM chip and C-SRAM chip were designed using standard 0.18 μm CMOS process.

Keywords: static noise margin (SNM), single event upset (SEU), radiation tolerance, soft error, radiation hardened SRAM cell, C-SRAM

1. Introduction

In the space environment, a common problem in memory semiconductors is soft errors [1], [2]. The soft error is a sort of single event effect (SEE) caused by radiation, which means that high energetic particles generate electric charges or current inside the semiconductor chip, resulting in malfunction [3], [4].

Static random access memory (SRAM) is now widely used in many digital circuits. The memory device of which cell consists of inverters can retain its stored information as long as power is supplied. Also, it has some advantages in fast processing speed. However, SRAMs are also vulnerable to radiation, especially when SEU occurs [2]. The SEU is a type of SEE that makes bits inverted. Therefore, it is critical for SRAM and must be considered when designing for specific applications under radiation environments.

Various radiation hardened SRAM cells have been reported for years [4]-[6]. But I think the methods that change the number of transistors are saturated. For example, the Quatro SRAM cell uses 10 transistors. Likewise, the DICE SRAM cell

and we-Quatro SRAM cell consist of 12 transistors. Therefore, I approached the cell design in a different way.

In this thesis, I propose a new 6T SRAM cell design which is simply added a capacitor to a conventional 6T SRAM as shown in Fig. 1.1 and Fig. 1.2. Then, I named it capacitor-static random access memory (C-SRAM). Even if the voltage value of Q or QB changes due to the radiation effect, the value will return stably again by the conservation law of electrical charge. Therefore, data can be protected from SEE. In addition, C-SRAM has an advantage of having the same cell size as the 6T SRAM, unlike the Quatro, we-Quatro, and DICE SRAM cell.

SNMs, which are indicators of operational stability, are equal to the 6T SRAM values in 530mV (hold mode), 220mV (read mode), and 860mV (write mode). Accordingly, it may be confirmed that even if a capacitor is added, it does not affect the operation. In addition, the simulation test of SEU obtained 4.761x better results than the conventional 6T SRAM with a value of 247.494 fC. In order to demonstrate the radiation tolerance, I conducted irradiation experiments.

In proton accelerator experiment, I perform test at two energy levels: 45 MeV and 100 MeV, in the fluence of $1x10^{11}$ particles/cm^2. As a result, since an error

occurs only in the conventional 6T SRAM, it is possible to prove that the C-SRAM is excellent. Additionally, experiment is conducted with H ions at an ion beam facility under the condition of an energy level of 150 keV and the fluence of $1x10^{17}$ particles/cm^2. This result will be described in detail in a later section.

Through these experiment results, it is confirmed that the new radiation hardened SRAM cell I proposed perform better than the 6T SRAM cell. As a result, it should be noted that C-SRAM cell performs well without change of cell size and SNM value compared to the 6T SRAM.

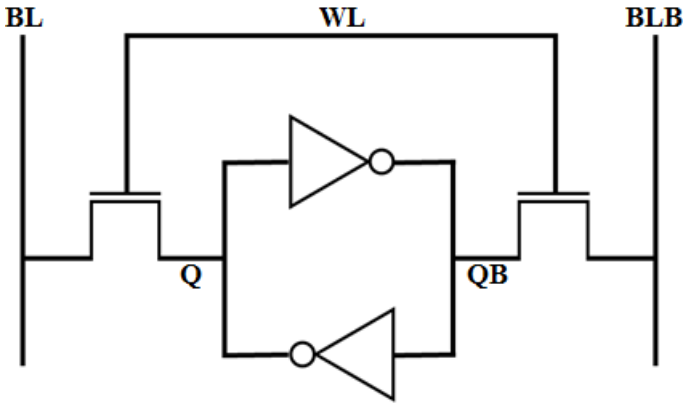

Figure. 1.1 Block diagram of the conventional 6T SRAM cell.

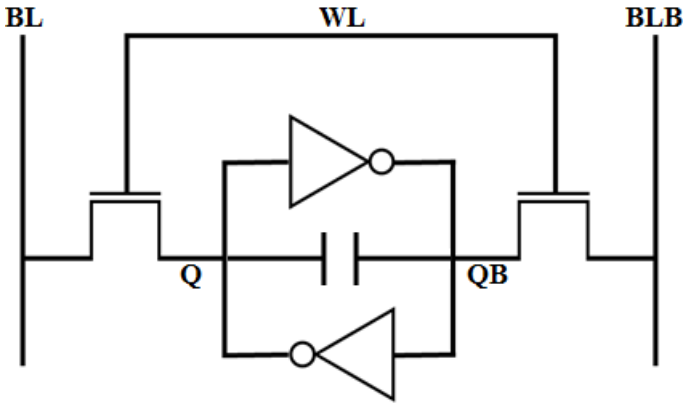

Figure. 1.2 Block diagram of C-SRAM cell.

2. Background

2.1 Conventional 6T SRAM

2.1.1 Structure

As shown in Fig. 2.1, the conventional 6T SRAM cell consists of six transistors which are pull-down transistors, access transistors, and pull-up transistors.

The Q and QB are data nodes. In addition, the word line(WL), bit line (BL), and bit line bar (BLB) are used in read/write operation. The read and write operation will be described in the following sections.

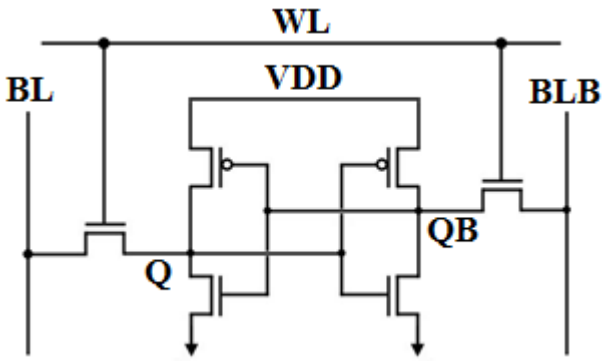

Figure. 2.1 Structure of the conventional 6T SRAM cell.

2.1.2 Operation

2.1.2.1 Hold Operation

In hold operation, the WL is given a LOW signal to turn off the access transistors. Thus, the data node Q and QB remains value in its initial condition.

If you wrote Q=0 V in the previous write operation, you can see that the cell has Q=0 V and QB=1.8 V in the hold mode as shown in the Fig. 2.2. Conversely, if the Q value was 1.8 V in the previous write operation, the Q and QB would remain 1.8 V and 0 V in the hold mode, respectively.

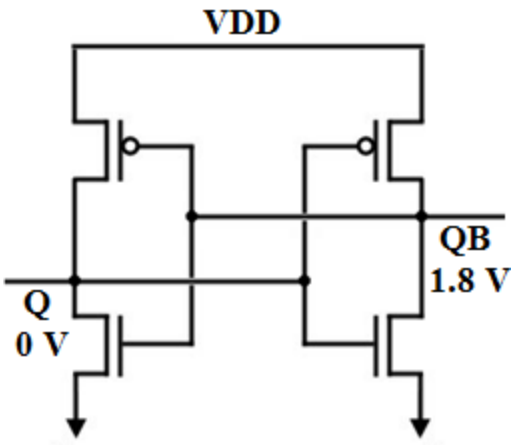

Figure. 2.2 Hold operation of the conventional 6T SRAM.

2.1.2.2 Read Operation

First, the WL is given a LOW signal to turn off the access transistors. The BL and BLB are then pre-charged to half of the VDD as shown in the Fig. 2.3. When the access transistors are turned on by giving HIGH signal to WL again, the values stored in nodes Q and QB are transmitted into BL and BLB. Finally, it is amplified by a sense amp at the end of BL and BLB.

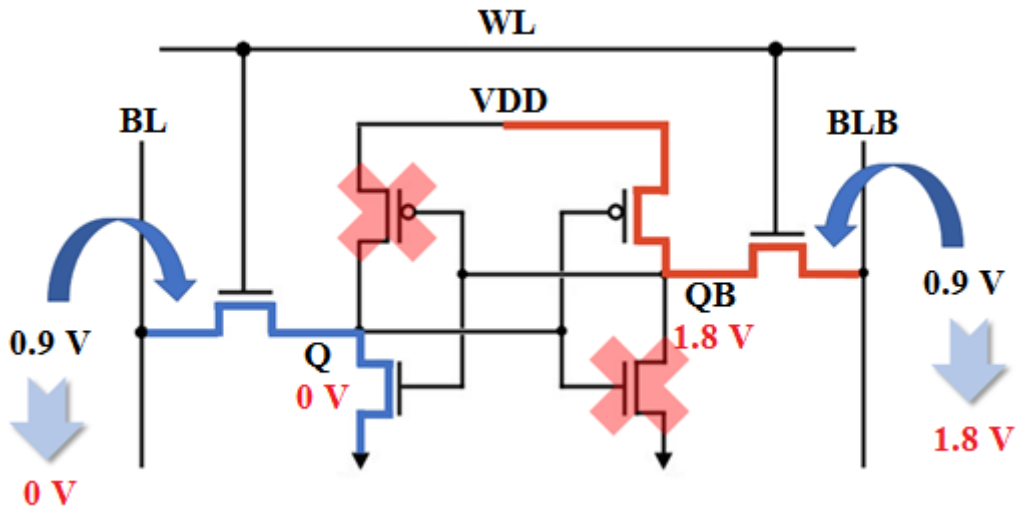

Figure. 2.3 Read operation of the conventional 6T SRAM.

2.1.2.3 Write Operation

In contrast to the read operation, the access transistors are initially turned on by applying a HIGH signal to the WL. As shown in Fig. 2.4, the BL must get HIGH signal for writing HIGH to memory, and LOW signal for writing LOW. Finally, turning off the access transistors by giving the LOW signal to the WL ends the operation and keeps the memory value until next writing.

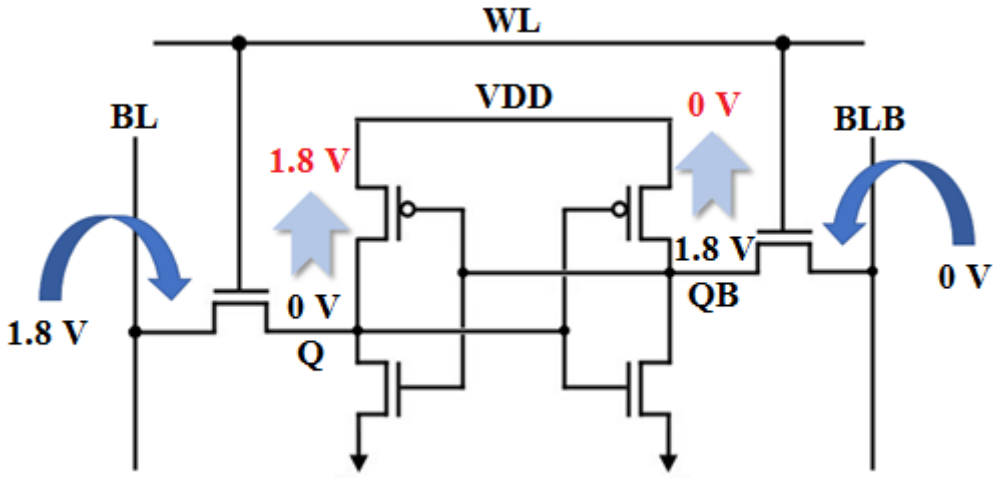

Figure. 2.4 Write operation of the conventional 6T SRAM.

2.1.3 Radiation Effect

Many radiation effects have been reported such as total ionizing dose (TID) and single event effect (SEE) [7].

When a transistor is exposed to high-energy particles, electron-hole pairs are generated in the oxide region. This generation leads to almost TID effect. The mobility of holes is relatively slower than the electrons. So, they can be trapped in the silicon and silicon dioxide region [7]-[9]. The TID effect is simply shown in Fig. 2.5.

In the case of SEE, high energetic particles generate electric charges or current inside the semiconductor chip, resulting in malfunction [10]-[12]. The SEE is also simply shown in Fig. 2.6. This SEE can be divided into hard error and soft error. If the circuit is recoverable after being affected by the SEE, it is called a soft error. Conversely, a case that does not is called a hard error. Representatively, there are single event latch-up (SEL) (hard error) and SEU (soft error). And I will focus on the SEU.

In the space environment, a common problem in memory semiconductors such as a SRAM is soft errors. These soft errors cause a bit flip and this event is referred to as the SEU.

A data of the conventional 6T SRAM is easily flipped by the radiation. In the worst case, current is generated in a sensitive node due to radiation effects. If the data of the affected node is changed, then the other is instantly changed along. Various radiation hardened SRAM cells such as a Quatro SRAM cell, we-Quatro SRAM cell, and DICE SRAM cell have been reported for years. And, I also propose a new radiation hardened SRAM cell using a capacitor to address this problem.

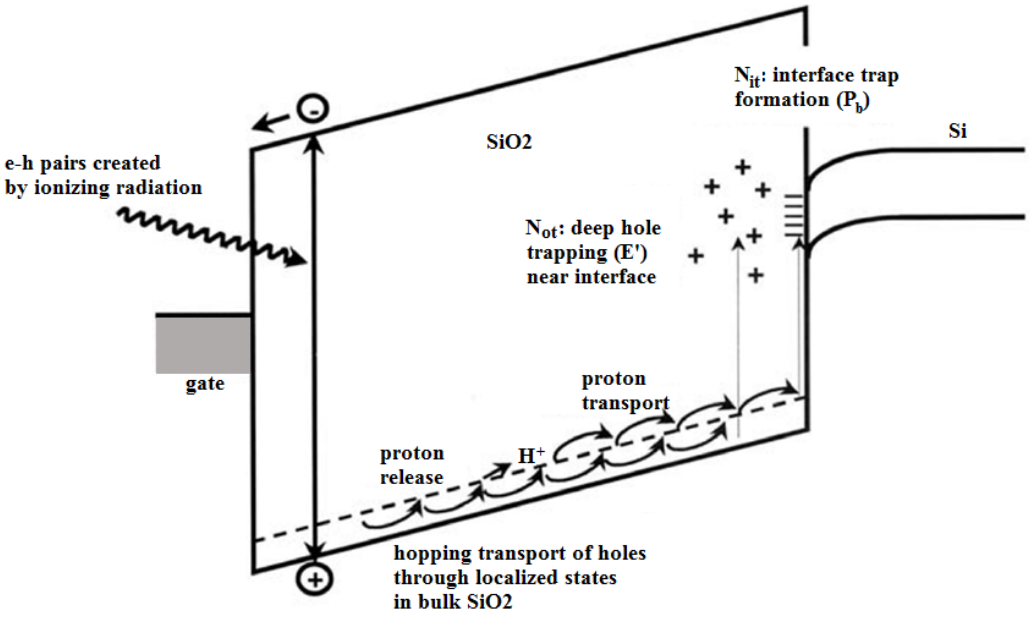

Figure. 2.5 Illustration of the TID damage.

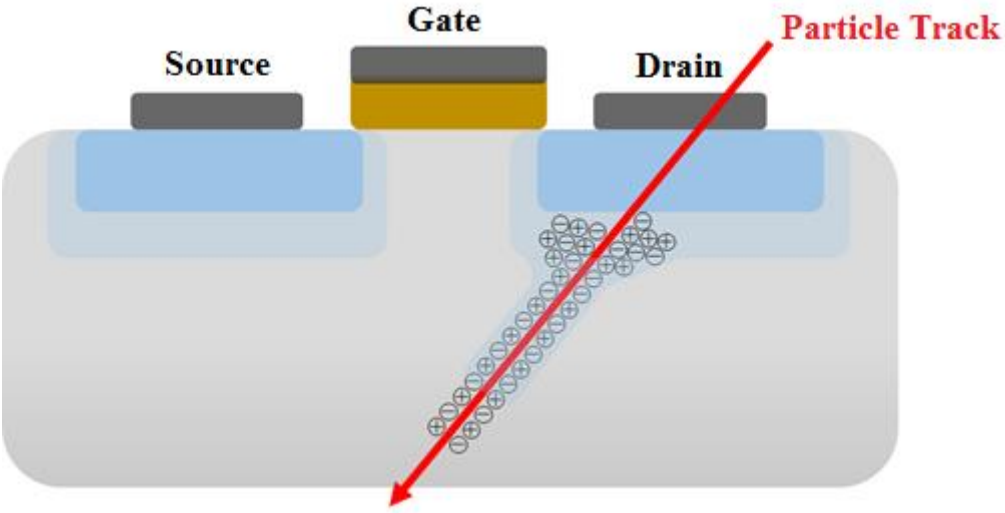

Figure. 2.6 Illustration of the SEE damage.

2.1.4 Previous SRAM Cell Designs for Radiation Tolerance

2.1.4.1 Quatro SRAM Cell

They propose a 10T soft error robust SRAM cell that offers differential read operation for robust sensing [4]. This SRAM cell is named as quad-node 10T or Quatro-10T cell. As shown in Fig. 2.7, the Quatro SRAM cell uses ten transistors and four data nodes. In addition, there are two access transistors, N5 and N6. If the stored data is '1', the logic values at nodes S1, S2, S3, and S4 are '1', '0', '0', and '1', respectively. According to their claim, the Quatro SRAM cell reduces soft errors by 98% lower than the conventional 6T SRAM cell [4].

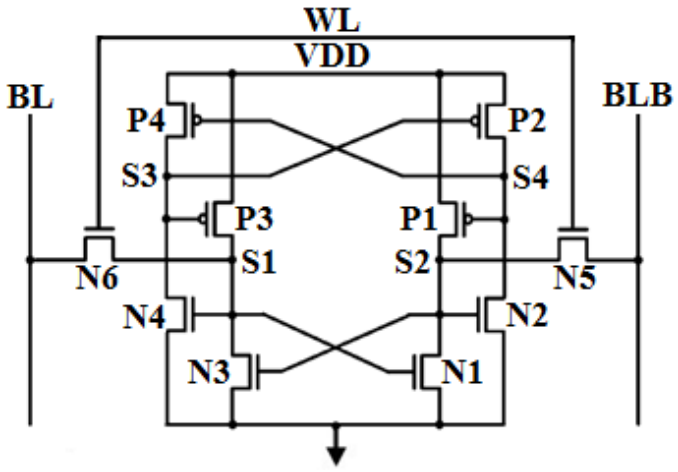

Figure. 2.7 Structure of the Quatro SRAM cell.

2.1.4.2 We-Quatro SRAM Cell

Their previous study shows that the Quatro SRAM cell suffers from poor writability [5]. So they present a new radiation hardened SRAM cell, "we-Quatro". "we" means "writability enhances". As shown in Fig. 2.8, they add two access transistors to the Quatro SRAM cell to obtain strong writability. Therefore, the we-Quatro SRAM cell has twelve transistors. Although the we-Quatro SRAM cell use more transistors, they occupy the same area as the Quatro SRAM cell. When the stored data is '0', the logic values at nodes S1, S2, S3, and S4 are '0', '1', '1', and '0', respectively [5].

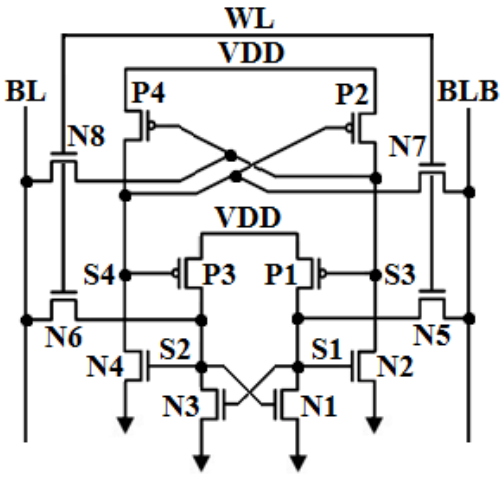

Figure. 2.8 Structure of the we-Quatro SRAM cell.

2.1.4.3 Dice SRAM Cell

Dual interlocked storage cell (DICE) is widely used in radiation hardened SRAM. Unlike the structure of the conventional 6T SRAM cell, it has an interlock structure in which one memory node is input to PMOS and NMOS of different inverters. As shown in Fig. 2.9, the DICE SRAM cell use twelve transistors. Therefore, they occupy more area than the 6T SRAM, Quatro SRAM, and we-Quatro SRAM cell. The DICE SRAM cell uses a 4-node redundant structure and these nodes store the data as opposite values of two pairs [6]. (i.e., 0101 or 1010)

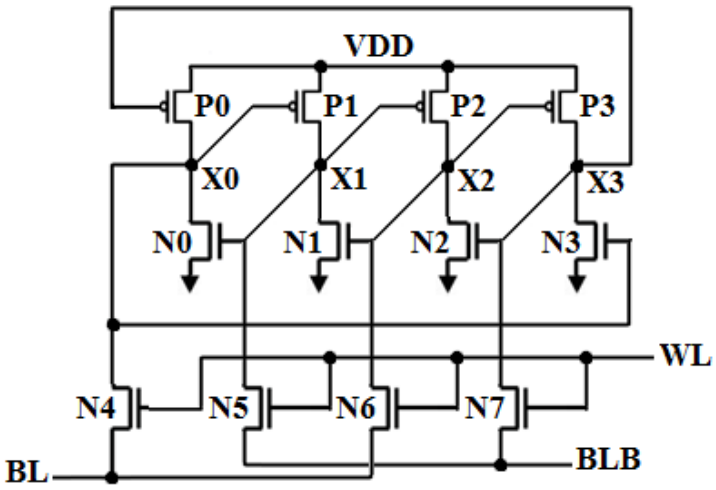

Figure. 2.9 Structure of the DICE SRAM cell.

3. Proposed SRAM Cell

3.1 C-SRAM

Many radiation-hardened SRAM cells such as the Quatro SRAM cell, we-Quatro SRAM cell, and DICE SRAM cell have been reported for years. However, these designs have the disadvantage of taking up more area than the conventional 6T SRAM cell. The Quatro SRAM cell uses 10 transistors. Likewise, the DICE SRAM cell and we-Quatro SRAM cell consist of 12 transistors.

I propose a new radiation hardened SRAM cell design named as C-SRAM. The C-SRAM is simply added a capacitor to the conventional 6T SRAM. It was designed to mitigate radiation effect using a conservation law of electrical charge. I used metal-cap by stacking several layers of metal without using the capacitor provided by the 0.18 μm CMOS process. Therefore, a cell size of the C-SRAM is the same as the 6T SRAM cell, as shown in Fig. 3.1 and Fig. 3.2.

Figure. 3.1 Illustration of the metal-cap.

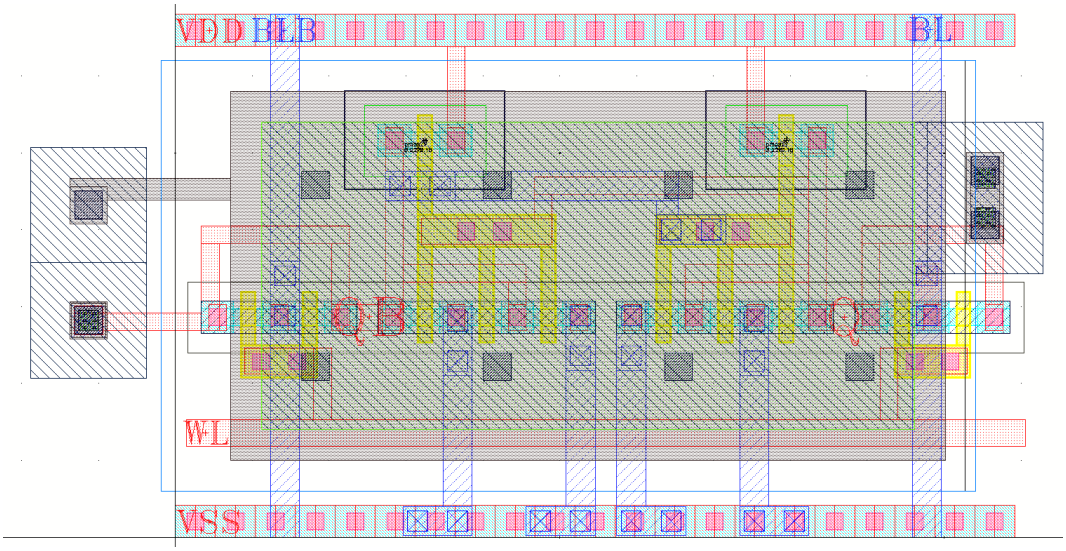

Figure. 3.2 Layout of the C-SRAM cell.

4. Experiment Results of C-SRAM

4.1 Simulation Test result

4.1.1 Static Noise Margin

The SNM is an indicator of operational stability. Therefore, the SNM is widely used to evaluate the stability of the SRAM cell [13]. As shown in Fig. 4.1 and Fig. 4.2, these are the conceptual setup of modeling SNM [14], [15]. The SNM is defined as the value of dc noise voltage "V_N" that is added to the data node before the data is flipped. As V_N continues to increase, cell stability will gradually decrease.

To validate the SNM of the 6T SRAM cell and C-SRAM cell, I use the dc noise voltage. The SNM can be observed in the read, write, and hold mode. As a result, the SNMs are equal to the 6T SRAM values in 530mV (hold mode), 220mV (read mode), and 860mV (write mode) as shown in Fig. 4.3 and Fig. 4.4. It shows that even if a capacitor is added, it does not affect the operation. Furthermore, since the read and write operations are trade-off relationships, a relatively large write

SNM value is obtained instead of a small read SNM value. However, SNM has a drawback in that it does not capture the dynamic behavior of SRAM operation [16], [17]. Therefore, additional dynamic noise margin (DNM) experiment is conducted using the pulse width of WL and capacitance of BL/BLB. As a result, it is confirmed that the read DNM value and the write DNM value of the C-SRAM are 630 mV and 590 mV, respectively.

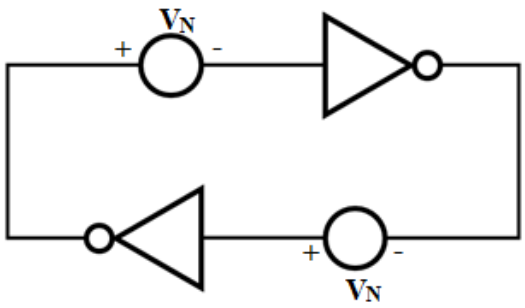

Figure. 4.1 The conceptual setup of modeling SNM (block diagram).

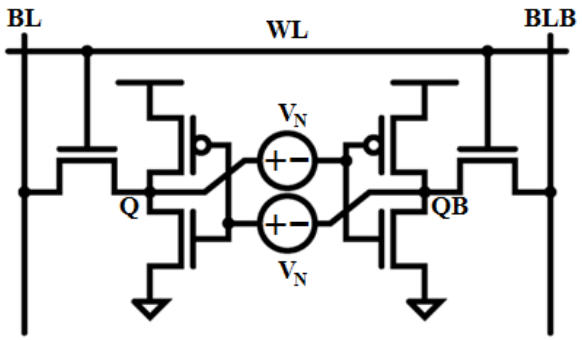

Figure. 4.2 The conceptual setup of modeling SNM (schematic).

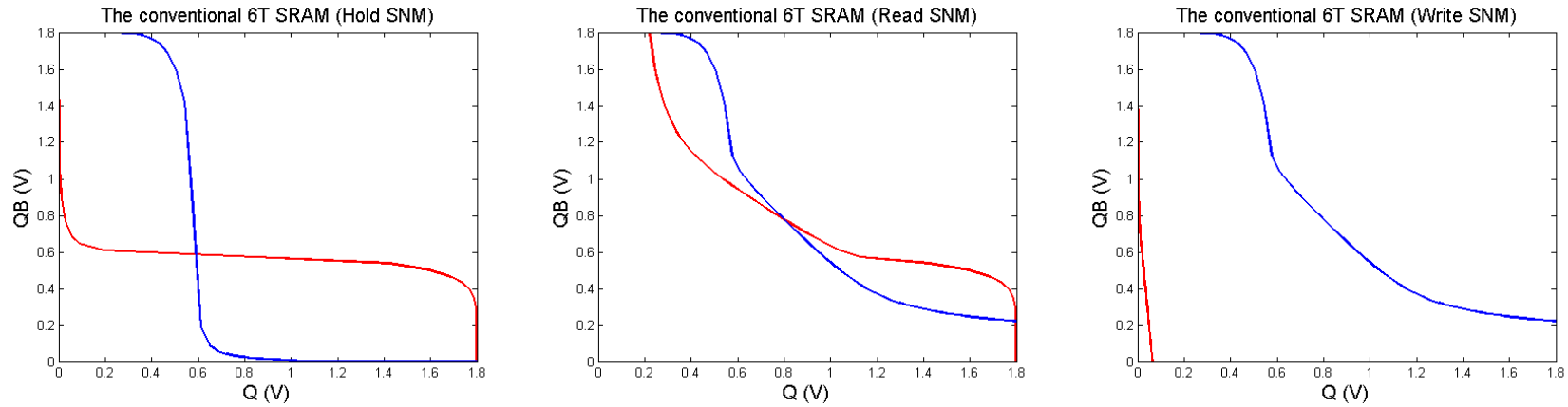

Figure. 4.3 The SNMs of the conventional 6T SRAM: 530mV (hold mode), 220mV (read mode), and 860mV (write mode).

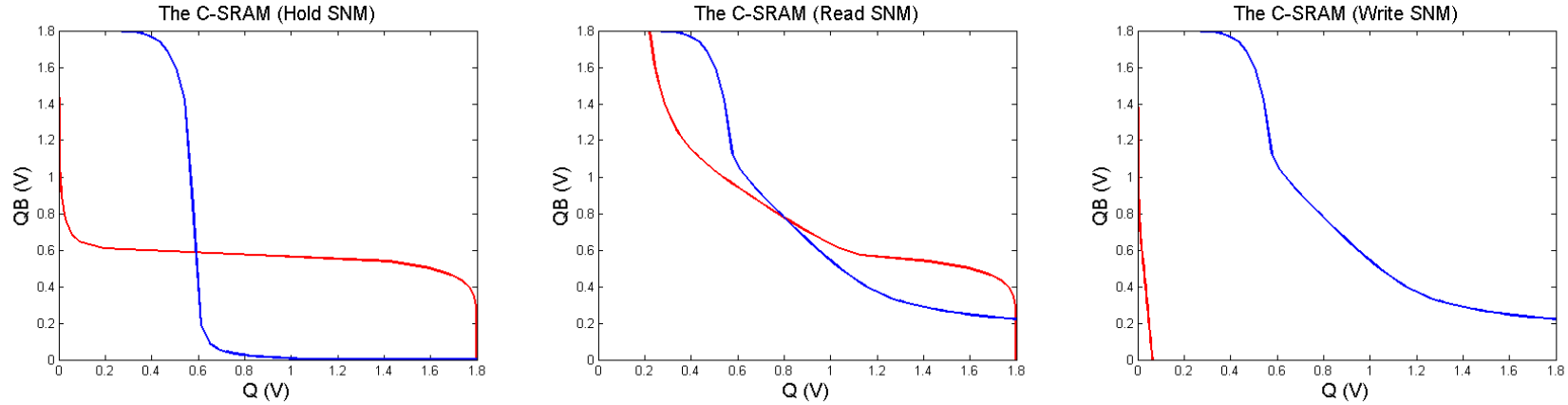

Figure. 4.4 The SNMs of the C-SRAM: 530mV (hold mode), 220mV (read mode), and 860mV (write mode).

4.1.2 SEU test

To prove the radiation tolerance of my cell design, I conducted a simulation test of SEU. As shown in Fig. 4.5, a current source is employed to the sensitive node for simulating the radiation effect on the SRAM cell [18]. As mentioned in [18], [19], a positive transient pulse is generated when the drain of PMOS is affected by radiation. On the other hand, a negative transient pulse is generated in the drain of NMOS. For this reason, the Q and QB are sensitive nodes in the conventional 6T SRAM cell structure. In the paper [18] and [20], a double exponential current source was used to simulate the SEU on sensitive nodes. And the parameter values of τ_α and τ_β were set to 164 ps and 50 ps.

I experimented using this setting value. And I compared each cell by applying a ratio similar to the conventional 6T SRAM cell size I designed in this paper. The injected current can be expressed as

$$I_{inj}(t) = I_{peak}(e^{\frac{-t}{\tau_\alpha}} - e^{\frac{-t}{\tau_\beta}}) \quad (1)$$

$$I_{peak} = \frac{Q}{\tau_\alpha - \tau_\beta} \tag{2}$$

where I_{peak} is approximately the peak current, τ_β is the rise time constant and τ_α is the fall time constant [18]-[20].

Critical charge (Qc) is the minimum value of charge that must be collected at the sensitive node to flip the bit [18], [19]. As a result, Qc of the conventional 6T SRAM is 51.984 fC, C-SRAM is 247.494 fC, Quatro and we-Quatro SRAM are 52.668 fC, and DICE SRAM is more than 300 fC. In addition, I converted this Qc value to an LET value with the following equation.

$$Q_C = \frac{L_{th} \times T \times d \times e}{X} \tag{3}$$

where L_{th} is a threshold LET value, T is a thickness, d is a Si density, e is an electronic charge, and X is an energy needed to create one e-h pair [21]. Here, T is the n-well thickness of 1um in the figure of paper [22]. As a result, the LET value of C-SRAM is 24.029 MeV•cm2/mg. This value is approximately 4.76x more than

the 5.047 MeV•cm2/mg of the conventional 6T SRAM. And this simulation results demonstrate that C-SRAM is superior to the conventional 6T SRAM.

Each comparison value is summarized in the Table 4-1 for ease of understanding [1], [20]. Of course, it may be confirmed that the 12T DICE SRAM cell is the best performance in the SEU test. However, considering the area, it is expected that C-SRAM will be used a lot. This is because it shows good radiation tolerance performance without increasing size from the conventional 6T SRAM cell.

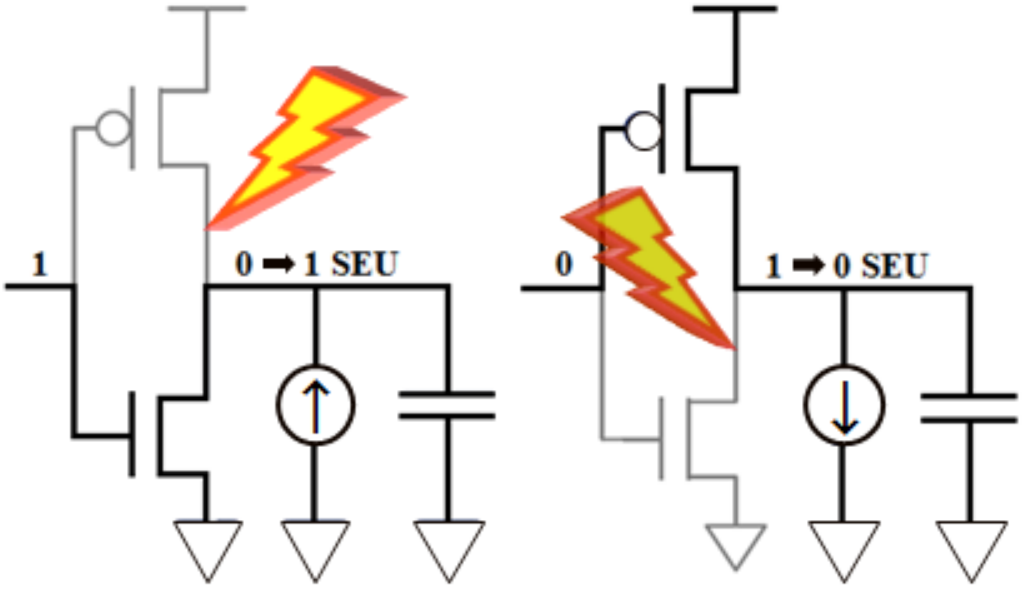

Figure. 4.5 The current source model for simulating the radiation effect.

Table 4-1. Comparisons between C-SRAM and other considered cells

	C-SRAM cell	Conventional 6T SRAM cell	DICE SRAM cell	Quatro SRAM cell	we-Quatro SRAM cell
Transistors	6	6	12	10	12
Relative Static Power	1	1	2	2	2
Relative Area	1	1	2.414	1.958	1.958
Qc (fC)	247.494	51.984	> 300	52.668	52.668
Max SEE Current Model (mA)	2.171	0.456	> 2.632	0.462	0.462
LET (MeV•cm²/mg)	24.029	5.047	> 29.126	5.113	5.113
Hold SNM (mV)	530	530	517	625	625
Read SNM (mV)	220	220	225	250	233
Write SNM (mV)	860	860	900	922	900
Read DNM (mV)	630	590	720	700	700
Write DNM (mV)	590	580	no fail	660	no fail

4.2 Irradiation Test Results

4.2.1 SEU Test

The chips of the conventional 6T SRAM and C-SRAM were fabricated in commercial 0.18 μm CMOS technology. And these chips were bonded to a printed circuit board (PCB) in a form of chip on board (COB). There are three boards: DUT, CTRL, and TRANS boards as shown in Fig. 4.6. In particular, the TRANS board is an additional board necessary for the use of ion beam facility. A total of four chips are placed on one DUT board, with two conventional 6T SRAM chips and two C-SRAM chips. The reason for this setting is to obtain a lot of data under the same experimental condition. For the I/O ports, LAN ports are used in consideration of the area of the DUT board. The CTRL board uses arduino mega, and similarly, LAN ports are used as I/O ports. Moreover, supply bus transceivers are used to compatible the voltage of arduino with the operation VDD of the chip.

The experiment is conducted by sequentially writing data in Q of each WLs and reading the value again. And if the bit is inverted during this experiment, I assume that an error has occurred.

The conventional 6T SRAM and C-SRAM have been tested at the proton accelerator facility (Fig. 4.7), Korea Atomic Energy Research Institute (KAERI), with energy levels of 45 MeV and 100 MeV. The applied fluence is $1x10^{11}$ particles/cm^2. As a result, no error occurred at 100 MeV, but one error occurred at 45 MeV in the conventional 6T SRAM (Fig. 4.8). It may seem strange that an error occurred at a relatively lower energy level. In this part, referring to the figure in the web site [23], it can be seen that the LET value of the proton decreases as the energy increases. For this reason, an error occurred at a relatively lower energy level of 45 MeV. In the proton accelerator experiment, one error out of 8,424 data was found in the conventional 6T SRAM. This result shows that the C-SRAM is superior to the 6T SRAM.

Additionally, both the conventional 6T SRAM and C-SRAM have been tested with H ions at the ion beam facility (Fig. 4.9), KAERI, with an energy level of 150 keV and the fluence of $1x10^{17}$ particles/cm^2. The ion beam facility uses a vacuum

chamber, so I needed feedthrough. For the ion beam experiment, the DUT board was newly designed and the TRANS board was also newly manufactured (Fig. 4.10). As a result of the experiment, there were no errors in both the conventional 6T SRAM and C-SRAM. Unfortunately, the reason is that the LET value under the corresponding conditions is about 0.46 MeV•cm2/mg, which is too small for bit to flip.

I conducted each experiment at KAERI's proton accelerator facility and ion beam facility to examine the SEU effect of SRAM. And this simulation results demonstrate that C-SRAM is superior to the 6T SRAM.

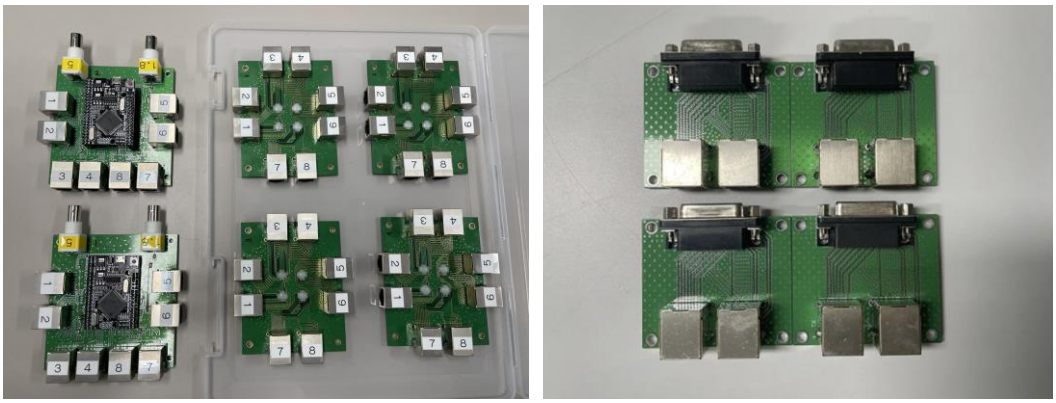

Figure. 4.6 The boards of DUT, CTRL (left), and TRANS (right).

Figure. 4.7 The proton accelerator facility at KAERI.

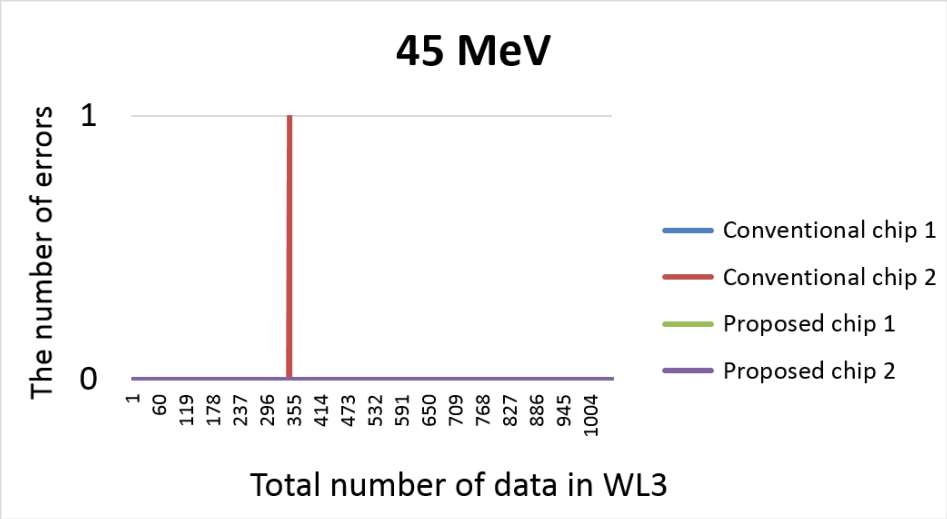

Figure. 4.8 The number of errors on the DUT board at energy level 45 MeV.

Figure. 4.9 The ion beam facility at KAERI.

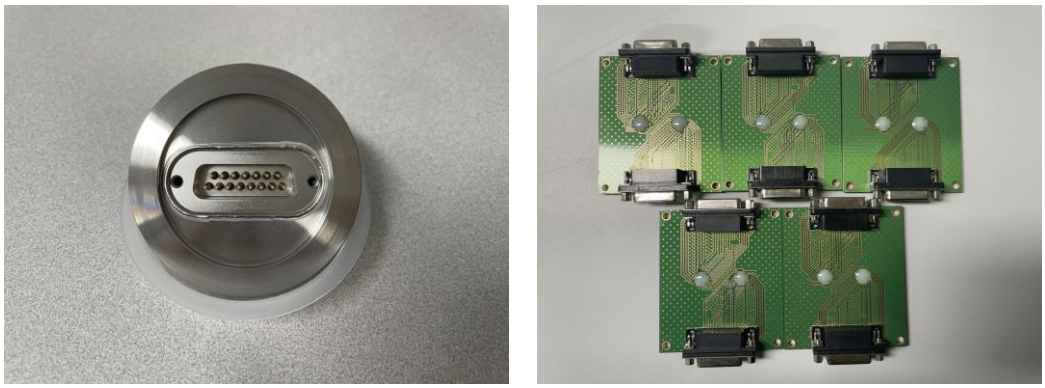

Figure. 4.10 The feedthrough (left) and new DUT board (right).

5. Conclusion

For memory semiconductor devices such as SRAM, soft errors must be considered for harsh radiation environments. So, I design a new radiation hardened SRAM cell which is simply added a capacitor to a conventional 6T SRAM. This proposed SRAM uses metal-cap by stacking several layers of metal without using the capacitor provided by the 0.18 μm CMOS process. Therefore, a cell size of the C-SRAM is the same as the 6T SRAM.

SNMs, which are indicators of operational stability, are equal to the 6T SRAM values in 530mV (hold mode), 220mV (read mode), and 860mV (write mode). It shows that even if a capacitor is added, it does not affect the operation. However, SNM has a drawback in that it does not capture the dynamic behavior of SRAM operation. Therefore, additional DNM experiment is conducted using the pulse width of WL and capacitance of BL/BLB. As a result, it is confirmed that the read DNM value and the write DNM value of the C-SRAM are 630 mV and 590 mV, respectively.

In the simulation test of the SEU, the result is better than the 6T SRAM with the value of 247.494 fC. In addition, the LET value of C-SRAM is 24.029 MeV•cm2/mg. This value is approximately 4.76x more than the 5.047 MeV•cm2/mg of the 6T SRAM. The simulation results show that C-SRAM has better radiation tolerance than the 6T SRAM.

Furthermore, I conducted each experiment at KAERI's proton accelerator facility and ion beam facility to examine the SEU effect of SRAM. The 6T SRAM and C-SRAM have been tested at the proton accelerator facility with energy levels of 45 MeV, 100 MeV and the fluence of $1x10^{11}$ particles/cm^2. As a result, no error occurred at 100 MeV, but one error occurred at 45 MeV in the 6T SRAM. Additionally, both the conventional 6T SRAM and C-SRAM have been tested with H ions at the ion beam facility with an energy level of 150 keV and the fluence of $1x10^{17}$ particles/cm^2. However, there were no errors in both the conventional 6T SRAM and C-SRAM. Unfortunately, the reason is that the LET value of the condition is too small to flip the bit.

The results of these simulations and irradiation experiments show that C-SRAM is superior to the conventional 6T SRAM comprehensively.

Here is something to watch out for. Metal cap proposed in this thesis used layer 5 and 6. Therefore, care should be taken when using a different metal line above the C-SRAM cell.

References

[1] S. Pal, D. D. Sri, W. -H. Ki and A. Islam, "Highly Stable Low Power Radiation Hardened Memory-by-Design SRAM for Space Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 6, pp. 2147-2151, June 2021, doi: 10.1109/TCSII.2020.3042520.

[2] L. D. Trang Dang, M. Kang, J. Kim and I. -J. Chang, "Studying the Variation Effects of Radiation Hardened Quatro SRAM Bit-Cell," in IEEE Transactions on Nuclear Science, vol. 63, no. 4, pp. 2399-2401, Aug. 2016, doi: 10.1109/TNS.2016.2590426.

[3] J. Wang, J. Prinzie, A. Coronetti, S. Thys, R. G. Alia and P. Leroux, "Study of SEU Sensitivity of SRAM-Based Radiation Monitors in 65-nm CMOS," in IEEE Transactions on Nuclear Science, vol. 68, no. 5, pp. 913-920, May 2021, doi: 10.1109/TNS.2021.3072328.

[4] S. M. Jahinuzzaman, D. J. Rennie and M. Sachdev, "A Soft Error Tolerant 10T SRAM Bit-Cell With Differential Read Capability," in IEEE Transactions on

Nuclear Science, vol. 56, no. 6, pp. 3768-3773, Dec. 2009, doi: 10.1109/TNS.2009.2032090.

[5] L. D. Trang Dang, J. S. Kim and I. J. Chang, "We-Quatro: Radiation-Hardened SRAM Cell With Parametric Process Variation Tolerance," in IEEE Transactions on Nuclear Science, vol. 64, no. 9, pp. 2489-2496, Sept. 2017, doi: 10.1109/TNS.2017.2728180.

[6] T. Calin, M. Nicolaidis and R. Velazco, "Upset hardened memory design for submicron CMOS technology," in IEEE Transactions on Nuclear Science, vol. 43, no. 6, pp. 2874-2878, Dec. 1996, doi: 10.1109/23.556880.

[7] M. S. M. Siddiqui, S. Ruchi, L. Van Le, T. Yoo, I. Chang and T. T. Kim, "SRAM Radiation Hardening Through Self-Refresh Operation and Error Correction," in IEEE Transactions on Device and Materials Reliability, vol. 20, no. 2, pp. 468-474, June 2020, doi: 10.1109/TDMR.2020.2994769.

[8] J. R. Schwank et al., "Radiation Effects in MOS Oxides," in IEEE Transactions on Nuclear Science, vol. 55, no. 4, pp. 1833-1853, Aug. 2008, doi: 10.1109/TNS.2008.2001040.

[9] H. J. Barnaby, "Total-Ionizing-Dose Effects in Modern CMOS Technologies," in IEEE Transactions on Nuclear Science, vol. 53, no. 6, pp. 3103-3121, Dec. 2006, doi: 10.1109/TNS.2006.885952.

[10] P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," in IEEE Transactions on Nuclear Science, vol. 50, no. 3, pp. 583-602, June 2003, doi: 10.1109/TNS.2003.813129.

[11] J. R. Schwank, V. Ferlet-Cavrois, M. R. Shaneyfelt, P. Paillet and P. E. Dodd, "Radiation effects in SOI technologies," in IEEE Transactions on Nuclear Science, vol. 50, no. 3, pp. 522-538, June 2003, doi: 10.1109/TNS.2003.812930.

[12] P. E. Dodd, M. R. Shaneyfelt, J. R. Schwank and J. A. Felix, "Current and Future Challenges in Radiation Effects on CMOS Electronics," in IEEE Transactions on Nuclear Science, vol. 57, no. 4, pp. 1747-1763, Aug. 2010, doi: 10.1109/TNS.2010.2042613.

[13] S. S. Dohar, S. R. K., V. M. H. and N. K. Y. B., "A 1.2 V, Highly Reliable RHBD 10T SRAM Cell for Aerospace Application," in IEEE Transactions on Electron

Devices, vol. 68, no. 5, pp. 2265-2270, May 2021, doi: 10.1109/TED.2021.3064899.

[14] E. Seevinck, F. J. List and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," in IEEE Journal of Solid-State Circuits, vol. 22, no. 5, pp. 748-754, Oct. 1987, doi: 10.1109/JSSC.1987.1052809.

[15] B. H. Calhoun and A. P. Chandrakasan, "A 256-kb 65-nm Sub-threshold SRAM Design for Ultra-Low-Voltage Operation," in IEEE Journal of Solid-State Circuits, vol. 42, no. 3, pp. 680-688, March 2007, doi: 10.1109/JSSC.2006.891726.

[16] D. Khalil, M. Khellah, N. Kim, Y. Ismail, T. Karnik and V. K. De, "Accurate Estimation of SRAM Dynamic Stability," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 16, no. 12, pp. 1639-1647, Dec. 2008, doi: 10.1109/TVLSI.2008.2001941.

[17] S. O. Toh, Z. Guo, T. K. Liu and B. Nikolic, "Characterization of Dynamic SRAM Stability in 45 nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 46, no. 11, pp. 2702-2712, Nov. 2011, doi: 10.1109/JSSC.2011.2164300.

[18] S. Pal, D. D. Sri, W. -H. Ki and A. Islam, "Highly Stable Low Power Radiation Hardened Memory-by-Design SRAM for Space Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 68, no. 6, pp. 2147-2151, June 2021, doi: 10.1109/TCSII.2020.3042520.

[19] S. Pal, S. Mohapatra, W. -H. Ki and A. Islam, "Soft-Error-Immune Read-Stability-Improved SRAM for Multi-Node Upset Tolerance in Space Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 68, no. 8, pp. 3317-3327, Aug. 2021, doi: 10.1109/TCSI.2021.3085516.

[20] J. Jiang, Y. Xu, W. Zhu, J. Xiao and S. Zou, "Quadruple Cross-Coupled Latch-Based 10T and 12T SRAM Bit-Cell Designs for Highly Reliable Terrestrial Applications," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 3, pp. 967-977, March 2019, doi: 10.1109/TCSI.2018.2872507.

[21] "Critical Charge and Threshold LET." the CRÈME site. last modified June 03, 2022, accessed May 25, https://creme.isde.vanderbilt.edu/CREME-MC/help/critical-charge-and-threshold-let.

[22] B. Ciftcioglu et al., "Integrated Silicon PIN Photodiodes Using Deep N-Well in a Standard 0.18-μ m CMOS Technology," in Journal of Lightwave Technology, vol. 27, no. 15, pp. 3303-3313, Aug.1, 2009, doi: 10.1109/JLT.2008.2008664.

[23] "Single Event Upset Test Facility." BNL Homepage. last modified June 03, 2022, accessed April 06, https://www.bnl.gov/tandem/capabilities/seu.php.

국문요약

내방사선 C-SRAM의 SNM과 SEU 영향 분석

연세대학교 대학원

전기전자공학과

조 은 주

본 논문은 내방사선 C-SRAM의 SNM과 SEU 영향 분석에 관한 것이다. 우주 환경에서 SRAM과 같은 메모리 반도체의 주된 문제는 소프트 에러이다. 이러한 소프트 에러는 비트 플립을 유발하며 이러한 이벤트를 SEU라고 한다.

Quatro SRAM 셀, we-Quatro SRAM 셀, 그리고 DICE SRAM 셀과 같은 다양한 내방사선 SRAM 셀들이 수년간 보고되어왔다. Quatro SRAM 셀은 10개의 트랜지스터를 사용한다. 마찬가지로 DICE SRAM 셀과 we-Quatro SRAM 셀은 12개의 트랜지스터로 구성된다.

그러나 이러한 설계 방식은 기존의 6T SRAM 셀보다 더 많은 면적을 차지한다는 단점이 있다. 또한, 트랜지스터 개수를 가지고 새로운 내방사선 SRAM 셀 디자인을 제안하는 방식은 이미 포화되었다고 생각한다.

그래서 우리는 C-SRAM이라는 새로운 내방사선 SRAM 셀을 제안한다. C-SRAM은 단순히 기존의 6T SRAM 구조에 커패시터 하나를 추가한 형태이다. 전하 보존 법칙을 사용하여 방사선 효과를 완화시키도록 설계했다. 뿐만 아니라, 공정에서 제공하는 커패시터를 사용하지 않고 메탈을 여러 층 겹쳐 metal-cap을 만들어 사용했다. 그렇기 때문에, 셀 크기는 기존의 6T SRAM 셀과 차이 없이 동일하다.

동작 안정성의 지표인 SNM은 홀드 모드, 읽기 모드, 그리고 쓰기 모드에서 각각 530mV, 220mV, 그리고 860mV 값으로 기존 6T SRAM 값과 동일하다. 특히, 읽기 모드에서의 SNM과 쓰기 모드에서의 SNM 값은 서로 trade-off 관계이다. 그래서 상대적으로 적은 읽기 SNM을 얻은 대신 비교적 좋은 쓰기 SNM 값을 얻은 것을 확인할 수 있다.

SEU의 시뮬레이션 테스트에서는 이중 지수 전류원을 가지고 모델링하였고, 247.494 fC의 값으로 기존의 6T SRAM보다 4.761배 더 우수한 결과를 얻었다. 또한 추가적으로 실제 조사 실험을 진행하였다. 한국원자력연구원의 양성자가속기 시설과 이온빔 시설을 이용해서 다양한 실험을 진행하였다. 이러한 실험을 통해 C-

SRAM 셀이 기존의 6T SRAM 셀보다 우수하다는 것도 입증할 수 있었다. 여기서, 기존의 6T SRAM 칩과 C-SRAM 칩은 표준 0.18 μm CMOS 공정을 사용하여 설계되었다.

Keywords: SNM, 소프트 에러, 방사선 영향, 내방사선 SRAM, C-SRAM, 양성자 가속기 시설, 이온빔 시설