A Study on the Characteristics of a Novel 0.1μm Asymmetric MOSFET

연세대학교 대학원

전기·전자공학과

최 창 순

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지도 최 우 영 교수

이 논문을 석사 학위논문으로 제출함

2000 년 12 월 일

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최창순의 석사 학위논문을 인준함

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A Study on the Characteristics of a Novel 0.1mm Asymmetric MOSFET

By

Chang-Soon Choi

Submitted to the Department of Electrical and Electronic Engineering

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at the

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The Graduate School

YONSEI University

Seoul, KOREA

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감사의 글

우선 이 논문을 쓰기까지 많은 도움을 주셨던 모든 분들에게 감사드립니다. 학부와 대학원 생활동안 많은 학문적 가르침을 주신 최우영 교수님께 우선 감사의 마음을 전하고 싶습니다. 또한 논문에 대한 많은 지도와 더불어 새로운 분야에 대한 관심을 넓혀주신 물리학과 임성일 교수님께도 깊은 감사를 드립니다. 본 논문을 자상하게 지도해주시고 수업시간을 통하여 많은 가르침을 주신 이상렬 교수님께도 감사드립니다. 그리고 본인의 연구분야에 대한 폭넓은 이해를 바탕으로 대학원 생활동안 많은 수업을 통해 학문적 관심을 넓혀주셨던 김봉렬 교수님께도 깊이 감사드립니다.
길지 않은 학부생활동안 전자공학이라는 생소한 분야를 좀 더 친숙하게 대할 수 있도록 지도해주신 박규태 교수님, 차일환 교수님, 이문기 교수님, 이용석 교수님, 박민용 교수님, 윤대희 교수님, 김재희 교수님, 이재용 교수님, 홍대식 교수님, 송홍엽 교수님, 이철희 교수님, 강문기 교수님, 한건희 교수님께도 감사의 말씀을 올립니다.
제가 2년동안의 세월을 보낸 우리 연구실 모든 사람들, 정말 감사합니다. 여러분들이 있기에 저는 힘든 대학원 생활을 견뎌나갔다고 생각합니다. 이미 졸업해서 ETRI에 계신 우리 연구실의 영원한 맏형, 태식이형, 형수님이랑 희진이랑 오래오래 행복하세요. 그리고 본 논문을 가장 많이 도와주시고 자상하게 지도해주신 우리 팀장 경환이형, 우리는 멋진 한팀이었다고 생각합니다. 빨리 결혼하세요. 연구분야에 대한 열정이 돋보이는 승우형, 집에 가는 길이 형 덕분에 유익한 시간이었습니다. 자주는 못 뵈었지만 자상하신 정태형, 언제나 행복하세요. 연구에 대한 폭넓은 이해와 자상한 성격으로 연구실을 이끌어 가주시는 용상이 형, 결혼생활 행복하세요. 우리 연구실의 위상을 전자공학과 내에서도 돋보이도록 만든 유근이 형, 형은 제가 정말 친형처럼 따르고 있는 거 아시죠? 언제나 연구를 열심히 하는 영광이형, 몸도 좀 아껴가세요. 그리고 대학원 입학동기인 멋쟁이 혁기형, 유학 가서도 저를 잊지 마세요. 또한 대학원 동기이며 많은 취미생활을 함께 즐긴 재욱이형, 다행이에요. 형이 박사과정을 올라가신다니. 그리고 숱한 선배의 타박을 받아주며 일을 정말로 잘해준 우리 막내 준혁, 기혁 형제, 앞으로 연구실은 너희들이 어떻게 하느냐에 달린거 같다. 앞으로도 잘 부탁한다. 이미 졸업하신 명수형, 성훈이 형, 그리고 2년전에 졸업해서 현대전자에 같이 가셨던 민우형, 세은이형, 용호형에게도 진심으로 감사하다는 말을 전하고 싶습니다.
옆방에서 많은 도움을 주셨던, 동렬이형을 비롯한 CAD2 연구실, 성우형, 용권이형

을 비롯한 CAD1연구실 사람들에게도 고맙다는 말을 전하고 싶습니다.
학부때 공대도서관에서 4년의 세월을 같이 보냈던 우리 입학동기, 인표, 병준, 현초, 수현, 현석, 재연, 수현, 학범, 승국, 용훈, 점군, 민수의 도움도 잊지 않을 것입니다. 또한 99년에 전자과를 졸업하면서 독실한 우애를 다졌던 종호형, 학무형, 원배형, 근일이형, 준환이형, 현민이형, 진동이형, 병조형, 욱민이형, 세준이형, 태훈이형, 지상이형과의 즐거웠던 추억을 영원히 기억할 것입니다.
최고의 친구라고 감히 말할 수 있는 중학교 3학년때 친구들 경식,재우,정석,성진,현수,주현 그리고 범생이들 같은 중학교 2학년때 친구들, 엄한 고등학교 생활을 견딘 우리 친구들, 모두의 도움으로 힘든 대학원 생활을 마칠 수 있었던 것 같습니다. 정말로 고마운 마음 말해주고 싶습니다. 또한 기웅이형과 기원이형, 기동이형을 비롯한 고등학교 선후배 님들에게도 고맙다는 말 꼭 전하고 싶습니다.
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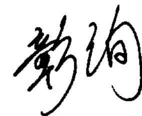
본 논문이 끝나면서 저의 박사과정의 생활은 시작이 될 것입니다. 많이 힘들고 어려운 길이겠지만 여러분들이 있기에 저는 꾸준히 연구를 할 수 있을 것 같습니다. 다시 한번 저의 주위에서 지켜 봐주시고 격려해주신 모든 분들에게 고개 숙여 깊이 감사드립니다.

이천년 십이월십구일 밤 연구실에서

최 창 순



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Abstract

A Study on the Characteristics of a Novel 0.1mm Asymmetric MOSFET

by

Chang-Soon Choi

at the

Department of Electrical and Electronic Engineering

The Graduate School

Yonsei University

The difficulties, limitations and some physical phenomena of deep sub-micrometer MOSFET are explained based on the previous research, and several structural approaches for overcoming such limitations is described. With asymmetric MOSFET, the improvement of device performance without sacrificing short channel characteristics and reliability are achieved. The design difficulties of asymmetric MOSFETs in 0.1μm regimes are also examined. In order to reduce these design difficulties, a new doping scheme, Self-Aligned Asymmetric Structure (SAAS), is proposed for 0.1μm MOSFET technology and its device characteristics are analyzed. The proposed structure

enables the source, drain and channel to be designed independently without additional lithography steps. SAAS with lateral asymmetric channel and highly doped source extension improves driving capability and short channel behavior without sacrificing hot carrier reliability. Based on the results of hydrodynamic device simulation over a wide range of process conditions, it is shown that highly doped asymmetric halo provides enhanced velocity overshoot and suppressed drain-induced barrier lowering (DIBL). By employing asymmetric highly doped source extension, the degradation of driving capability is suppressed that can be caused by the increased parasitic resistance in highly doped asymmetric halo.

Keywords: MOSFET, Asymmetric structure, Self-Aligned,
Velocity overshoot, Device simulation, Scaling CMOS,
Short channel effect, halo doping

Chapter 1. Introduction

For more than 30 years, silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET) device technologies have been improved at a dramatic rate. A large part of the success of MOSFET device is due to the fact that it can be scaled to increasingly smaller dimensions, which results in high performance and integration. The ability to improve performance consistently while decreasing power consumption has made Complementary MOS (CMOS) architecture the dominant technology for integrated circuits (IC). The scaling of the CMOS transistor has been primary factor for improving device performance in IC [1].

As device dimensions have been continuously reduced, the scaling of MOSFET approaches the physical limits associated with device characteristics as referred in Table 1. In 0.1μm regime and below, however, the non-equilibrium carrier transport has received significant attention because it is directly related to the improvement of driving capability and transconductance. As the carrier transit time becomes comparable with the energy-relaxation time, the carriers do not have enough time to reach equilibrium with the applied electric field by scattering. These phenomena described above cause the velocity overshoot and, thus the improvement of driving capability is achieved [2-3]. Another main concern of scaling down to 0.1μm regime is suppression of short channel effects [4]. Therefore, creating the shallow source/drain extension and using halo doping for improved short channel

characteristics have been used in present CMOS industry. However, the adverse effect caused by substantially increased parasitic resistance in shallow lightly doped drain (LDD) extension with halo doping severely degrades the device performance. To overcome such limitation, highly doped drain extension is required, but this gives negative influence on the hot carrier reliability and punchthrough resistance.

One attractive way to improve device performance without sacrificing reliability and short channel behavior is adopting new structures, asymmetric MOSFET structures, which have been investigated extensively in recent years [5-10]. They have an inherent advantage that source and drain regions can be designed independently, even though they need additional masks and complex layout steps. It makes the device design more suitable for improving the driving capability while maintaining the hot carrier reliability and the short channel behaviors.

Several types of asymmetric structures have been proposed and experimentally demonstrated. Asymmetric LDD structures with the heavily doped deep junction at the source side while lightly doped extension at the drain side have been proposed to reduce the parasitic resistance at the source side [5-6]. However, it is difficult to employ such structures to sub-0.1μm MOSFET because the short channel effects are worsened due to the absence of the LDD extension at the source side. Lateral Asymmetric Channel (LAC) structures have been proposed in order to take full advantage of the velocity overshoot and suppress the short channel effects [7-11]. It has non-uniform

channel doping profile with a localized pileup region next to source extension as a result of asymmetric halo. As the channel length is scaled down below 0.1μm, the asymmetric halo doping concentration must be increased in order to fully suppress Drain Induced Barrier Lowering (DIBL) and to provide the acceptable threshold voltage. However, it causes serious degradation of device performance due to the increased parasitic source resistance caused by the halo induced charge compensation [12]. In addition, the fabrication processes of previously reported asymmetric structures have poor feasibility in sub-0.1μm regime because they require additional masks and precise alignments.

In this thesis, a novel Self-Aligned Asymmetric Structure (SAAS) without the problems mentioned above and its fabrication process are presented and it is verified that the SAAS provides many advantages for improving device performance while maintaining good short channel behavior and reliability.

In Chapter 2, the investigation of scaling below 0.1μm MOSFET is described. And the previously reported MOSFET structures and asymmetric MOSFET structures, which are regarded as ultimate structures at scaling limit [4], are presented and investigated based on several papers and simulation analysis. And, advantages and disadvantages of the asymmetric structures are presented. In Chapter 3, a new structural approach, SAAS, is presented and its fabrication process is also described. In Chapter 4, the device characteristics are discussed by comparing SAAS with the previously reported asymmetric structures, and the reasons for improvement of device performance in SAAS are explained.

Table 1. The limitations for scaling MOSFET below 0.1μm

Scaling Parameter	*Values at L_G=0.1μm*	*Limiting factor for further scaling*
Gate Length	0.1μm	Cost of lithography
Junction Depth	30nm	Resistance of diffused layer
Oxide thickness	2.3nm	Direct tunneling leakage
Substrate Doping	$10^{18}cm^{-3}$	Junction leakage
Supply Voltage	1.2V	Lower limit of V_T
Threshold Voltage	0.4V	Subthreshold leakage

Chapter 2. Deep sub-micrometer MOSFET Structures: Design and Characterization

2-1. Velocity Overshoot in 0.1μm MOSFET

In recent years, extensive studies have been devoted to the 0.1μm MOSFET design and characterization [1,4]. Even though the supply voltage is continuously scaled down according to the channel length, the lateral electric field shows a large gradient in the channel from the source to the drain in 0.1μm gate dimension. The large electric field gradient causes the electron transit time to become comparable with the energy relaxation time. Therefore, the electrons do not have enough time to reach equilibrium with the lattice by insufficient phonon scattering. The phenomenon mentioned above makes the electrons to be accelerated to the velocities higher than the saturation velocity. It has been termed the velocity overshoot, which is one of the most important physical phenomena for the practical point of view because it is directly related to the improvement of driving capability in sub-0.1μm MOSFET [2-3]. Some studies have shown that experimental measurements of trans-conductance are higher than the theoretical maximum transconductance that can be reached in the case where the electron drift in equilibrium with their velocity being limited by the velocity saturation effect. Fig. 1 shows the electron velocity overshoot effect comparing with velocity saturation in 0.1μm MOSFET.

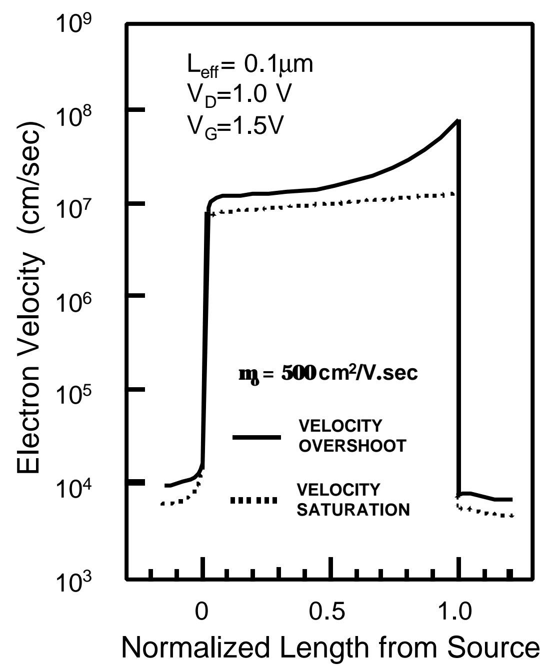


Figure 1. Average electron velocity as a function of position below $Si\text{-}SiO_2$ interface in 0.1 μm channel MOSFET.

If the velocity overshoot can be controlled, the performance of ultra-short channel MOSFET (~0.1μm) can be improved with the respect to the performance of long channel MOSFET. In order to take full advantage of velocity overshoot in 0.1μm channel, the importance of the electric field at the source end of the channel was suggested by hydrodynamic simulators [7-8]. Consequently, the velocity overshoot effect should be considered in 0.1μm MOSFET design for the improvement of device performance.

2-2. Scaling the MOSFET below 0.1mm

The scaling of silicon MOSFET channel lengths to 0.1μm and below has recently attracted great interest. Many works have been done approaching this problem from both the experimental and theoretical points of view. Several important issues must be considered when scaling MOSFET's channel length down to 0.1μm regime as follows [13-15].

(1) The short channel effects which cause severe degradation of the subthreshold characteristics and an unacceptable dependence of threshold voltage on channel length, as shown in Fig. 2.

(2) The lower limit on the threshold voltage (V_T) and supply voltage (V_{DD}) imposed by the requirement of noise immunity margins.

(3) The lower limit on oxide thickness (T_{ox}) imposed by direct tunneling which degrades the device characteristics as briefly explained in Fig. 3.

(4) The limitations due to hot carrier effects including hot carrier

generation, injection, and trapping which reduce device lifetime and reliability, as schematically shown in Fig. 4.

(5) The limitation due to band-to-band tunneling which degrades the Gate-Induced Drain leakage (GIDL) characteristics as illustrated in Fig. 5.

(6) The maximization of intrinsic device performance.

(7) The minimization of parasitic effects such as those due to parasitic resistance and capacitance associated to source/drain junction

(8) The minimization of process complexity and cost

If requirements and limitations listed in (1)-(7) are to be met, a new scaling approach are needed. The scaling of conventional structure, requiring an increase of channel doping and reduction of oxide thickness and supply voltage, is expected to become undesirable as the channel length scales below 0.1μm due to the following limitations:

1) Conventional MOSFET requires channel doping approaching or exceeding $10^{18}cm^{-3}$ in order to limit short channel effects. Such high doping concentrations are likely to cause severe degradations of device performance due to impurity scattering and reduced carrier mobility. Furthermore, the source-substrate and drain-substrate junctions become highly doped *pn* junctions and act as tunnel diodes. Thus the isolation of source/drain with substrate cannot be maintained.
2) Additional limit is imposed by (3) above. On the basis of experimental results, the ultimate lower limit for SiO_2 thickness is expected to be 2.3nm.

3) The supply voltage reduction needed in conventional structure is limited by noise immunity margins as stated in (2). In this regard, we did not investigate in details on the actual lower limit for the threshold voltage because it is dependent on specific application. For logic applications, we expect that V_{TH} = 0.3V is a lower limit for a subthreshold swing of 80-100mV/Dec [16]. On the other hand, in DRAM applications, the threshold voltage in the memory cell transistor should be around 1V regardless of feature size, density and supply voltage in order to suppress the subthreshold leakage current [17].

Thus, realization of sub-0.1μm MOSFET requires a new structural approach that improves the device performance and the short channel characteristics, while maintaining gate oxide thickness (T_{ox}), supply voltage (V_{DD}), and channel doping constant for $L_G < 0.1$μm. To overcome these limitations listed in 1)-3), several research papers have been extensively published for the development of new MOSFET structure [ref]. For the candidates of sub-0.1μm MOSFET, double gate structure, elevated source/drain structure, asymmetric structure have been proposed and experimentally demonstrated. In this thesis, the device characteristics of asymmetric structure have been focused and extensively studied using simulation methods in 0.1μm regime.

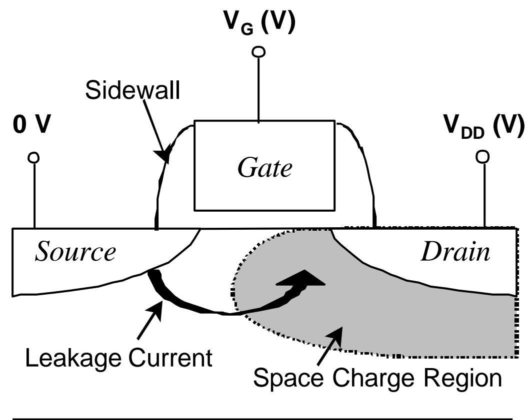


Figure 2. The cross-section of MOSFET used to explain the short channel effects (charge sharing and subthreshold leakage current).

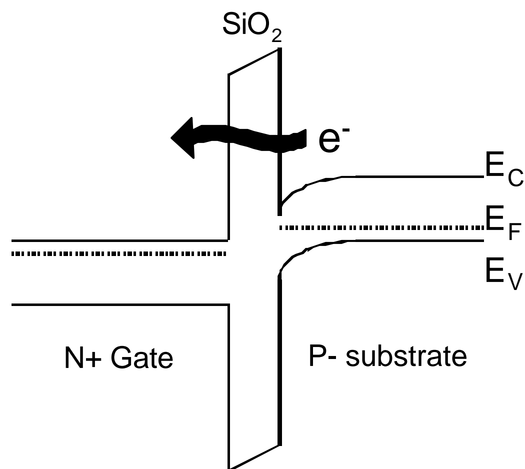


Figure 3. The direct tunneling leakage mechanism for thin gate oxide.

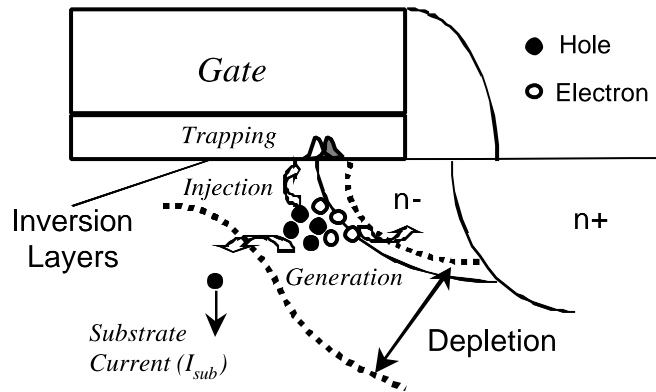


Figure 4. The mechanism of hot carrier effects, including hot carrier generation, injection, and trapping.

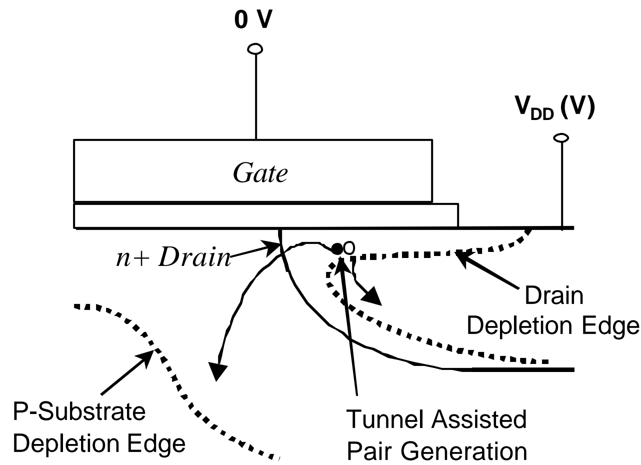


Figure 5. The mechanism of Gate-Induced Drain leakage (GIDL) in the gate-drain overlap region of MOSFET.

2-3. Novel Structures for 0.1μm MOSFET technology

2-3-1. Double gate MOSFET structure

The schematic cross-section of double gate MOSFET is shown in Fig. 6. It has the extremely shallow source/drain junctions made by the inversion layer for the suppression of short channel effects. The source/drain inversion layers is formed by the second polysilicon gate electrode placed over the first gate electrode of MOSFETs. Due to the high resistance of the source and drain layer composed of the inversion layer, the drain current is two or three orders of magnitude smaller than the conventional MOSFET, but the short channel effects can be fully suppressed because of extremely shallow source/drain junction [18]. (The depth of the junction is estimated to be 10-1nm, depending on the second gate bias.)

2-3-2. Elevated source/drain MOSFET structure

Fig. 7. shows the schematic cross-sections of several Elevated Source/Drain MOSFET structures (E-S/D) [19-21]. It has been reported that elevated source/drain is effective in allowing both junction depth reduction and leakage control of silicided junctions. Due to the small parasitic resistance at the source/drain extension, the device performance of E-S/D is superior to that of conventional MOSFET. Although E-S/D has been regarded as a candidate of the ultimate structure of MOSFET at the practical scaling limit, its process complexities, such as self-alignment problems, have delayed its

employment in deep sub-micrometer technology [19-20]. Recently, the new E-S/D shown in Fig. 7(b) was proposed in order to solve the self-alignment problems. And it was reported that the structure was very effective in the improvement of device performance without increasing GIDL current [21].

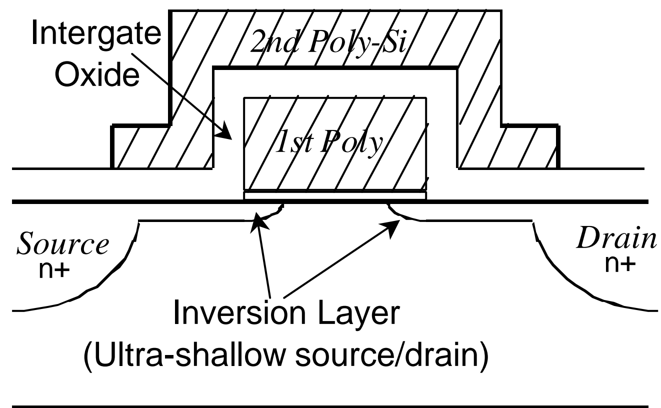
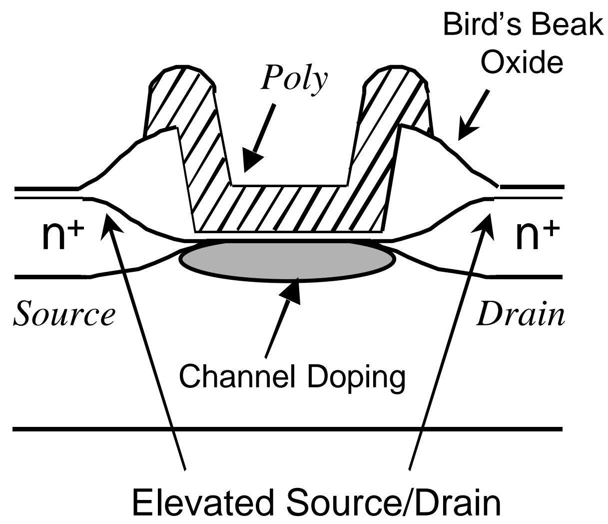


Figure 6. The double gate MOSFET structure. It is also called Electrically Junction MOSFET (EJ-MOSFET).



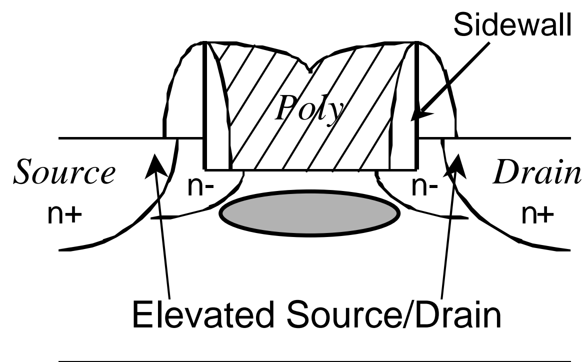


Figure 7. Two types of Elevates Source/Drain (E-S/D) MOSFET structures, (a) Gate-Recessed MOSFET (b) Self-Aligned Elevated Source/Drain MOSFET.

2-4. Asymmetric structures for 0.1μm MOSFET technology

2-4-1. Background

The most widely used device structure in a recent scaled MOSFET technology is the Lightly Doped Drain (LDD) structure which was firstly introduced in 1.25μm MOSFET. Although this gives the suppressed hot carrier generation at the drain side, the saturation current level of LDD MOSFET is reduced due to the increased parasitic resistance at the source extension [13]. This makes simultaneous optimization of the device performance and hot carrier reliability difficult to achieve in symmetrical design. Therefore, the separation of source engineering and drain engineering in asymmetric MOSFET structure is essentially important to achieve the high performance and reliability. In this section, several types of asymmetric MOSFET structure are presented. And their advantages and disadvantages on the device functionality and the manufacturability are briefly explained.

2-4-2. Asymmetric channel structures

Fig. 8(a) shows the schematic cross-section of Lateral Asymmetric Structure (LAC) nMOSFET. For 0.1μm MOSFET technology, this structure has been proposed and introduced to Silicon on Insulator (SOI) in order to achieve the improved driving capability and hot-carrier reliability. It has laterally non-uniform channel with a localized pileup region next to the source junction as a result of asymmetric halo after gate electrode formation. It has

the high electron velocity at the source end of channel, indicating velocity overshoot, which is created by the localized highly doped channel at the source side. As device dimensions are scaled down, the asymmetric halo doping concentration must be increased in order to fully suppress DIBL and to adjust threshold voltage. However, it severely degrades the device performance due to the increased parasitic source resistance caused by the halo induced charge compensation. Consequently, highly doped halo cannot be used for the improvement of device characteristics in 0.1μm regime [7-11].

2-4-3. Asymmetric LDD

Fig. 8(b) shows the schematic cross-section of Asymmetric LDD structure nMOSFET. The structure having a heavily doped deep junction at the source side while lightly doped extension at the drain side shows that the improvement of driving capability has been successfully achieved while maintaining acceptable hot carrier reliability. Because of the reduction of parasitic resistance at the source side, the driving capability and the circuit speed are dramatically improved. However, it is difficult to employ such structures to sub-0.1μm MOSFET because the short channel effects are worsened due to the absence of the LDD extension at the source side [5-6].

2-3-4. Process complexities of the asymmetric MOSFET structures

Although these structures have several advantages on the device performance and reliability, their fabrication processes have a poor feasibility

in a CMOS process. For example, in asymmetric channel structure, the process using shadowing effects of a large tilted angled ion implantation after gate electrode formation consumes additional masking steps to form an asymmetric halo [7]. In addition, the process requires the alignment of a photoresist mask to the transistor gate with a precision better than the gate length in asymmetric MOSFET structures [6]. Fig. 9 schematically illustrates the process difficulties of asymmetric structures in 0.1μm MOSFET fabrication process.

In this thesis, Self-Aligned Asymmetric Structure (SAAS) without the problems mentioned above is proposed [22]. And it is verified that the new lateral-doping scheme of SAAS provides many advantages on the device characteristics including driving capability, short channel characteristics, and hot carrier reliability.

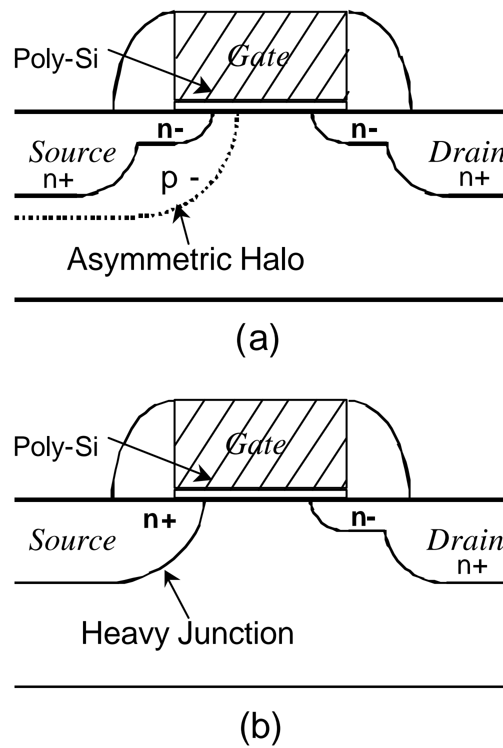


Figure 8. Two types of asymmetric MOSFET structures. (a) Lateral Asymmetric Channel (LAC) structure (b) A symmetric LDD structure

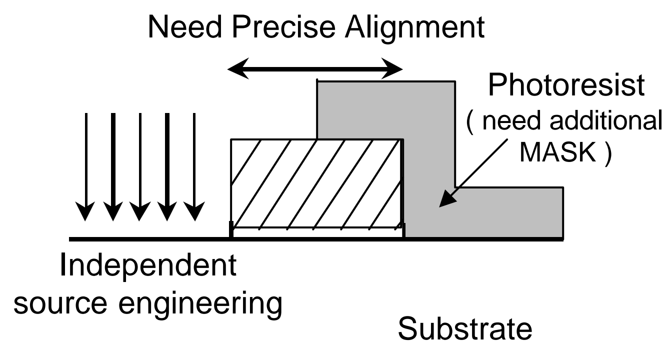


Figure 9. The Illustration used to explain the process complexities of asymmetric structures

Chapter 3. New Structural Approach: Self-Aligned Asymmetric Structure

3-1. Proposed Fabrication Process for SAAS

The key fabrication steps for n-channel SAAS MOSFET are schematically shown in Fig. 10. After 38Å thick gate oxide is grown on (100) p-type wafer, polysilicon (poly-Si) is deposited for gate material. Poly-Si is doped with $POCl_3$ and the pad oxide is deposited on the poly-Si. Next, the pad oxide on the gate-source area is etched away using lithography and dry etching process. Nitride film is deposited and etched to form a sidewall as shown in Fig. 10(C). In sidewall formation, the thickness of nitride film determines the poly gate length. This sidewall masking technique has been employed in 0.1μm MOSFET technology and reported to have better uniformity of line-width compared with e-beam lithography [23]. After the exposed poly-Si is anisotropically etched, the highly doped source extension is formed by As^+ ($1\times10^{15}cm^{-2}$, 10keV) implantation. The asymmetric halo implantation with BF_2^+ ($2\times10^{13}cm^{-2}$, 65keV, 25°) is performed to make lateral asymmetric channel profile. In order to prevent damages during the subsequent steps, nitride is deposited for capping the source region and etched by dry etching or CMP until the pad oxide reveals as shown in Fig. 10(E). After the pad oxide is etched, the exposed poly-Si is etched by dry etching. The lightly doped drain extension is formed using As^+ ($5\times10^{13}cm^{-2}$, 10keV) implantation. The

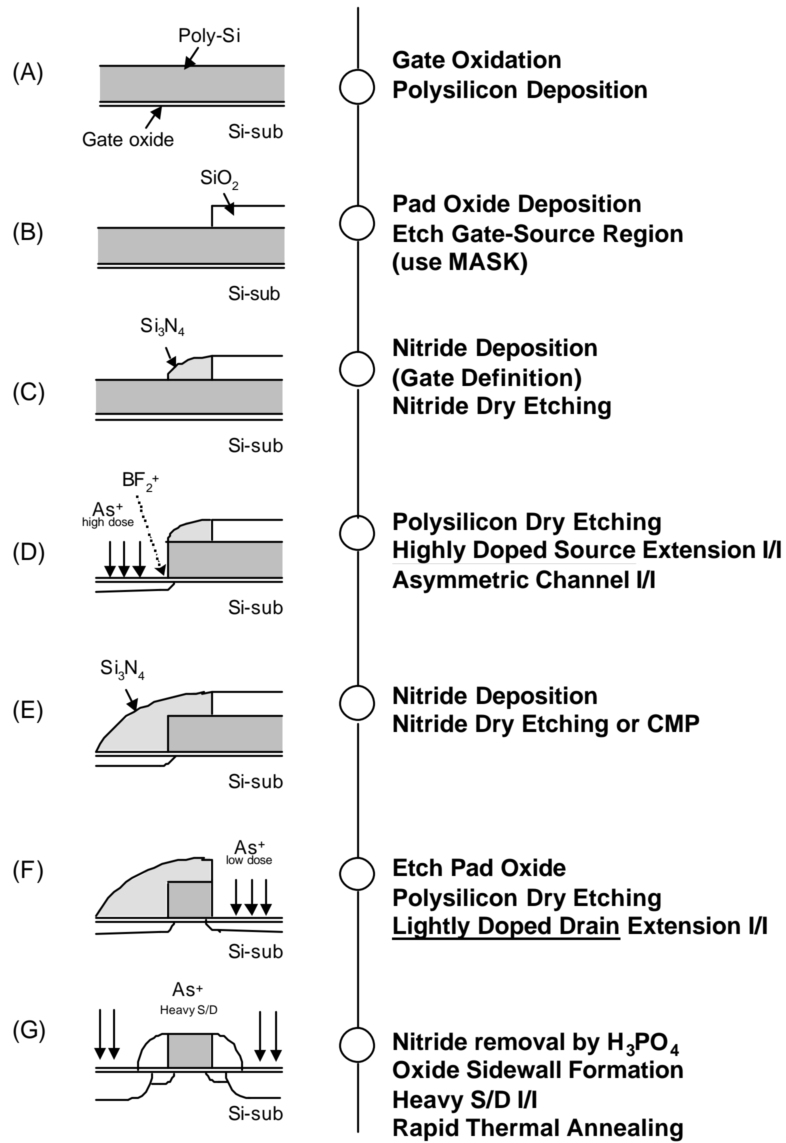


Figure 10. The proposed fabrication steps for Self-Aligned Asymmetric Structure (SAAS) n-channel MOSFET

remaining nitride is removed by H_3PO_4. After the 1000Å sidewall formation, the deep source/drain junctions are formed with As^+ ($6\times10^{15}cm^{-2}$, 40keV) implantation, followed by rapid thermal annealing (1050°C, 10sec). The following process steps are identical to those of the conventional MOSFETs.

As discussed above, we use only one lithography step for gate-source definition (Fig. 10(B)). Therefore, the proposed fabrication process for SAAS is expected to solve the self-alignment problem without additional masks, and independent optimization of the channel and the source/drain regions is possible for high performance and reliability.

3-2. Device Design

To optimize the SAAS design idea for high performance and reliability, extensive simulations are performed using the process simulators, TSUPREM-4 [24], which employs the point defect diffusion and the Dual Pearson implantation models. It has been reported that the point defect diffusion model reasonably predicts the ion implantation induced damages. And Dual Pearson distribution has been found to work well for modeling dose-dependent implantation profile [25].

The schematic cross-section of n-type SAAS MOSFET used for simulation analysis is given in Fig. 11(a). The structure is similar to the conventional MOSFET except for asymmetric LDD and asymmetric channel. Fig. 11(b)

shows the simulated two-dimensional doping profile of SAAS. Fig. 11 indicates that SAAS has the asymmetric channel profile along the Si-SiO_2 interface. It also has the highly doped source extension in opposition to the lightly doped drain extension. From these figures, SAAS differs from the conventional MOSFET structures in that it has localized highly doped channel next to the highly doped source and gradually lowered channel at the lightly doped drain.

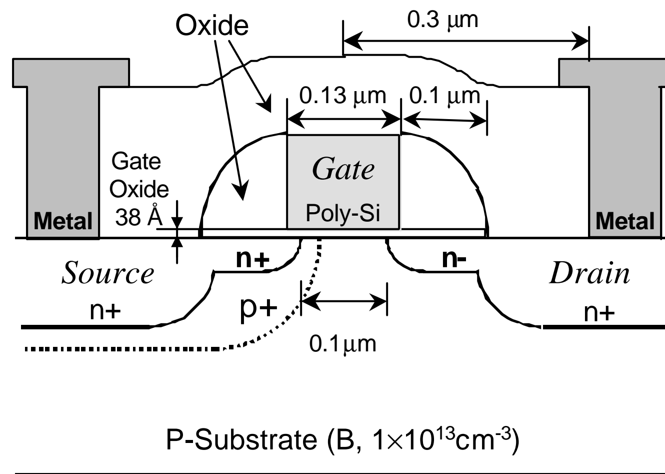
The structural concepts of SAAS are expected to show the following several advantages on device characteristics in deep sub-micrometer MOSFET.

1) Highly doped source may alleviate increased parasitic resistance caused by the highly doped halo which is employed to control the threshold voltage and to suppress the subthreshold leakage. By reducing the parasitic resistance at the source side, the improvement of saturation current is successfully achieved. In addition, the degraded short channel effects in highly doped source (asymmetric LDD) can be reduced by adopting the asymmetric halo [7].

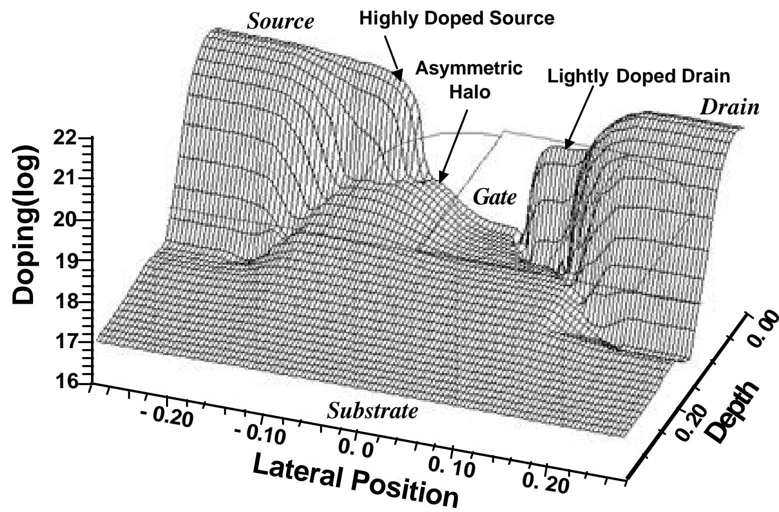
2) In the drain side, lightly doped drain extension and gradually lowered channel are expected to effectively suppress the hot carrier induced reliability problems. Moreover, with asymmetric channel, the V_T control can be obtained by adjusting asymmetric halo doping concentration, therefore, it allows to maintain a lower doped well concentration under the drain *pn* junction. Thus, drain junction leakage current and junction capacitance can be effectively reduced.

3) High built-in electric field created by the doping concentration gradient of the asymmetric channel improves the non-equilibrium carrier transport, velocity overshoot, at the source side [7,10]. This should benefit the driving capability and the circuit operation speed. Therefore, the device performance of SAAS is likely to be higher than that of conventional structure.

4) As previously mentioned in Chapter 2, increasing the halo dose in LAC structure results in the degradation of driving capability because the halo interacts with LDD doping, which causes the increased parasitic resistance. In SAAS, much higher doped halo can be used with the help of highly doped source, as mentioned 1). Because the doping concentration gradient of SAAS is much larger than that of the reported structure, SAAS enables the velocity overshoot to be more enhanced. Therefore, SAAS with higher carrier velocity is expected to have larger driving capability than that of LAC structure.



(a)



(b)

Figure 11. (a) The schematic cross-section of Self-Aligned Asymmetric Structure (SAAS) nMOSFET (b) The surface plots of the impurity concentration of SAAS that is used for the simulation analysis

Chapter 4. Simulation Analysis and Discussion

4-1. Simulation Methodology

4-1-1 Simulation Model Descriptions

In order to demonstrate the advantage of this new structure on higher performance and reliability compared to previously reported conventional and asymmetric structures, the numerical simulations are performed using well-known two-dimensional device simulator, MEDICI, which employs LSMMOB, FLDMOB, INCOMPLE, CONSRH, and AUGER models [26].

LSMMOB, which represents Lombardi surface mobility model, is used for better calculating the surface scattering in MOSFET's inversion layers. It was reported that this model could be applied to the carrier mobility not only in the inversion layer but also in the bulk silicon [27].

The carrier mobility can be written,

$$\mu_S = \left[\frac{1}{\mu_{ac}} + \frac{1}{\mu_b} + \frac{1}{\mu_{sr}} \right]^{-1} \qquad (4\text{-}1)$$

where μ_{ac} is the carrier mobility limited by the scattering with surface acoustic phonons, μ_b is the carrier mobility in bulk silicon, and μ_{sr} is the carrier mobility limited by the surface roughness scattering. The detailed model descriptions are presented in [27].

FLDMOB, which represents Caughey-Tomas expression for both electron

and hole mobility, is used for calculating the parallel field dependent mobility in MOSFET's inversion layers.

The model can be written,

$$\mu_n = \frac{\mu_{S,n}}{\left[1+\left(\frac{\mu_{S,n}E_{//,n}}{v_n^{sat}}\right)^{\mathbf{BETAN}}\right]^{\mathbf{1/BETAN}}} \tag{4-2}$$

$$\mu_p = \frac{\mu_{S,p}}{\left[1+\left(\frac{\mu_{S,p}E_{//,p}}{v_p^{sat}}\right)^{\mathbf{BETAP}}\right]^{\mathbf{1/BETAP}}} \tag{4-3}$$

where $\mu_{S,n}$ and $\mu_{S,p}$ are the low field mobilities and v_n^{sat} and v_p^{sat} are the saturation velocities for electrons and holes, respectively. $E_{//}$ is the component of electric field paralled to the current direction. EBETAN and BETAP are the fitting parameters which can be extracted from experimental data taken in appropriate experimental conditions. Values for v_n^{sat} and v_p^{sat} are computed by default from the following expression. In these simulations BETAN=2.0, BETAP=1.0, $v_n^{sat}=1.035\times10^7$cm/s, and $v_p^{sat}=1.035\times10^7$cm/s are selected for the silicon material.

$$v_{n,p}^{sat}(T) = \frac{2.4\times10^7}{1+0.8\cdot\exp\left(\frac{T}{600}\right)} \tag{4-4}$$

INCOMPLE is used for calculating the incomplete ionization of impurities

after ion implantation for the channel and the source/drain region. Although, for the case of long-channel device (which are formed by high energy ion implantation), full impurity ionization may be assumed, incomplete impurity ionization model is employed in these short channel device simulations with appropriate degeneracy factors for the conduction and valence bands GCB and GVB,

$$N_D^+ = \frac{N_D}{1 + \mathbf{GCB} \exp\left(\frac{E_{Fn} - E_D}{kT} \right)} \qquad (4\text{-}5)$$

$$N_A^- = \frac{N_A}{1 + \mathbf{GVB} \exp\left(\frac{E_A - E_{Fp}}{kT} \right)} \qquad (4\text{-}6)$$

where $E_D=E_C$-EDB and E_A=EAB+E_V are the donor and acceptor energy levels, respectively. N_D and N_A are net compensated n-type and p-type doping, respectively. In these simulations GCB=2, GVB=4, EDB=0.044eV, EAB=0.045eV are selected for the silicon material.

Net electron and hole recombination models in the continuity equations are essentially required for calculating the electrical behaviors of semiconductor device. In these simulations, CONSRH and AUGER models are used for better calculating the recombination (U). CONSRH represents Shockley-Read-Hall recombination model with concentration dependent lifetime. And AUGER represents Auger recombination model.

That is,

$$U = U_n = U_p = U_{SRH} + U_{Auger} \tag{4-7}$$

where,

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p \left[n + n_{ie} exp\left(\frac{\mathbf{ETRAP}}{kT} \right) \right] + \tau_n \left[p + n_{ie} exp\left(\frac{\mathbf{-ETRAP}}{kT} \right) \right]}$$

$$U_{Auger} = \mathbf{AUGN}(pn^2 - nn_{ie}^2) + \mathbf{AUGP}(np^2 - pn_{ie}^2) \tag{4-8}$$

In the above, n_{ie} is the effective intrinsic carrier concentration and τ_n and τ_p are the electron and hole lifetimes, which are dependent the impurity concentration in CONSRH model. The parameter ETRAP represents the difference between the trap energy level E_t and the intrinsic Fermi energy E_i (i.e., ETRAP = E_t-E_i), and AUGN and AUGP are specified constants. ETRAP = 0eV, AUGN = $2.8 \times 10^{-31} cm^6/s$, AUGP = $9.9 \times 10^{-32} cm^6/s$ are selected for the silicon material.

4-1-2. Device Structures for Simulation Analysis

Fig. 13 and Table 2 give the schematic cross-sections and the main device parameters for the structures considered in this works. For fair comparison, all structures have the effective channel length of 0.1μm, the punchthrough stopper of B^+ ($3\times10^{12} cm^{-2}$, 40keV), the substrate doping of 1×10^{13} cm^{-3} and the threshold voltage of about 0.38V. For all structure, As^+ implantation for the formation of heavy deep junction ($6\times10^{15} cm^{-2}$, 40keV) and thermal annealing condition (1050°C, 10sec) have been kept identical. The device fabrication

parameters of the structures are compared in Table 3. A-Chan and A-Drain represent the asymmetric nMOSFETs with asymmetric channel and asymmetric drain, respectively. It should be noted that the two different halo doses ($5\times10^{12}cm^{-2}$, $2\times10^{13}cm^{-2}$) are selected for investigating the influence of halo doping concentration on the device characteristics in asymmetric drain (SAAS) and symmetric drain (A-Chan) structures. Conv represents the conventional nMOSFET with the uniform channel. The uniformly doped channels in the case of Conv and A-Drain structures are formed by the threshold adjustment implantation (BF_2^+, $5\times10^{12}cm^{-2}$, 90keV) before the gate oxidation. The process conditions mentioned above are kept the same for all the structures while the asymmetric channel and the source/drain related process conditions are changed as shown in Table 3.

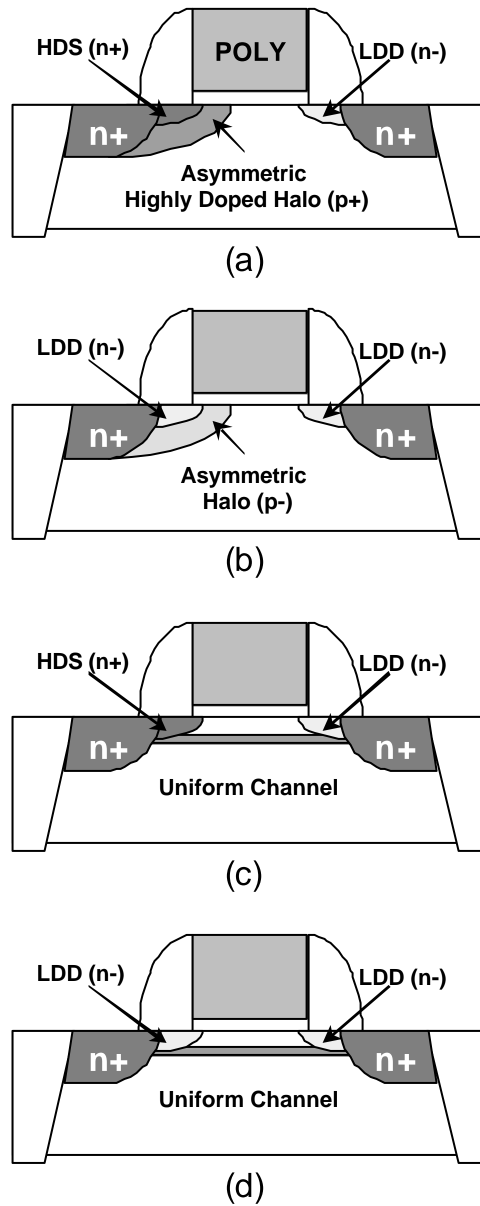


Figure 12. The schematic cross-section of the compared structures used for simulation analysis, (a) SAAS (b) asymmetric channel structure (A-Chan) (c) asymmetric drain structure (A-Drain) (d) conventional structure (Conv)

Table 2. Device process parameters of the compared structures used for simulation analysis

Device Process Parameter	*Values*
Oxide Thickness (t_{ox})	38 Å
Substrate Doping Concentration	1×10^{13} cm^{-3}
Punchthrough Stopper	$3\times10^{12}cm^{-2}$, 40keV, B^{+}
Heavy Junction Ion Implantation	$6\times10^{15}cm^{-2}$, 40keV, As^{+}
Annealing Condition	1050°C, 10sec
Sidewall thickness	0.1µm
Effective Channel Length	0.1~0.5µm

Table 3. Main features of the compared structures used for simulation analysis. Uniform channel is formed by BF_2^+ ($5\times10^{12}cm^{-2}$, 90keV) implantation before the gate oxidation. Asymmetric channel is formed by BF_2^+ ($5\times10^{12}cm^{-2}$ or $2\times10^{13}cm^{-2}$, 65keV, 25°) implantation only at the source side. As^+ implantation for the formation of source/drain is performed with 10keV energy and 0° tilt.

LABEL	*Source*	*Channel*	*Drain*
SAAS (2E13)	$1\times10^{15}cm^{-2}$ (n+)	*Asymmetric* $2\times10^{13}cm^{-2}$ (p+)	$5\times10^{13}cm^{-2}$ (n-)
SAAS (5E12)	$1\times10^{15}cm^{-2}$ (n+)	*Asymmetric* $5\times10^{12}cm^{-2}$ (p-)	$5\times10^{13}cm^{-2}$ (n-)
A-Chan (2E13)	$5\times10^{13}cm^{-2}$ (n-)	*Asymmetric* $2\times10^{13}cm^{-2}$ (p+)	$5\times10^{13}cm^{-2}$ (n-)
A-Chan (5E12)	$5\times10^{13}cm^{-2}$ (n-)	*Asymmetric* $5\times10^{12}cm^{-2}$ (p-)	$5\times10^{13}cm^{-2}$ (n-)
A-Drain	$1\times10^{15}cm^{-2}$ (n+)	*Uniform* $5\times10^{12}cm^{-2}$ (p-)	$5\times10^{13}cm^{-2}$ (n-)
Conv	$5\times10^{13}cm^{-2}$ (n-)	*Uniform* $5\times10^{12}cm^{-2}$ (p-)	$5\times10^{13}cm^{-2}$ (n-)

4-2. Comparison SAAS with other asymmetric structures

4-2-1. Short Channel Characteristics

Fig. 13 shows the linear region threshold voltage (V_D=0.1V), V_T, extracted from the calculated I_D-V_G data, as function of the effective channel length for the SAAS and compared structures. As shown in Fig. 13, the asymmetric channel structures (SAAS, A-Chan) do not experience the V_T roll-off effect even in the 0.1μm dimension because the localized high boron concentration at the source side results in the reverse short channel effect [28]. On the other hand, the uniform channel structures (A-Drain, Conv) have serious V_T roll-off effects, because they suffer from severe charge sharing effects.

Fig. 14(a), (b) shows I_D-V_G characteristics as a function of the effective channel length for SAAS and Conv, respectively. It is shown that the subthreshold characteristics of the asymmetric channel structure (SAAS) are independent of the effective channel length, while those of the uniform channel structure (Conv) are not. In the asymmetric channel structures, the localized high boron concentration at the source end of channel makes the structures show the same subthreshold characteristics regardless of the effective channel length [29]. Therefore, SAAS with channel independent subthreshold characteristics will have improved device performance without increasing the subthrehold current.

Fig. 15 shows the DIBL characteristics of these structures. In these simulations, DIBL is defined as the horizontal shift of gate voltage (V_G) at 10^{-7}

A/μm of subthreshold current (I_D) when the drain voltage (V_D) is increased from 0.1V to 2.0V. The uniform channel structures have worse DIBL characteristics than those of the asymmetric channel structures. In these structures, A-Drain with the highly doped source shows the worst DIBL characteristics. This result ensures the fact that asymmetric LDD have the degraded short channel characteristics [5-6]. In the asymmetric channel structures, the DIBL is well controlled due to the large potential barrier generated by the highly doped channel next to the source extension, which limits the spread of the depletion region from drain to source.

Fig. 16 shows the surface potential distributions of the structures along the channel. The large potential barrier as mentioned above is clearly observed in the asymmetric channel structures. It can be seen that the barrier height depends on the doping concentration of asymmetric halo, and thus, DIBL will be further suppressed if higher doped halo is adopted in the case of SAAS. From these results, highly doped asymmetric halo is needed to effectively suppress DIBL.

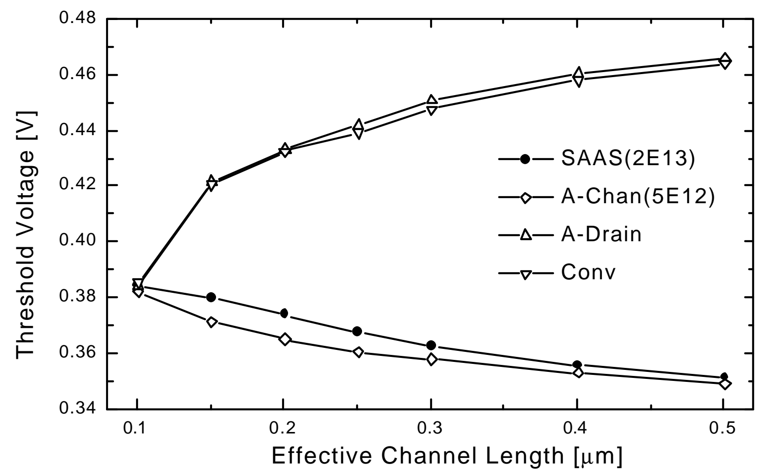
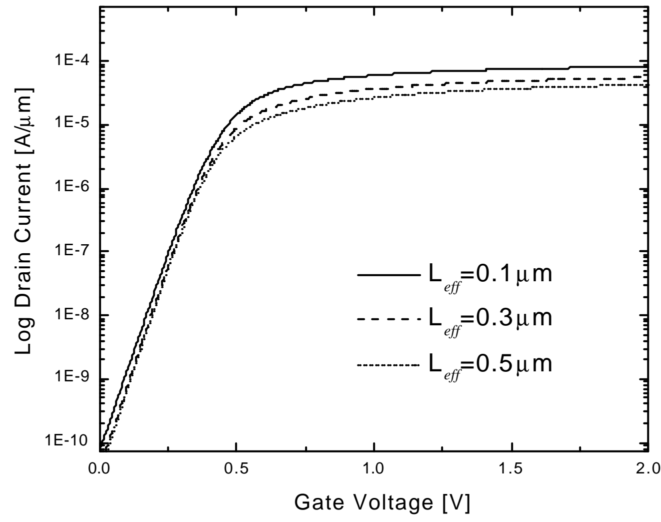
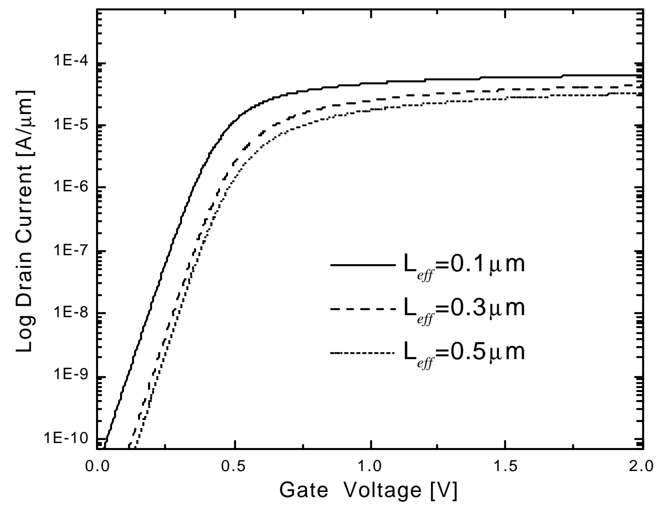


Figure 13. The threshold voltages (V_T) as a function of the effective channel length for SAAS and compared structures



(a)



(b)

Figure 14. The subthreshold characteristics as a function of the effective channel length for (a) SAAS and (b) Conv

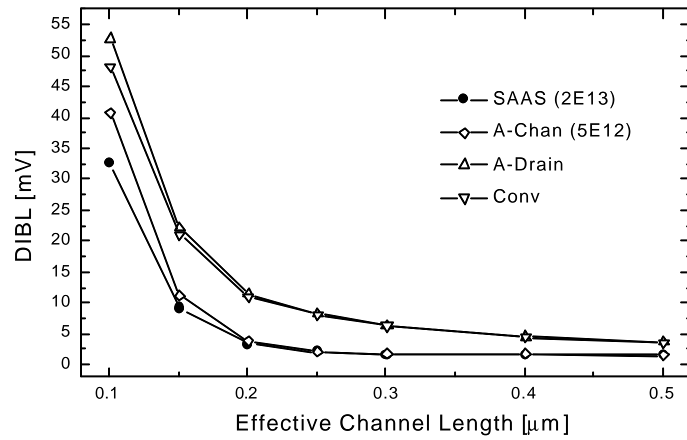


Figure 15. The Drain Induced Barrier Lowering (DIBL) [$V_{GS}(V_{DS}$=0.1V) – $V_{GS}(V_{DS}$=2.0) at $I_D=10^{-7}$ A/μm] as a function of effective channel length for SAAS and compared structures

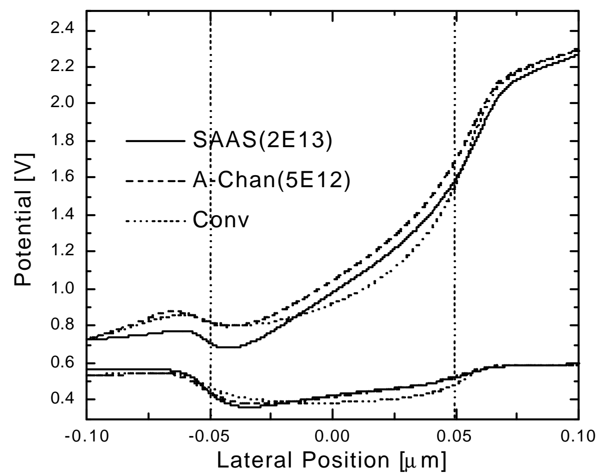


Figure 16. The potential distributions along the channel for SAAS, A -Chan and Conv

4-2-2. Driving Capability

Fig. 17 shows the simulated I_D-V_D characteristics for SAAS and compared structures. We can clearly observe higher current driving capability of SAAS than those of any other compared structures. Fig. 18 shows the influence of asymmetric halo dose on the driving capability in SAAS and A-Chan. It is shown that A-Chan with higher dose halo implantation results in the degradation of driving capability. On the contrary, the driving capability of SAAS is enhanced by higher dose halo implantation.

To explain the reason for the enhancement of driving capability in these structures, we simulated the electron velocity and the electric field along the channel using hydrodynamic simulator with energy balance equation, which has been reported to reasonably predict the enhancement of driving current caused by the velocity overshoot [3].

Fig. 19 shows the average electron velocity of SAAS and compared structures along the interface. For the asymmetric channel structures, the electron velocity rises rapidly at the source side and it causes the velocity overshoot phenomenon. Fig. 20 shows the electron density of SAAS and compares structures along the interface. The current density of drain currents can be simply written as,

$$J = -qnv \qquad (4\text{-}9)$$

where q is the magnitude of electronic charge, n is the electron concentration and v is the effective electron velocity. Since the electron density of the asymmetric channel structure is slightly lower than that of

uniform channel structure as shown in Fig. 20, the origin of the improved driving capability in asymmetric structures (SAAS, A-Chan) is attributed to the high carrier velocity at the channel next to source. Furthermore, SAAS with higher doped halo further enhances the electron velocity at the source side. This result indicates that the halo dose is closely related to the electron velocity.

Fig. 21 shows the influences of halo dose on the electron velocity along the channel. From this figure, it is known that the electron velocity at channel depends on the channel profiles, not the source/drain. As the halo dose increases, the electron velocity at the source also increases. As shown in Fig. 18, the highly doped halo results in the improvement of driving capability in SAAS, which can be explained by the enhancement of electron velocity. On the contrary, A-Chan shows the decreased driving current level as the halo dose increases. This is because the halo interacts with LDD doping and causes the source resistance to be increased, which is a key factor for the saturation current levels [12]. It makes the A-Chan undesirable for scaling down to 0.1μm regime while maintaining adequate short channel behaviors. In other words, increasing the asymmetric halo doping in order to suppress the short channel effects and to enhance the velocity overshoot results in the degradation of driving performance in conventional (symmetric) drain structures. However, SAAS is less sensitive to such effects because of having the highly doped asymmetric source extension with low parasitic resistance.

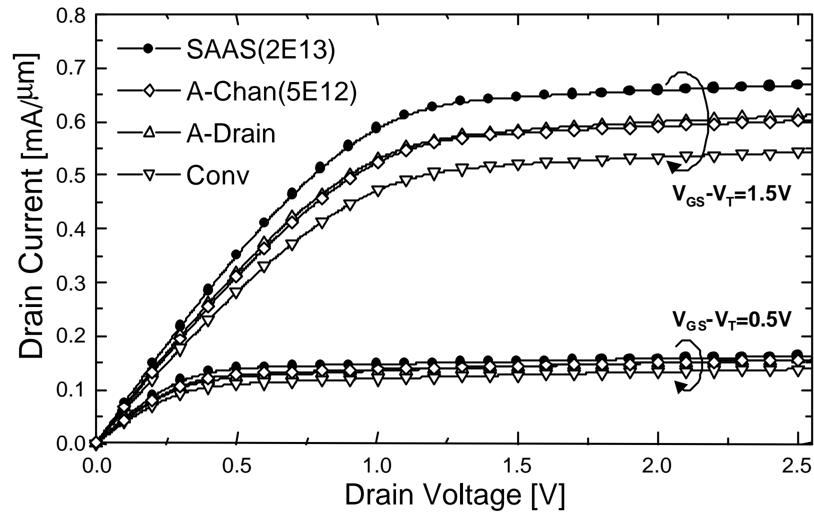


Figure 17. Simulated I_D-V_D characteristics of SAAS and compared structures

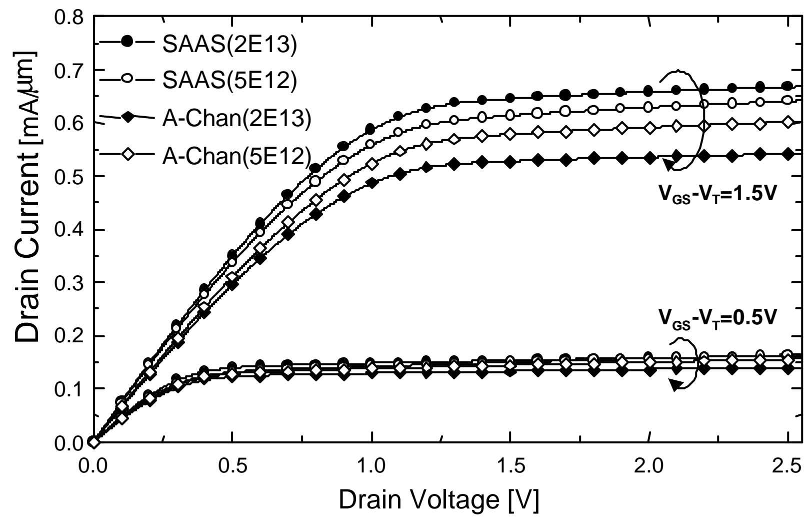


Figure 18. Simulated I_D-V_D characteristics of SAAS and asymmetric channel structure (A-Chan) under the different asymmetric halo doping conditions

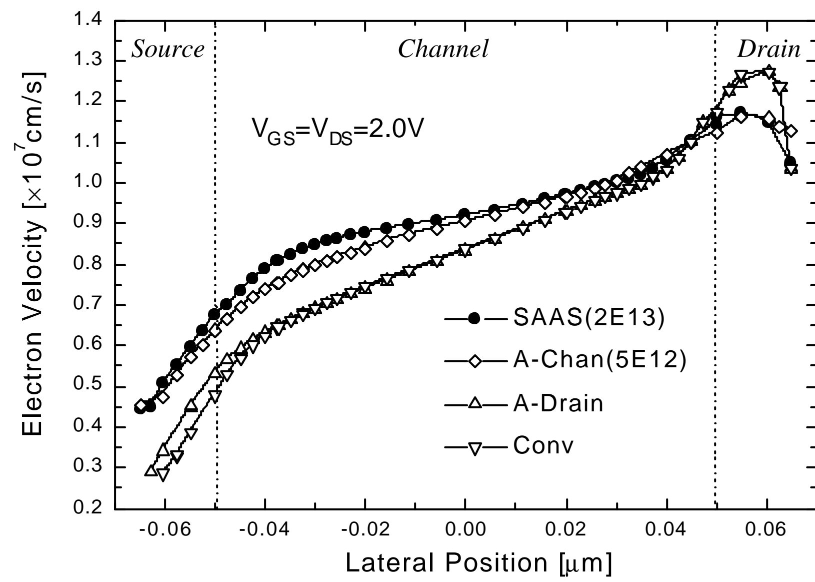


Figure 19. Simulated average electron velocity distributions of SAAS and compared structures ($V_{GS}=V_{DS}=2.0V$)

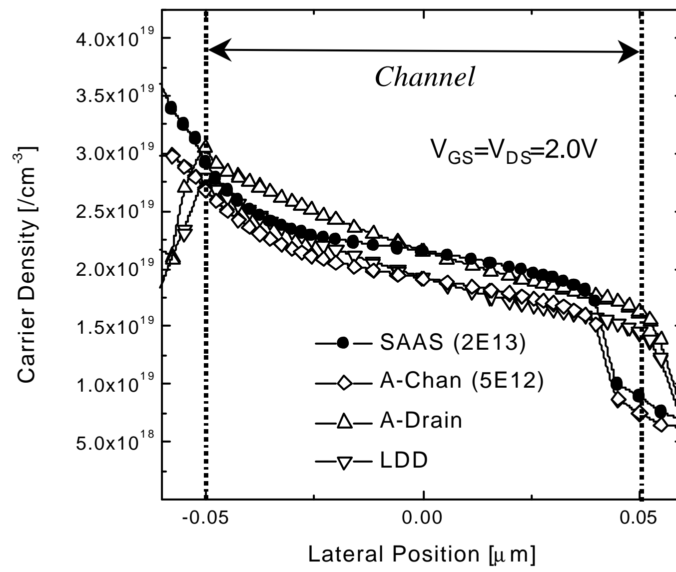


Figure 20. Simulated electron carrier densities of SAAS and compared structures ($V_{GS}=V_{DS}=2.0V$)

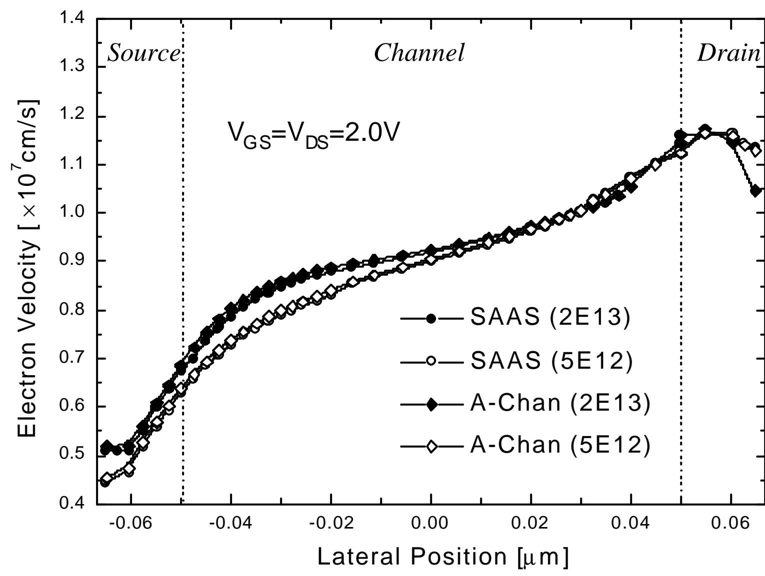


Figure 21. Simulated average electron velocity distributions of SAAS and A-Chan structure under the different asymmetric halo doping conditions ($V_{GS}=V_{DS}=2.0V$)

Fig. 22 and Fig. 23 show the simulated lateral electric field profiles and net doping concentration along the interface for SAAS and compared structures, respectively. It can be seen that the electric fields of asymmetric channel structures are much higher those of uniform channel structures at the channe l next to the source, while the electric fields of uniform channel structures exceed those of the asymmetric channel structures at the drain end of channel. In the asymmetric structures, the high electron velocity as seen in Fig. 19 is due to the large electric field and its gradients produced by the localized highly doped channel next to the source extension as shown in Fig. 23. The inset of Fig. 23 is the magnification of the net doping concentration at the source side. The figure shows that the net doping of A-Chan is much lower than those of other structures. This means that the parasitic resistance at the source side is increased due to the charge compensation. As a result, the symmetric drain structure (A-Chan) is not advantageous in the respect of driving capability if highly doped halo is employed, which was already discussed and shown in Fig. 18. On the contrary, SAAS has the highest net doping level at the source side in the compared structures. The reason is that highly doped source as well as highly doped channel promises high net doping concentration. Consequently, SAAS with high net doping at the source extension is effective in alleviating the increasing parasitic resistance caused by the highly doped halo.

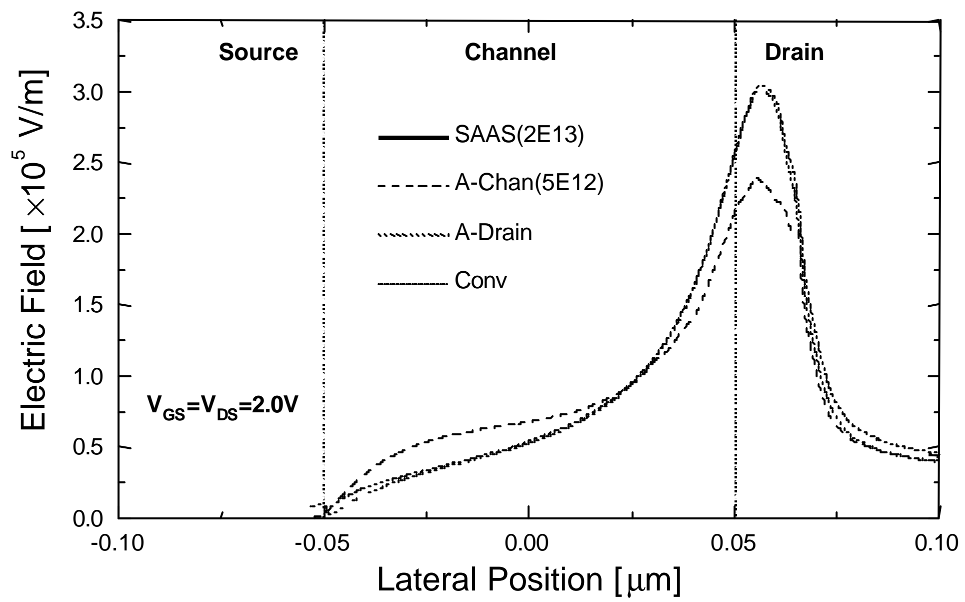


Figure 22. Simulated lateral electric fields of SAAS and compared structure (V_{GS}=V_{DS}=2.0V)

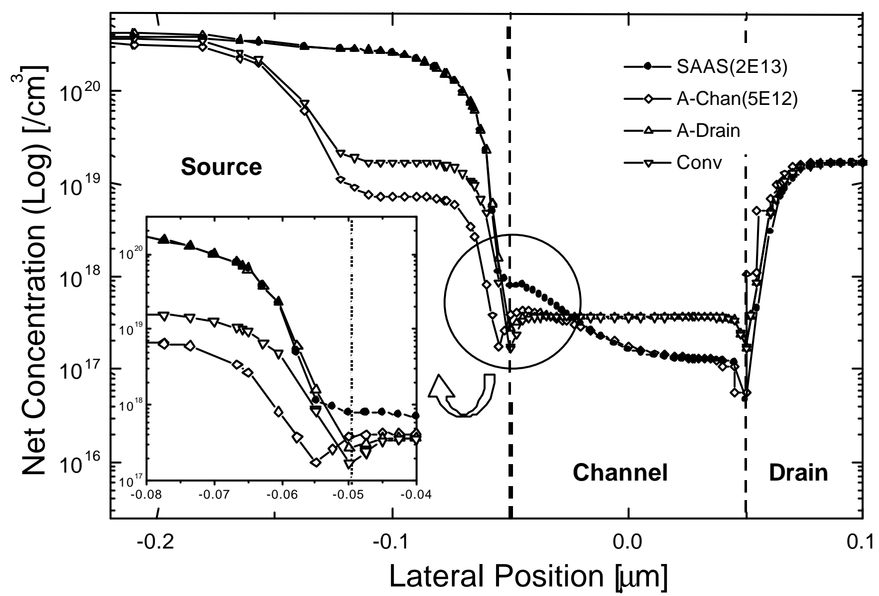


Figure 23. Net doping profiles of SAAS and compared structures at 1.5nm away from Si-SiO_2 interface. The inset shows the net doping profiles at the source area.

4-2-3. Hot Carrier Reliability

Fig. 22 indicates that the magnitudes of the drain electric fields in asymmetric channel (SAAS, A-Chan) structures are approximately 22% less than those of uniform channel (A-Drain, Conv) structures. It is because the gradually lowered channel at the lightly doped drain as shown in Fig. 23 results in the decreased lateral electric field at the drain side. Since the hot carrier degradation is exponentially dependent on the electric field at drain, SAAS with the lower electric field at the drain junction is expected to effectively suppress the hot carrier generation. Fig. 24 shows the simulated effective impact ionization rates (I_{sub}/I_D) of SAAS and compared structures, which take into consideration the nonlocal effects with energy balance equation. The asymmetric channel structures have a relatively lower effective impact ionization rate compared with uniform channel structures for the same effective channel length due to their low electric field at the drain side. In consequence, gradually lowered channel in asymmetric channel structures is very effective in reduction of hot carrier induced degradations.

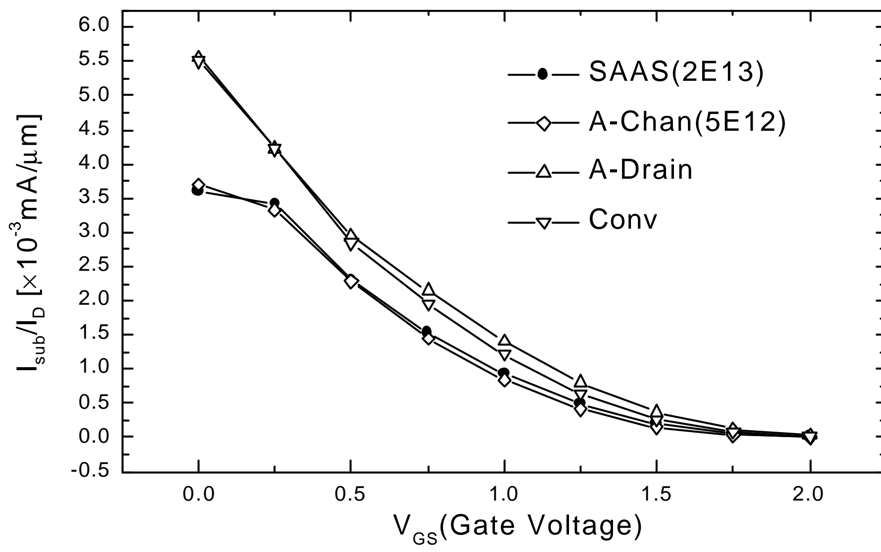


Figure 24. Simulated effective impact ionization rates (I_{sub}/I_D) of SAAS and compared structures

Chapter 5. Conclusion

The difficulties and limitations of deep sub-micrometer MOSFET are explained based on the previous research, and several structural approaches for overcoming such limitations are described.

Using the asymmetric doping scheme, significant improvements in device characteristics can be obtained. Asymmetric LDD structures are effective in improving device performance due to the low parasitic resistance at the source extension, even though they have the degraded short channel behaviors. The stabilized threshold voltage and the channel independent subthreshold characteristics are successfully achieved in LAC structures. And, they also give rise to improvement of device performance. The origin of the improved driving capability in LAC structure is attributed to the high carrier velocity at the channel next to source. However, the trade-off between the enhancement of velocity overshoot and the increase of parasitic resistance exists for asymmetric channel structure formed by the asymmetric halo. Moreover, the difficulties of fabrication process in asymmetric structure are worsening as devices are scaled below 0.1μm.

For overcoming the trade-off, disadvantages and process complexities, Self-Aligned Asymmetric Structure (SAAS), which have asymmetric drain with asymmetric channel, has been proposed for 0.1μm MOSFET technology. The main advantage of proposed structure is that source, drain and channel to be designed independently without additional lithography steps. By

hydrodynamic simulations, it is shown that SAAS with higher doped halo fully enhances the velocity overshoot and completely suppresses the subthreshold leakage current. The highly doped source in SAAS alleviates the increasing parasitic resistance caused by the highly doped halo induced charge compensation. Therefore, the device performance of SAAS is superior to that of the previously reported MOSFET structures under the same device parameters. Another important advantage of SAAS is the suppression of hot carrier induced degradation. It is because the gradually lowered channel in SAAS results in the reduced drain electric field. Consequently, this new structure should enable MOSFET devices to be more successfully scaled to sub-0.1μm dimension for improving device performance without increasing process cost.

This thesis work is mainly focused on the simulated device characteristics discussed by comparing the new structure with the previously reported structures. The experimental verification of SAAS remains as future works.

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국문요약

새로운 구조를 가진 0.1㎛ 급 비대칭 MOSFET 구조의 특성에 관한 연구

본 논문에서는 소자의 크기가 작아짐에 따라 생기는 여러 가지 현상 및 문제점을 설명하고, 해결방안으로 자기정렬이 가능한 비대칭구조와 그것의 공정방법을 제안하고 기존에 제안된 구조와 비교 분석하였다. 제안된 공정방법은 추가적인 마스크 없이 비대칭구조 MOSFET 의 형성이 가능하다. 제안된 비대칭구조는 소오스가 드레인에 비해 상대적으로 높은 불순물 도즈양을 갖는 비대칭적 드레인구조일뿐만 아니라, 채널이 소오스쪽에만 부분적으로 높은 불순물 분포를 갖는 비대칭적인 채널구조를 가지고 있다. 이차원 시뮬레이션을 통하여 이러한 새로운 구조는 기존에 제안된 비대칭 구조에 비해 우수한 단채널 특성, 성능 및 신뢰성을 가지고 있음을 보였다. 또한 성능향상의 원인이 높은 도즈의 비대칭 Halo 에 의한 높은 캐리어 속도와 소오스 부분의 낮은 기생저항 때문인 것 확인되었다.

높은 소자 성능을 가지고 있는 비대칭구조 MOSFET 을 설계하고 제작할 경우, 본 논문에서 제안한 구조는 기존의 제안된 비대칭구조 MOSFET 보다 높은 성능 및 낮은 공정 비용으로 인하여 앞으로 유용하게 사용될 것으로 기대된다.

핵심 되는 말 : MOSFET, 비대칭구조, 자기정렬, Velocity overshoot, 소자 시뮬레이션, 단채널효과, CMOS Scaling