ISOCC 2023
20th International SoC Design Conference

Program at a Glance

Preliminary Program

Notice:

Please check the presentation time with the paper number you submitted to CMT.

For the regular oral papers (including special session papers),
the presentation time is 15 minutes,typically 12 minutes for presentation and 3 minutes for Q&As.
The poster presentation time is **October 27 (Fri), 2023**.

The schedule according to the local conditions may be changed.

ISOCC 2023 Program Download

ISOCC 2023 Program Schedule At-a-glance

WEDNESDAY_ OCTOBER 25, 2023

From	Till	Lobby	LOBBY 1F	GRAND BALLROOM2 1F	GRAND BALLROOM3 2F	GRAND BALLROOM4 2F	Mara 2F	Udo 2F
12:00	13:00	On-site Regist ration	Job Fair (Grand Ballroom1)					
13:00	13:30			Main Tutorial	Job Fair Company Prsentation	AutoCAS		
13:30	14:00							
14:00	14:30			Short Tutorial				
14:30	16:30							
16:30	16:50				Mini Tutorial			
16:50	17:10							
17:10	17:30			Mini Tutorial				
17:30	18:00		Break Time (30min.)					
18:00	20:00		**Welcome Reception** (8F Tamna Hall)					

THURSDAY_ OCTOBER 26, 2023

From	Till	Lobby	LOBBY 1F	GRAND BALLROOM2 1F		GRAND BALLROOM3 2F		GRAND BALLROOM4 2F		Mara 2F		Udo 2F	
08:30	08:40	On-site Regist ration & Sponsor Exhibition	Chip Design Contest (CDC) **Poster 1**	CDC Oral									
08:40	08:50												
08:50	09:00												
09:00	09:10												
09:10	09:20												
09:20	09:35		**Opening Ceremony** (Grand Ballroom1)										
09:35	10:15		**Keynote Speech-1** (Grand Ballroom1)										
10:15	10:55		**Keynote Speech-2** (Grand Ballroom1)										
10:55	11:10		Break Time (15min.)										
11:05	11:15				140		32		105		18		48
11:15	11:30				91		72		23		26		84
11:30	11:45			ET1	102	AC1	103	DCAS1	14	SS1	52	SS2	126
11:45	12:00				142		119		6		63		133
12:00	12:15				184		189		156		177		134
12:15	13:30		Lunch (1F Tamora Restaurant), WiCAS(2F, Grand Ballroom4)										
13:30	13:45		Chip Design Contest (CDC) **Poster 2**		65		19		183		12		79
13:45	14:00				135		86		167		33		81
14:00	14:15			ET2	162	AC2	107	DCAS2	187	SS3	42	SS4	85
14:15	14:30				191		148		35		104		87
14:30	14:45				202		199		155		168		92
14:45	15:00		Break Time (15min.)										
15:00	15:15						89		31		5		45
15:15	15:30						17		240		66		53
15:30	15:45						188		106		68		54
15:45	16:00					RF	218	DCAS3	15	SS5	110	SS6	99
16:00	16:15						219		51		121		164
16:15	16:30								1		123		203
16:30	16:45								132				264
16:45	17:00		Chip Design Contest (CDC) Poster Exhibition										
17:00	17:30												
17:30	18:00		Break Time (30min.)										
18:00	20:00		**Banquet** (Grand Ballroom)										

FRIDAY_OCTOBER 27, 2023

From	Till	Lobby	LOBBY 1F	GRAND BALLROOM2 1F		GRAND BALLROOM3 2F		GRAND BALLROOM4 2F		Mara 2F		Udo 2F	
08:30	08:45	On-site Regist ration & Sponsor Exhibition			59		196						
08:45	09:00				60		3						
09:00	09:15			SOC1	83	DC	160						
09:15	09:30				166		193						
09:30	09:45				181		4						
09:45	10:25		Poster Session (2F, Lobby) (Standing Time: 40min.)										
10:25	11:05		Poster Exhibition Time & Intro. of Research Lab. (Poster)	**Keynote Speech-3** (Grand Ballroom1)									
11:05	11:45			**Keynote Speech-4** (Grand Ballroom1)									
11:45	13:00			Lunch (1F Tamora Restaurant)									
13:00	13:15				34		157		265		37		204
13:15	13:30				80		108		152		58		227
13:30	13:45			MLAI	109	WL	75	SS7	224	SS8	74		228
13:45	14:00				165		49		226		150		229
14:00	14:15				175		159				237		230
14:15	14:30			Break Time (15min.)								SS9	232
14:30	14:45				73		43		10		28		234
14:45	14:45				127		88		11		93		
14:45	15:00			SOC2	128	SS10	94	SS11	24	SS12	95		
15:00	15:15				169		137		36		136		
15:15	15:30				185		163		90		172		
15:30	15:45				197		173		111				
15:45	16:00		Break Time (15min.)										
16:00	16:30		**Closing Ceremony** (Grand Ballroom1)										

CHIP DESIGN CONTEST

CDC-P004 **Multi-Layer Nanoelectromechanical (NEM) Memory Switches for Efficient Multi-Path Routing**

Geun Tae Park, JinWook Lee, Ji Soo Yoon, and Woo Young Choi
Seoul National University, Korea

CDC-P005 **AnOver100mWWirelessPowerTransferSystemwith1.695MbpsUplinkTelemetry and a Shared Inductor Dual-Output Regulating Rectification under Distance Variation**

Hongkyun Kim, Chul Kim
Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P006 **LOG-CIM: An Energy-Efficient Digital Computing-In-Memory Processor Supporting a Wide Range of Logarithmic Quantization with Zero-Aware 6T Dual-WL Cell**

Soyeon Um, Sangjin Kim, Seongyon Hong, Sangyeob Kim, and Hoi-Jun Yoo
Korea Advanced Institute of Science and Technology (KAIST), Korea

CDC-P007 **A RISC-V Processor Supporting AMBA AXI Protocol for Embedded Systems**

Won Sik Jeong, Sunbeom Kwon, Hyun Woo Oh, Jeongeun Kim and Seung Eun Lee
Seoul National University of Science and Technology, Korea

CDC-P008 **A 40Gb/s/pin Single – Ended Transmitter with Output pad Network for Memory Interface Application in 28-nm CMOS**

Dae-Won Rho, Jae-Koo Park, Seung-Jae Yang, and Woo-Young Choi
Yonsei University, Korea

CDC-P009 **FlexBlock: A Flexible DNN Training Accelerator with Multi-Mode Block Floating Point Support**

Jahyun Koo[1], Seock-Hwan Noh[1], and Jaeha Kung[2]
[1]*Daegu Gyeongbuk Institute of Science & Technology(DGIST), Korea*
[2]*Korea University, Korea*

CDC-P010 **48-Channel Sub-Array Ultrasound Beamforming System for High-Resolution Image Acquisition**

Soohyun Yun, and Joonsung Bae
Kangwon National University, Korea

Print

ISOCC 2023
20th International SoC Design Conference

October 25-28, 2023
Ramada Plaza Jeju Hotel, South Korea

Receipt of Registration

Sep 1, 2023

Mr. Daewon Rho
Electrical Electonical Engineering,
Yonsei University,
Korea

Dear Mr. Daewon Rho,

This is to officially confirm your payment of registration fee for ISOCC 2023, which will be held in conference during October 25-28, 2023.

Registration Fee

Registration No.	R0086
Full Name	Daewon Rho
Total Due Amount	Registration Fee - KRW 116,000 Additional Request Fee - KRW 157,500 Total Paid Amount - KRW 273,500 Balance - KRW 0
Payment Method	Credit Card

The Institute of Semiconductor Engineers(ISE)

ISOCC 2023 Secretariat.
#1736, Dukmyung B/D, 625, Teheran-ro, Gangnam-gu, Seoul, Republic of Korea
Tel: +82-2-757-0981 / Email: secretary@isocc.org

단체명 : (사)반도체공학회 / 고유번호: 464-82-00137
대표자 : 이규복(Kyu-Bok Lee) / 소재지 : (06173) 서울특별시 강남구 테헤란로 625, 1736호(삼성동, 덕명빌딩)

IDEC Chip Design Contest

A 40Gb/s/pin Single – Ended Transmitter with Output pad Network for Memory Interface Application in 28-nm CMOS

Dae-Won Rho, Jae-Koo Park, Seung-Jae Yang and Woo-Young Choi

Innovative Research Group HSCS

Introduction

- The demands for the higher bandwidth memory access are continuously increasing for many applications such as data centers, HPC and AI processors.
- The importance of high-speed memory interfaces is increasing as well and a number of technical approaches are being researched and developed.
- This CDC work presents the technique of designing high–speed transmitter(TX) in 28-nm process.

Proposed Transmitter

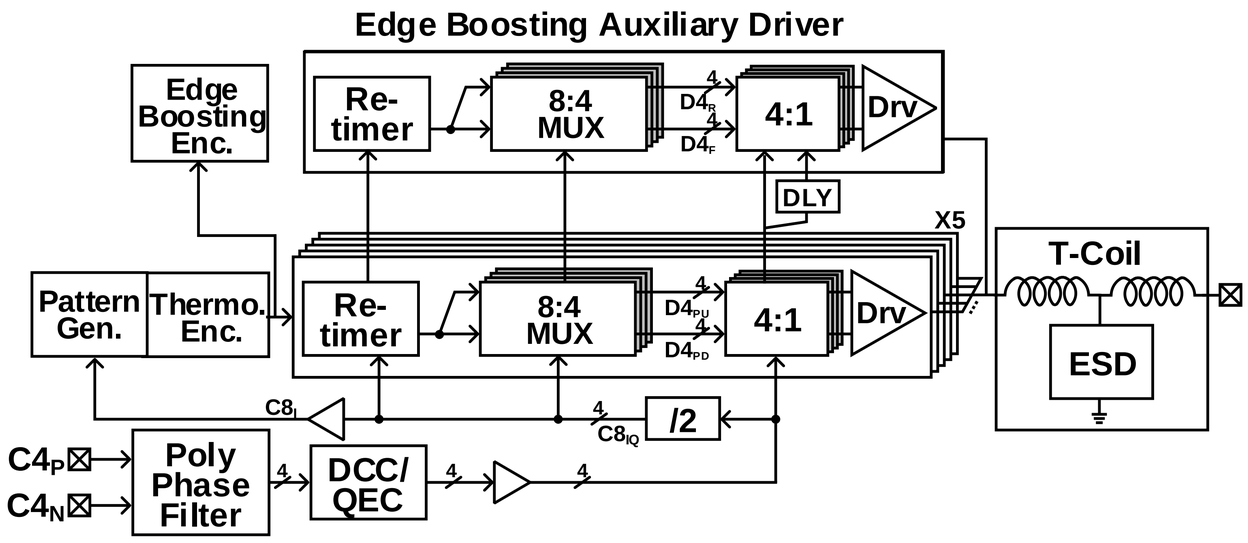


Fig 1. Transmitter overall block diagram

- Fig 1. shows the overall block diagram of transmitter
- It contains PRBS generator, retimer, serializer and driver in data path and output pad network is composed of T-coil and ESD protection.
- Edge boosting auxiliary driver is implemented to maximize eye opening
- A 7GHz differential clock is inputted into poly phase filter and passes through duty-cycle corrector(DCC) and quadrature error corrector(QEC) to produce enough timing margin.

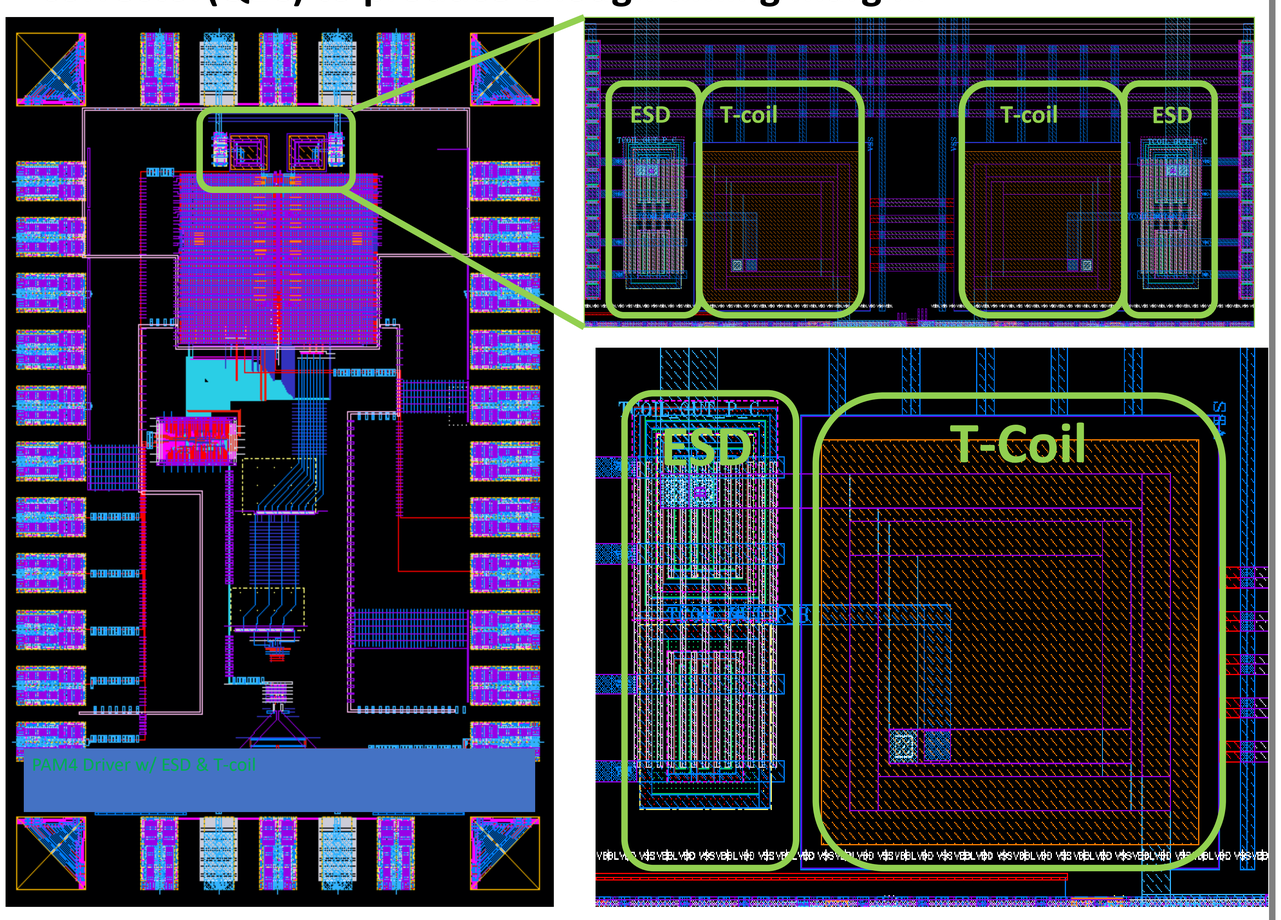


Fig 2. Top Layout and an enlarged view of T-coil and ESD protection

- Fig 2. shows top layout and an enlarged view of T-coil and ESD protection.

Chip photograph and measurement setups

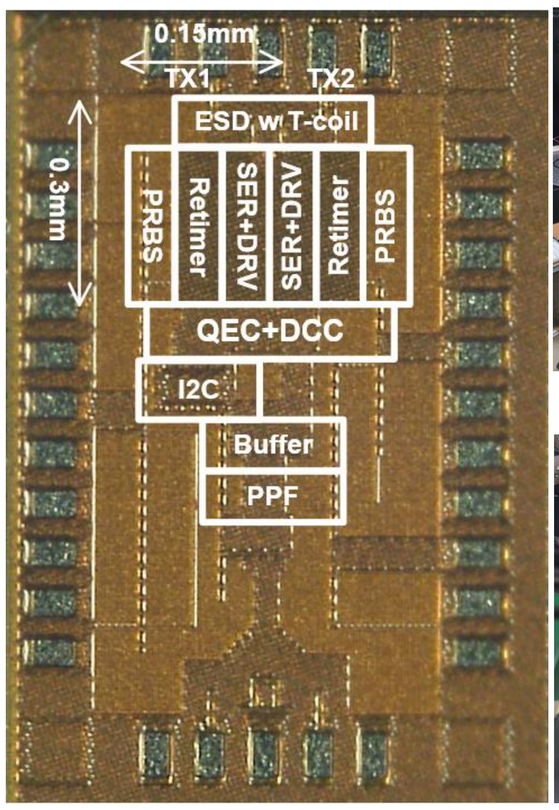


Fig 3. (a) Chip Photo

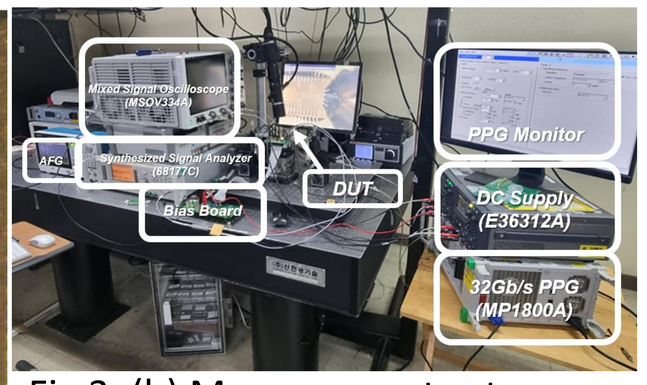


Fig 3. (b) Measurement setup

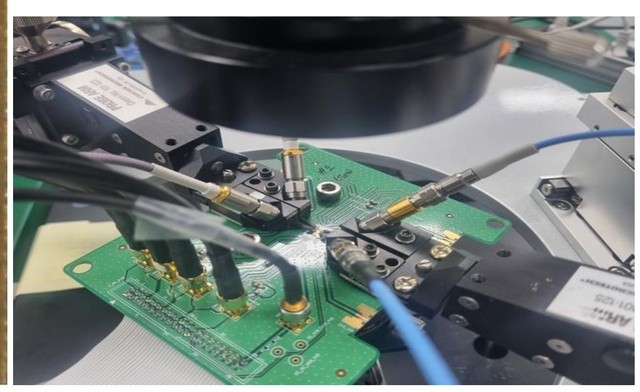
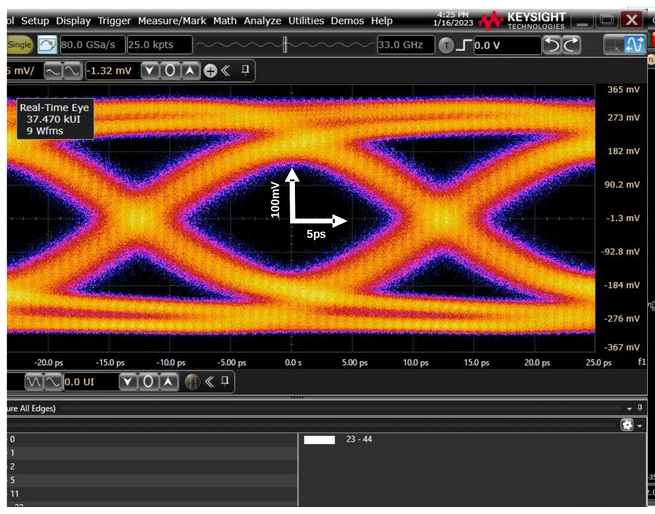


Fig 3. (c) Probe station

- Fig 3. (a) shows the fabricated chip of our design
- Fig 3. (b) shows the measurement setup. It comprised of the pulse pattern generator(PPG), oscilloscope, arbitrary function generator(AFG), and etc.
- Fig 3. (c) shows the probe station and DUT.

Measurement Results



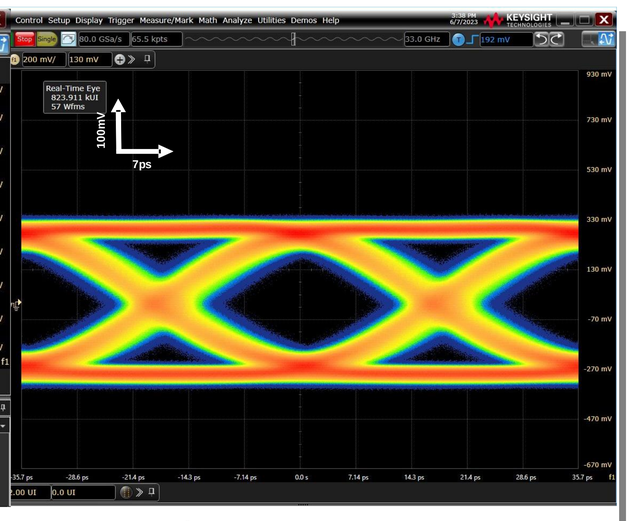


Fig 4. (a) 40Gb/s w/o ESD (b) 28Gb/s NRZ with T-coil & ESD

- The eye diagrams are presented in Fig. 4
- Single-ended 40Gb/s eye is demonstrated
- It has 297mV eye opening
- T-coil with ESD reduces the data rate, but improves yield.

Conclusion

- We have demonstrated 40Gb/s/pin single-ended transmitter in CMOS 28-nm process
- We designed low-voltage swing terminated logic(LVSTL) driver, which allows the efficient driver size and the impedance control.
- By using an edge-boosting auxiliary driver, we can finely adjust the pulse width, which enables to optimize the eye opening.

Acknowledgement

- Chip fabrication and EDA Tool were supported by IC Design Education Center, Korea.