IEDM 69th International Electron Devices Meeting

2023 IEDM Conference Theme

Devices for a Smart World
Built Upon 60 Years of CMOS

IEEE Electron Devices Society

2023 IEEE International Electron Devices Meeting

December 9-13, 2023

Hilton San Francisco Union Square
San Francisco, California

Call for Papers

Submission deadline: July 13th
Single submission of final, four-page paper

Topics

IEDM encourages submissions in all areas with special emphasis on:

- Neuromorphic / compute in memory / AI
- Quantum computing devices
- Devices for RF, 5G/6G, THz and mm-wave
- Advanced memory technologies
- Advanced logic technologies and power distribution network
- Novel materials for next generation devices
- Non-charge-based materials, devices and systems
- Advanced power devices, modules and systems
- Sensors, MEMS and bioelectronics
- Devices/circuits/system interaction
- Advanced Packaging, and package-device level interactions
- Electron device simulation and modeling
- Reliability of systems and electronic devices
- Robustness/security of electronic circuits and systems
- Optoelectronics, displays and imaging systems

Meeting Highlights

- Three plenary presentations by prominent experts
- Special focus sessions covering topics in:
  - Sustainability in Semiconductor Device Technology and Manufacturing
  - Logic, Memory, Package and System Technologies for Future Generative AI
  - 3D Stacking for Next-Generation Logic & Memory by Wafer Bonding and Related Technologies
  - Neuromorphic Computing for Smart Sensors
- Evening Panel Discussions
- Six tutorial sessions on Saturday, December 9th
- Two short courses on Sunday, December 10th
- Exhibits on December 11th – 13th

For More Information

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Description:

This session includes 5 papers that describe recent developments in the area of emerging photodetectors spanning from MIR to the DUV spectral range and from group IV and III-V sensors to organic detectors.
The first paper by KAIST presents a fully CMOS compatible Ge on Insulator platform for detection of wavelengths beyond 4 µm.
The second paper by KIST presents a new record low jitter SPAD device integrated into a CIS process technology covering a spectral range of visible up to NIR.
The third paper by KAIST shows a wavelength tunable detection device combining optical gratings and phase-change materials reaching wavelengths up to 1700 nm.
The next paper by the University of Science and Technology of China reports a dual function tunable emitter and NIR photodetector combination based on III-V GaN/AlGaN nanowires on silicon.
The last (invited) paper gives an overview on the next-generation of sustainable organic photodetectors and emitters.

On Mobile App? View Papers Here

Type: Technical Session

PRESENTATIONS

Tuesday, December 12, 2023 - 02:20 PM
20-1 | Fully CMOS-Compatible Room-Temperature Waveguide-Integrated Bolometer Based on Germanium-on-Insulator Platform at Mid-Infrared Operating Beyond 4 µm

Tuesday, December 12, 2023 - 02:45 PM
20-2 | Back-Illuminated SPAD in 40 nm CIS Technology Achieving 56 ps Timing Jitter With 15 V Breakdown Voltage for Short/Mid-Range LiDAR Applications

Tuesday, December 12, 2023 - 03:10 PM
20-3 | Wavelength-tunable grating-resonance InGaAs narrowband photodetector with infrared optical PCM, antimony triselenide (Sb_2Se_3)

Back-Illuminated SPAD in 40 nm CIS Technology Achieving 56 ps Timing Jitter With 15 V Breakdown Voltage for Short/Mid-Range LiDAR Applications

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***Abstract*—**We report on a back-illuminated single-photon avalanche diode (SPAD) based on stacked 40 nm CIS technology for short/mid-range LiDAR applications. The SPAD is optimized to achieve superior temporal resolution with a low breakdown voltage of 15 V. It achieves a photon detection probability of 21% and timing jitter of 56 ps at 940 nm with the excess bias voltage of 5 V.

I. Introduction

The emergence of advanced 3D imaging technologies has revolutionized image sensors for numerous applications such as augmented/virtual/mixed/extended reality (AR/VR/MR/XR), autonomous driving, robots, drones, and security surveillance. Single-photon avalanche diodes (SPADs) have gained significant attention due to their exceptional sensitivity and fast response time. SPADs offer unique advantages in photon counting applications, enabling the detection of a single photon with high accuracy and temporal resolution. In recent years, several groups have enhanced the performance of SPADs, especially for such crucial parameters as the wider depletion region and the higher photon detection probability (PDP) [1]–[7]. For these efforts, it is essential to consider the specific requirements of the target applications. One important application is long-range LiDAR systems that are needed for autonomous vehicles and drones where high performance and reliability are critical factors, for which the higher PDP offers numerous advantages in terms of detection range, frame rate, power consumption, etc. However, the approach has some drawbacks when applied to short/mid-range LiDAR applications. The applications require close-range object detection with precise distance measurement. In these applications, maintaining a certain level of PDP with a higher breakdown voltage (V_B) for the wide depletion region can lead to higher power consumption. Timing jitter, another crucial aspect of SPAD performance, refers to the uncertainty in the detection time of incoming photons. Lower timing jitter leads to higher temporal resolution, enabling precise timestamping of the photons and facilitating more accurate event reconstruction. Achieving low timing jitter is particularly challenging for the previous approaches due to the wide depletion regions and the non-isolated SPAD structures in the back-illuminated (BI) process. In this paper, we propose a SPAD with a significantly reduced V_B of 15 V but with superior temporal resolution. This breakthrough is achieved through innovative device engineering and advanced fabrication techniques. By reducing the V_B, our SPAD offers improved power consumption efficiency and enables seamless integration with low-voltage electronic systems. In addition, we present a comprehensive analysis of the timing jitter characteristics of the proposed SPAD. We have achieved a remarkable timing jitter performance at the excess bias voltage (V_E) of 5 V. This achievement surpasses the state-of-the-art BI SPADs and demonstrates the significant improvement in temporal resolution offered by the proposed device. The reduced timing jitter enables more precise measurement, enhancing the overall performance and capabilities of SPAD-based short/mid-range LiDAR for several mobile applications.

II. Technology and Device Structure

A. Technology

Fig. 1 shows a transmission electron microscopy (TEM) image of the BI SPAD developed with SK hynix Inc. stacked 40 nm CIS technology. The thickness of the silicon after the backside etching and thinning process is about 4 μm. This thickness was determined carefully to optimize the performance of the SPAD, especially for lower timing jitter to maximize temporal resolution performance, and to minimize the noise from the surface of the silicon. The anti-reflection coating is on top of the SPAD, and the metal reflector is at the bottom of the SPAD to optimize the absorption of the near-infrared (NIR) photons.

B. SPAD Structure

The PN junction is realized with highly doped P-type and lowly doped N-type implantations for achieving a low V_B. The whole SPAD region is covered by retrograded deep N-type implantation for isolation from the P-type silicon substrate. In addition, P-epi between the anode and cathode has the role of the virtual guard ring (GR) to prevent premature edge breakdown (PEB). The PN junction is 2.5 μm and the width of the GR covering the junction is 1.5 μm. The total pixel pitch of the SPAD including the cathode is 7.5 μm. The avalanche multiplication region of the SPAD is closed to the bottom of the silicon as shown in Fig. 1. Thanks to the isolation of the SPAD from the backside surface with the deep N-type implantation, the carriers induced by defects at the backside

surface can be blocked not to trigger avalanche multiplication. Thanks to the optimized drift region and the isolated structure, the proposed BI SPAD can provide superior timing performance compared to the state-of-the-art BI SPADs with longer drift regions shown in Fig. 2 [1], [4].

III. Simulation and Measurement Results

Figs. 3(a) and (b) depict the TCAD simulation results of the SPAD, illustrating the E-field profiles at the V_B and the V_E of 5 V, respectively. The SPAD exhibits no PEB and demonstrates a uniform E-field throughout the entire junction area. Fig. 4 shows the light-emission test (LET) results indicating a consistent E-field at the junction, which is sufficiently strong to trigger avalanche multiplication.

Fig. 5 shows the current-voltage characteristics of the BI SPAD. The SPAD has a low V_B of 15 V thanks to the higher P-type implantation for a junction. The inset of Fig. 5 shows V_B variation measured with 10 different dies. The distribution of V_B is 15 V ~ 15.1 V, which implies excellent process uniformity. The dark count rate (DCR) was measured as a function of V_E from 0.5 V to 5 V using a 200 kΩ passive quenching resistor and the result is depicted in Fig. 6. The 10 different dies were used to check its distribution and the normalized DCR at V_E of 5 V is about 550 cps/μm^2. Temperature dependency of the DCR is also characterized using an environmental chamber at the temperature from -30 to 90 ℃ with 15 ℃ steps and the results are shown in Fig. 7. The normalized DCR at V_E of 5 V in 90 ℃ is about 7000 cps/μm^2. And the V_B distribution with varying temperatures is shown in Fig. 8. The coefficient for V_B dependence on temperature is about 13 mV/K. The V_B difference between 90 ℃ and the room temperature is less than 1 V. These results demonstrate that our SPAD is very stable against temperature. To analyze the sources of the DCR, activation energy (E_a) values were estimated using the Arrhenius plots depicted in Fig. 9. The activation energy values at the lower and higher temperature (E_{a1} *and* E_{a2}) are about 0.27 eV and 0.47 eV, respectively. From these, the major noise source can be regarded as tunneling below room temperature and trap-assisted thermal generation above room temperature.

The PDP is characterized as a function of the wavelength with V_E = 1 V to 5 V and the results are shown in Fig. 10. At V_E = 5 V, the proposed BI SPAD has a PDP of 24% at 905 nm and 21% at 940 nm, respectively. Because the structure of the SPAD is isolated from the backside surface of the silicon using the deep N-type implantation, the cut-on wavelength of around 450 nm is observed. The PDP gradually increases with increasing V_E, even if V_E = 2 V, the PDP at 905 nm is about 10%, good enough for short/mid-range applications such as mobile applications. In order to verify the integrity of the PDP measurement, the inter-avalanche time histogram was also checked as shown in Fig. 11. It can be seen that the afterpulsing probability is negligible and the PDP measurement only includes the primary pulses generated by the photons. The timing jitter performance is measured using the time-correlated single-photon counting (TCSPC) technique with a 940 nm picosecond pulsed laser at three different V_E as shown in Fig. 12. The FWHM value at V_E of 5 V is 56 ps including the jitter of the laser and laser driver. For the lower V_E value of 3 V, the FWHM is still good enough, 65 ps.

IV. State-of-the-Art Comparisons

Fig. 14 shows the comparison in terms of the timing jitter and V_B with the state-of-the-art BI SPADs reported so far. Without any after-process, e.g., biasing at the middle of the silicon or at the surface of the silicon, our SPAD achieves excellent timing jitter performance at the wavelength of 940 nm while having lower V_B. Also, the comparison in terms of timing jitter and PDP are shown in Fig. 15. Finally, Table 1 summarizes and compares the state-of-the-art SPADs reported to date. The SPAD reported in this paper has been fabricated in the most advanced CIS technology, providing excellent timing jitter with a low breakdown voltage.

V. Conclusion

We present a high-performance BI SPAD fabricated in stacked 40 nm CIS technology. Thanks to the device design optimization and excellent process quality, it achieves about 56 ps timing jitter at 940 nm at V_E = 5 V and the low V_B of 15 V. We expect this SPAD can play a key role in short/mid-range LiDAR applications, especially where high temporal resolution is required.

Acknowledgment

The authors are grateful to SK hynix Inc. collaborators (especially Minseok Shin, Kwang June Sohn, Ji-Hoon Cho, and Kangbong Seo) for their help and support. This paper was the result of the research project supported by SK hynix Inc. This work was supported by the Korea Institute of Science and Technology (KIST) Institution Program (Grant No. 2E32242) and the National Research Foundation of Korea (NRF) (Grant No. 2021M3D1A2046731).

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[5] S. Shimada *et al*., "A Back Illuminated 6 μm SPAD Pixel Array with High PDE and Timing Jitter Performance," *Int. Electron Devices Meeting*, Dec. 2021.

[6] K. Morimoto *et al*., "3.2 Megapixel 3D-Stacked Charge Focusing SPAD for Low-Light Imaging and Depth Sensing," *Int. Electron Devices Meeting*, Dec. 2021.

[7] Angelo Gulinatti *et al*., "Custom Silicon Technology for SPAD-Arrays with Red-Enhanced Sensitivity and Low Timing Jitter," *Opt. Express*, vol. 28, no. 3, Feb. 2021.

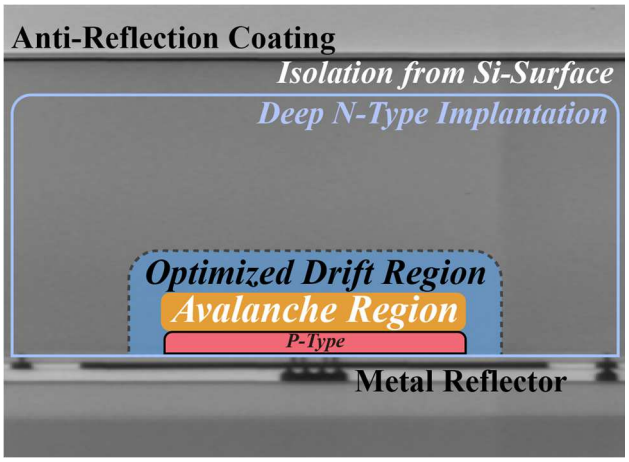


Fig. 1. A TEM image of the proposed BI SPAD.

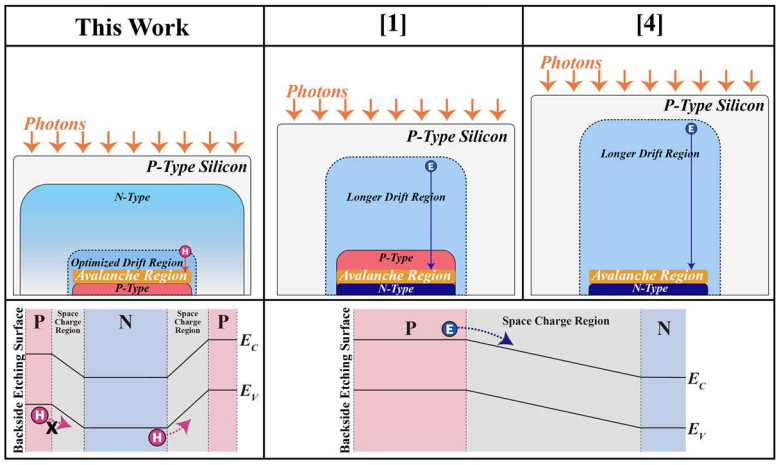


Fig. 2. Simplified X-section images for comparisons with the state-of-the-art SPADs.

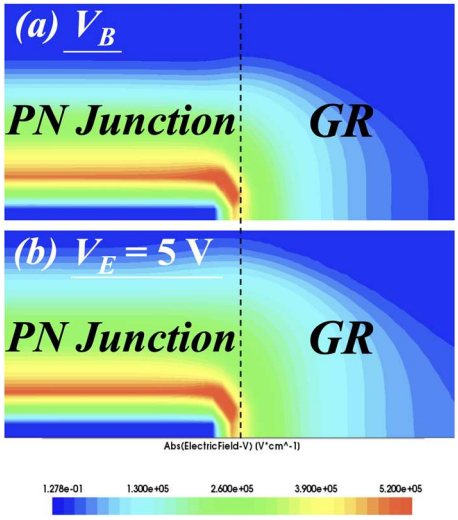


Fig. 3. TCAD simulation results of the proposed BI SPAD: E-field profiles (a) at V_B and (b) at V_E = 5 V.

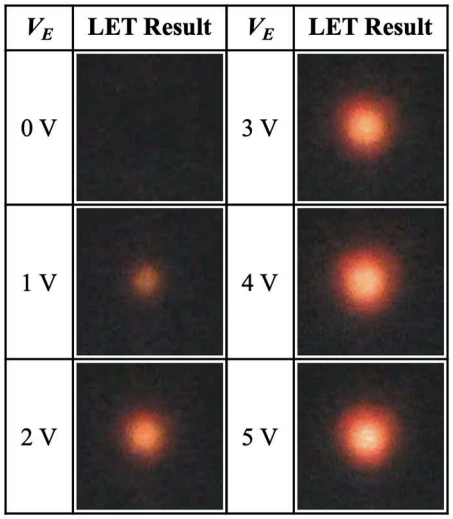


Fig. 4. Light-emission test results of the BI SPAD from V_B to V_E = 5 V.

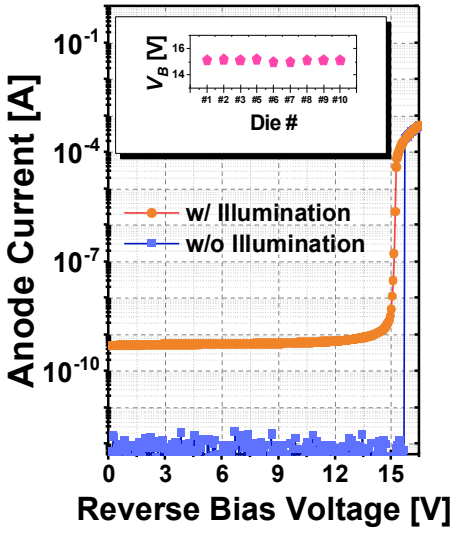


Fig. 5. Current-voltage characteristics with and without illumination.

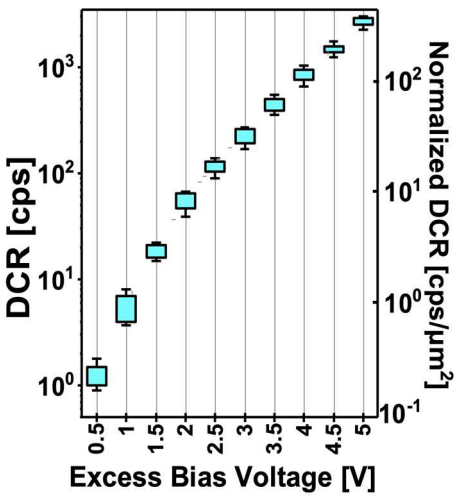


Fig. 6. DCR results obtained with 10 different dies as a function of V_E.

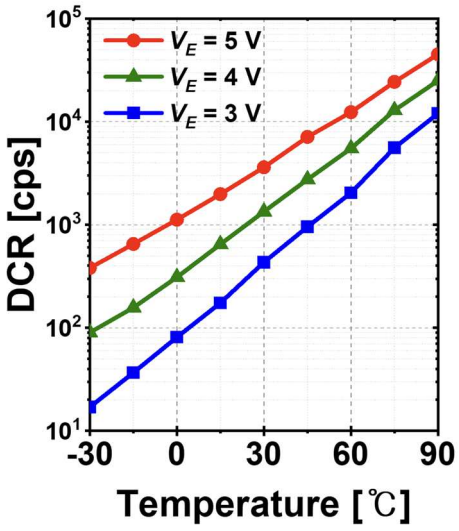


Fig. 7. Temperature-dependent DCR of the proposed BI SPAD.

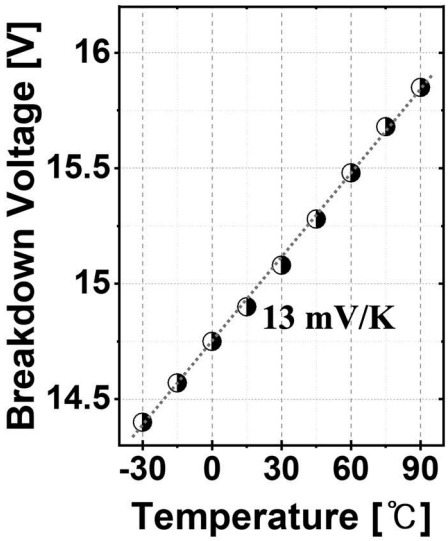


Fig. 8. Temperature-dependent breakdown voltage.

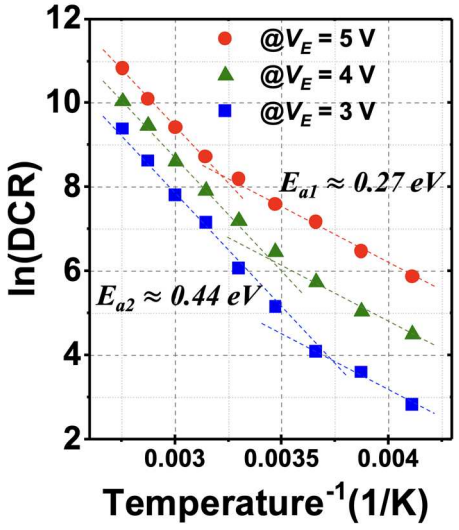


Fig. 9. Arrhenius plot of the BI SPAD.

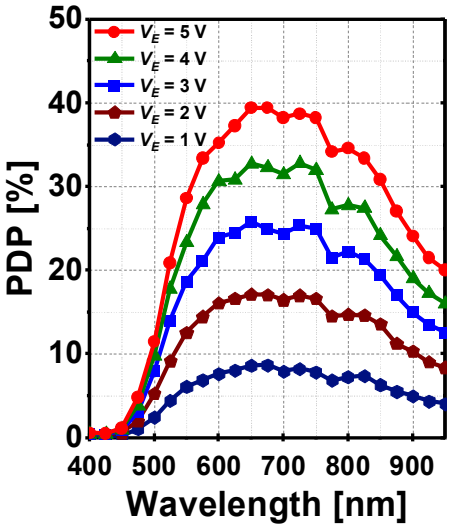


Fig. 10. PDP as a function of the wavelength at 5 different V_E.

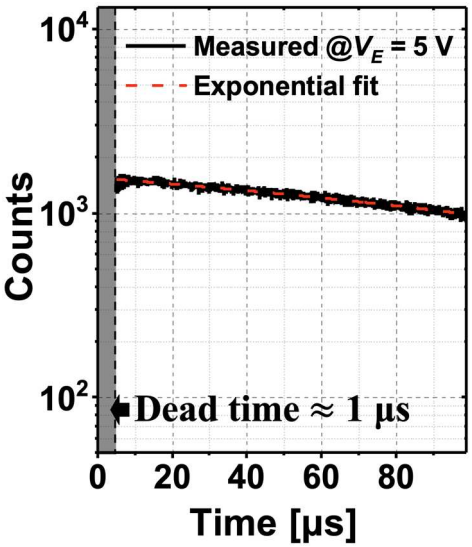
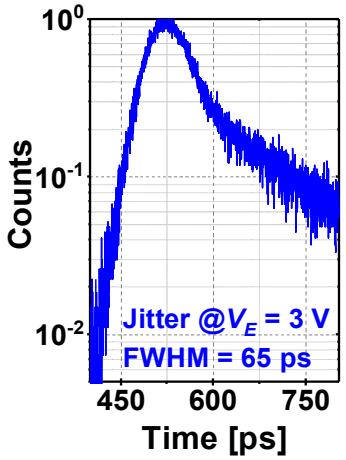
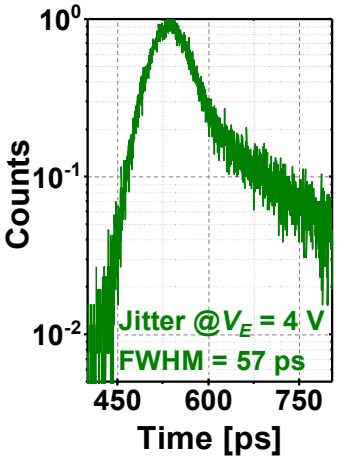


Fig. 11. Inter-avalanche time histogram of BI SPAD at V_E = 5 V.





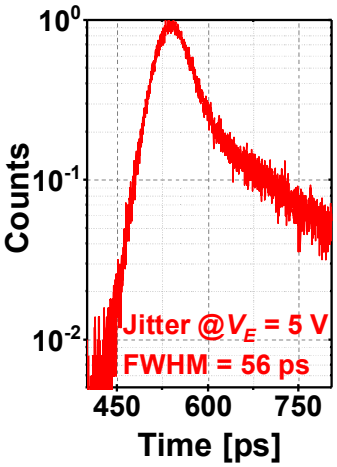


Fig. 12. Timing jitter results at three different excess bias voltages (a) V_E = 3 V, (b) V_E = 4 V, and (c) V_E = 5 V.

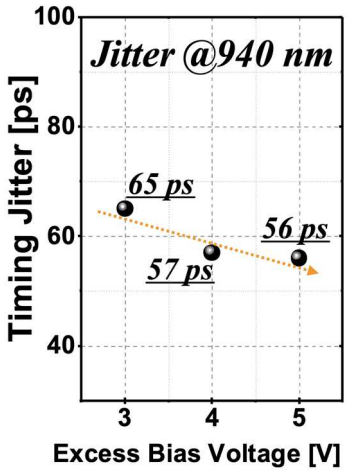


Fig. 13. FWHM values as a function of V_E.

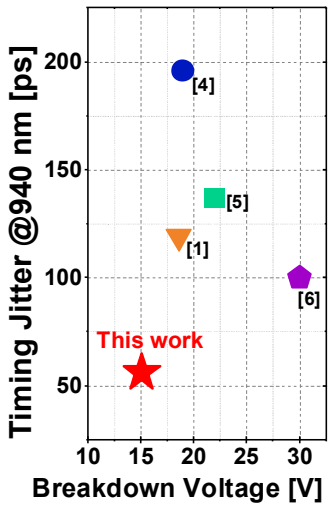


Fig. 14. Comparison: Breakdown voltage vs timing jitter @940 nm.

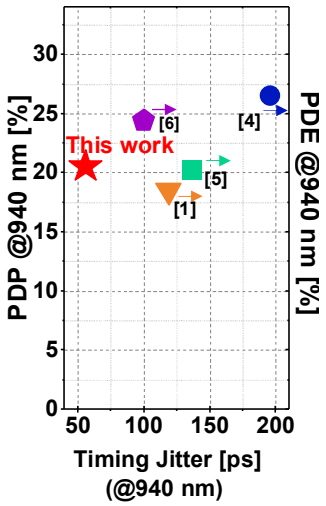


Fig. 15. Comparison: Timing jitter @940 nm vs PDP(PDE) @940 nm.

Parameter	This Work	[1]	[2]	[3]	[4]	[5]	[6]	[7]
Technology [nm]	**40**	65/40	55	90	90	90	90/40	Custom
Pixel Pitch [µm]	**7.5**	10.17	8.5	3.06	3.3	6	6.39	250
V_B [V]	**15**	18.6$^{\alpha}$	23	20.9	19	22	30	25
V_E [V]	**5**	2.5	3	3	3	3	2.5	20
DCR [cps/µm^2]	**550**	810$^{\alpha,\beta}$	31.2	-	2.2$^{\beta}$	19$^{\beta}$	0.044$^{\beta}$	-
PDP@940nm [%]	**21**	18.5$^{\alpha,\gamma}$	8.3	-	26.5$^{\gamma}$	20.2$^{\gamma}$	24.4$^{\gamma}$	14$^{\varepsilon}$
PDP@905nm [%]	**24**	23$^{\alpha,\gamma}$	11	-	-	32$^{\gamma}$	28$^{\gamma}$	22$^{\varepsilon}$
Timing Jitter @ 940nm [ps]	**56**	119$^{\alpha}$	96$^{\delta}$	-	196	137	100	95$^{\zeta}$

$^{\alpha}$@60 °C, $^{\beta}$cps/pix, $^{\gamma}$PDE w/ microlens, $^{\delta}$@850 nm, $^{\varepsilon}$PDE, $^{\zeta}$@820 nm

Table 1. Comparison with the state-of-the-art SPADs.