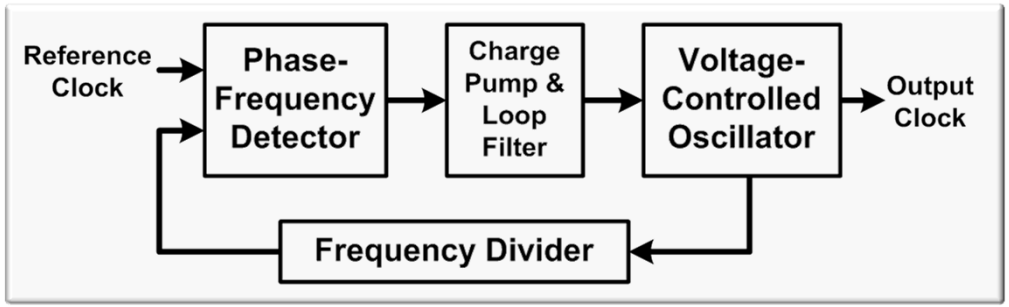
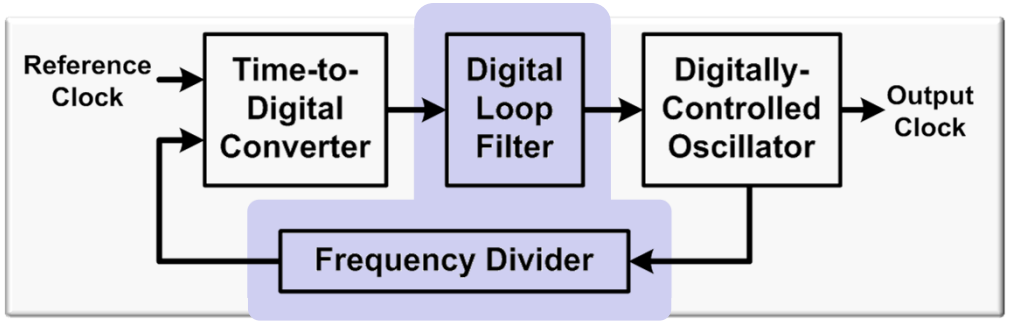
All-Digital PLL with PVT Compensation

Conventional Charge-Pump PLL



- Passive components for loop filter consume large chip size.
- Leakage current degrades jitter performance.

Alternative: All-Digital PLL



PVT-independent

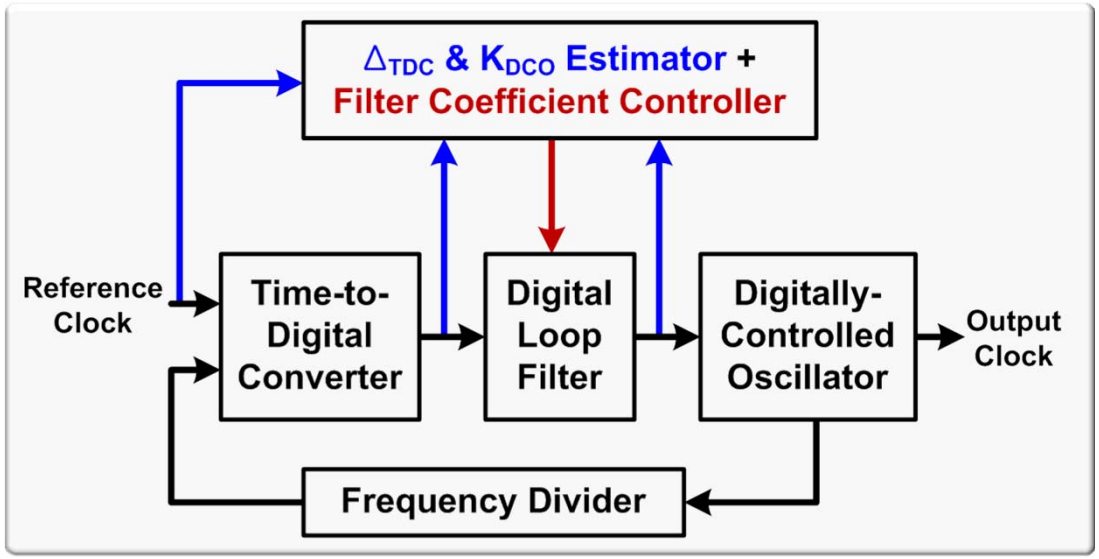
- Large-size passive components are not required.
- There's no need to worry about leakage current.
- DLF & FD are PVT-independent.

	Input	Output
TDC	Analog Phase or Frequency Error	Digital Code
DCO	Digital Code	Analog Frequency

TDC & DCO can't be independent to PVT variation.

All-Digital PLL with PVT Compensation

ADPLL with PVT Compensation



1. TDC gain (Δ_{TDC}) and DCO gain (K_{DCO}) are estimated.
2. DLF coefficients are adjusted in accordance with Δ_{TDC} and K_{DCO} variation.
3. Loop dynamics is calibrated in real time.

→ Jitter characteristic can be fixed as intended.

Results:

- (Paper) "A Time-To-Digital Converter based on a Multi-Phase Reference Clock and a Binary Counter with a Novel Sampling Error Corrector", *IEEE Transactions on Circuits and Systems – II*.
- (Patent) "고해상도 저잡음 디지털 제어 발진기", *대한민국 특허.*
- (Patent) "DIGITAL PHASE LOCKED LOOP HAVING INSENSITIVE JITTER CHARACTERISTIC FOR OPERATING CIRCUMSTANCES", *U.S. Patent.*