SECOND ANNOUNCEMENT AND CALL FOR PAPERS

2023 SYMPOSIUM ON VLSI TECHNOLOGY AND CIRCUITS

~ Rebooting Technology and Circuits for a Sustainable Future ~

Rihga Royal Hotel Kyoto, Japan
Sunday–Friday, June 11–16, 2023

June 11 Workshops
June 12 Short Courses
June 13–15 Technical Sessions
June 16 Forum

Paper Submission Deadline: 23:59 JST Wednesday, February 1, 2023
Details: www.vlsisymposium.org

Symposium Scope

The Symposium calls for papers in the following areas:

- **Advanced CMOS and interconnect technologies**
- **Advanced packaging, 2.5D and 3D integration**
- **Advanced process and material for scaling and new devices**
- **Beyond CMOS, such as spin logic, optical and quantum computing**
- **Biomedical devices, circuits, and systems**
- **Data converters**
- **Device physics, characterization, reliability, and modelling**
- **Devices and accelerators for machine learning**
- **Digital circuits, hardware security, signal integrity, IOs**
- **DTCO and design enablement**
- **Frequency generation and clocking circuits**
- **Innovative Systems using FPGAs and COTS components**
- **Memory technologies, devices, circuits, and architectures**
- **Power, analog and mixed-signal devices, and circuits**
- **Processors and SoCs**
- **Sensors, imagers, IoT, MEMS, display circuits**
- **Wireless and RF devices circuits and systems**
- **Wireline and optical transceivers, optical interconnects and processors**

Paper Submission

Prospective authors must submit two-page paper abstracts to the Symposium website www.vlsisymposium.org. Accepted papers will be published *as-submitted* with **no revisions permitted**. Authors must follow detailed instructions provided in the "Authors" section of the website, including the Authors' Guide and Pre-publication Policy. **Extended versions of outstanding papers will be invited for publication in the IEEE Transaction on Electron Devices, IEEE Journal of Solid-State Circuits, and IEEE Solid-State Circuits Letters.**

Focus Sessions

In addition to the solicited topics, the Symposium will offer Focus Sessions on special areas of Technology and Circuits of joint interest, such as:

- **AR/VR/MR/Metaverse and its integration**
- **Automotive and Aerospace applications**
- **BEOL Interconnects and BPD/BSPDN**
- **Novel 3D memory devices to continue scaling DRAM, Flash, and other NVM**
- **New Computing**
- **3D Packaging Technologies and System Integration (Thermal management)**

Highlights

The 6-day Symposium will offer the following events in addition to the technical sessions:

- **Plenary Sessions**
- **Demo Session for outstanding papers**
- **Full-Day Short Courses on key VLSI topics**
- **Evening Panels**
- **Full-Day Forum**
- **Workshops**

Best Student Paper Award

Selection will be based on quality of the paper and presentation at the Symposium. The winning student will be presented with a certificate and monetary award at the 2024 VLSI Symposium opening session. **At time of submission, the student must be enrolled as a full-time student, be the leading author and presenter of the paper, and indicate consideration for the award.**

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Yusuke Oike, Sony Semiconductor Solutions

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Program Chairs:
Takaaki Tsunomura, Tokyo Electron Limited
Mototsugu Hamada, The University of Tokyo

Program Co-Chairs:
Vijay Narayanan, IBM
Ron Kapusta, Analog Devices, Inc.

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C18-2 - 8:55
A 24-OSR to Simplify Anti-Aliasing Filter 2MHz-BW 83dB-DR 3rd-Order DT-DSM Using FIA-Based Integrator and Noise-Shaping SAR Combined Digital Noise-Coupling Quantizer, M. Fukazawa and T. Matsui, Renesas Electronics Corp., Japan

This paper proposes a dynamic circuits-based discrete-time (DT) delta-sigma modulator (DSM) with 2MHz bandwidth (BW) at an oversampling ratio of 24 to simplify anti-alias filter, flexible operating frequency, and power scalability. The proposed DSM consists of floating inverter amplifier based integrators and an asynchronous SAR quantizer that combines passive noise shaping and digital noise coupling to enhance total noise shaping effect equal to the 3rd-order DSM. This DT-DSM achieves 83.1dB dynamic range while consuming 1.04mW, resulting in 175.9dB DR-based Schreier FoM.

C18-3 - 9:20
A 2.5mW 12MHz-BW 69dB SNDR Passive Bandpass ΔΣ ADC with Highpass Noise-Shaping SAR Quantizers, S. Oh*, S. Park*, Y. Jung*, K. Jimin*, C. Donghee*, S. Ha** and J. Minkyu*, *KAIST, Korea and **New York Univ. Abu Dhabi, United Arab Emirates

A 4th-order passive bandpass ΔΣ modulator (BPDSM) using a 2-path transformation structure is presented. The proposed BPDSM replaces a power-hungry resonator with a z-to-z^2-transformed passive loop filter. The prototype bandpass ΔΣ ADC provides a wide intermediate frequency (IF) range of 1.25MHz to 60MHz. The measured SNDR is 69dB with a power consumption of 2.5mW at 12MHz bandwidth when its highest sampling rate is 240MS/s.

C18-4 - 9:45
A 187dB FoMS 46fJ/Conv. 2nd-order Highpass ΔΣ Capacitance-to-Digital Converter, Y. Jung*, S. Oh*, J. Koo*, S. Park*, J.-H. Suh*, D. Cho**, S. Ha*** and M. Je*, *KAIST, **Samsung Electronics Co., Ltd., Korea and ***New York Univ. Abu Dhabi, United Arab Emirates

The proposed capacitance-to-digital converter (CDC) achieves 187dB FoM_S, which is >2x improvement over the state-of-the-art, with FoM_W of 46fJ/Conv.-Step. We employ a highpass ΔΣ modulator in CDC applications for the first time while using loop filters based on power-efficient floating inverter amplifiers (FIAs).

Technology / Circuits Joint Focus Session 3

AR/VR/MR Metaverse 2 [Shunju III]

Thursday, June 15, 8:30-9:45

Chairpersons: R. Kuroda, Tohoku Univ.
B. Rae, STMicroelectronics N.V.

JFS3-1 - 8:30 (Invited)
216 fps 672 × 512 pixel 3 µm Indirect Time-of-Flight Image Sensor with 1-Frame Depth Acquisition for Motion Artifact Suppression, C. Okada*, S. Yokogawa*, Y. Yorikado*, K. Honda*, N. Okuno*, R. Ikeno*, M. Yamakoshi*, H. Ito*, S. Yoshitsune**, M. Desaki**, S. Hida**, A. Nose*, H. Wakabayashi* and F. Koga*, *Sony, Japan

A 216 fps, 672 × 512 pixel, 3 µm indirect time-of-flight image sensor with 1-frame depth acquisition for motion artifact suppression was developed for versatile applications. To suppress motion artifacts, we employed a floating diffusion sharing circuit, vertical gate technology for the transfer gate, and IQ mosaic pixel coding with demosaic processing. Consequently, a motion artifact-free depth map was obtained, with a 3.5 times faster frame rate, 50% lower power, and 71% lower readout noise compared to a conventional 4-frame sensor.

JFS3-2 - 8:55
A 3.96µm, 124dB Dynamic Range, 6.2mW Stacked Digital Pixel Sensor with Monochrome and Near-Infrared Dual-Channel Global Shutter Capture, S. Chen*, C. Liu*, L. Bainbridge*, Q. Chao*, R. Chilukuri*, W. Gao*, A. P. Hammond*, T.-H. Tsai*, K. Miyauchi**, I. Takayanagi**, M. Nagamatsu**, H. Abe**, K. Mori**, M. Uno**, T. Isozaki**, R. Ikeno**, H.-L. Chen***, C.-H. Lin***, W.-C. Fu*** and S.-G. Wuu***, *Meta, USA, ***Brillnics Japan Inc., Japan and ****Brillnics Inc., Taiwan

Keywords: indirect time of flight, single frame, motion artifact suppression

JFS3-3 - 9:20
Doping-Optimized Back-Illuminated Single-Photon Avalanche Diode in Stacked 40 nm CIS Technology Achieving 60% PDP at 905 nm, E. Park*, **, W.-Y. Ha****, D. Eom*, **, D.-H. Ahn*, H. An***, S. Yi***, K.-D. Kim***, J. Kim***, W.-Y. Choi** and M.-J. Lee*, *Korea Institute of Science and Technology (KIST), **Yonsei Univ., ***SK hynix Inc., Korea and ****École Polytechnique Fédérale de Lausanne (EPFL), Switzerland

We report on back-illuminated single-photon avalanche diodes (SPADs) based on 40 nm CIS technology. The SPAD performance is optimized with doping engineering, enabling the extension of the effective active area resulting in much higher efficiency. It achieves a dark count rate (DCR) of 15 cps/µm², timing jitter of 97 ps, and excellent photon detection probability (PDP) in near-infrared (NIR) wavelength of about 60% at 905 nm and 44% at 940 nm at the excess bias voltage (V_E) of 2.5 V.

Doping-Optimized Back-illuminated Single-Photon Avalanche Diode in Stacked 40 nm CIS Technology Achieving 60% PDP at 905 nm

Eunsung Park[1,2], Won-Yong Ha[4], Doyoon Eom[1,2], Dae-Hwan Ahn[1], Hyuk An[3], Suhyun Yi[3], Kyung-Do Kim[3], Jongchae Kim[3], Woo-Young Choi[2,*], and Myung-Jae Lee[1,*]

[1]Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology, South Korea, email: mj.lee@kist.re.kr, [2]Department of Electrical and Electronic Engineering, Yonsei University, South Korea, [3]CIS Division, SK hynix, South Korea, [4]Institute of Electrical and Micro Engineering, École Polytechnique Fédérale de Lausanne, Rue de la Maladière 71B, Neuchatel, NE 2000, Switzerland, [*]These authors contributed equally to this work.

Abstract

We report on back-illuminated single-photon avalanche diodes (SPADs) based on 40 nm CIS technology. The SPAD performance is optimized with doping engineering, enabling the extension of the effective active area resulting in much higher efficiency. It achieves a dark count rate (DCR) of 15 cps/μm^2, timing jitter of 97 ps, and excellent photon detection probability (PDP) in near-infrared (NIR) wavelength of about 60% at 905 nm and 44% at 940 nm at the excess bias voltage (V_E) of 2.5 V.

Introduction

Single-photon sensors are highly demanded in various applications such as LiDAR, AR/VR/MR/XR, night vision, bio imaging, etc. Especially for the major emerging applications like LiDAR, the key requirements are the high detection efficiency at the near-infrared (NIR) wavelength range. In this paper, we present back-illuminated SPADs fabricated in 40 nm CIS technology, which is the most advanced CIS technology that has been used for SPAD implementation up to date. Furthermore, we have optimized SPAD performance, especially the fill factor and the efficiency, with doping engineering.

Device Structure and Simulation Result

Fig. 1 shows a transmission electron microscopy (TEM) image of the back-illuminated SPAD. With the backside thinning/etching process, the thickness of the Si epi can be controlled, and about 4 μm thick Si epi remains after the process. The SPAD is based on a shallow n-type region on a p-type region forming a 5 μm diameter main PN junction with a 2 μm guard–ring (GR) structure surrounding the edge of the junction to prevent edge breakdown. Through the p-type doping optimization over the GR and anode, the PDP can be greatly improved over the wide wavelength range. Fig. 2 shows the TCAD simulation results of the SPADs in terms of the E-field profile without and with doping optimization, respectively. The SPAD with doping optimization achieves a wider avalanche multiplication region over the whole GR area without suffering any edge breakdown compared to the SPAD without doping optimization. In addition, as shown in Fig. 2, the carrier flow becomes better with the doping optimization, i.e., the most of carriers go through the planar junction where the highest E-field is formed, which is highly desirable to improve its PDP performance.

Experimental Results and Discussion

Fig. 3(a) shows the micrograph of the back-illuminated SPAD, and Figs. 3(b) and (c) are the light-emission-test (LET) results of the SPADs without and with doping optimization, respectively, at V_E = 2.5 V. The areas emitting light in Figs. 3(b) and (c) indicate that each SPAD has a uniform E-field higher than the critical E-field of Si over the planar junction. As the two results show different light-emitting areas and intensities, we can clearly confirm that the effective active area is much wider and more avalanche processes occur in the doping-optimized SPAD. Fig. 4 presents the PDP results of the two SPADs at NIR to directly compare their detection efficiencies. It is clearly shown that the PDP has been improved more than by a factor of two. In order to investigate further the effective active area, a measurement with a laser scanning microscope was performed, and the results are shown in Fig. 5. The results show that the active region is formed not only at the junction but also in the GR with the full width at half maximum (FWHM) contour of about 8 μm. The current-voltage characteristics of the SPAD are shown in Fig. 6. The SPAD has very low dark currents of a few pAs and its breakdown voltage, V_B, is about 21.2 V. The temperature dependence of V_B was investigated from 0 to 60 °C, and the results are shown in Fig. 7. The output waveforms in terms of voltage and current pulses are shown in Fig. 8. The DCR characteristics were measured at room temperature as a function of V_E, and the results are shown in Fig. 9. The SPAD exhibits a low DCR of about 15 cps/μm^2 at V_E = 2.5 V. The DCR was also characterized at different temperatures, from 0 to 60 °C, and the device shows acceptable DCR even at 60 °C at V_E = 2.5 V as can be seen in Fig. 10. The activation energy, E_a, is about 0.837 eV at V_E = 2.5 V, extracted from the Arrhenius plot shown in Fig. 11. Fig. 12 shows the PDP characteristics of the back-illuminated SPAD as a function of the wavelength for the three different V_E. The SPAD achieves high PDP, about 60% and 44% at 905 and 940 nm, respectively, at V_E = 2.5 V, thanks to the effective SPAD structure with a metal reflector and anti-reflection coating as well as doping optimization. Fig. 13 shows the measured timing jitter of the SPAD using the time-correlated single-photon counting (TCSPC) technique with a 940 nm picosecond pulsed laser. The FWHM is about 97 ps at V_E = 2.5 V. Figs. 14 and 15 show the comparison of PDP performance with the latest back-illuminated SPADs reported so far [1]–[4]. Finally, Table I compares and summarizes the state-of-the-art SPADs reported to date.

Conclusion

We present a high-efficient back-illuminated SPAD in stacked 40 nm CIS technology. Thanks to the doping optimization as well as proper device design and excellent process quality, it can achieve about 60% PDP at 905 nm wavelength at V_E = 2.5 V, which is the highest PDP reported so far. We expect that this SPAD can play a key role in various applications, especially where high NIR efficiency is required.

Acknowledgment

This work was supported by the KIST Institution Program (Grant No. 2E32242), NRF of Korea (Grant No. 2021M3D1A2046731), and KEIT grant funded by MOTIE, Korea (Grant No. 20008757).

References

[1] T. Al Abbas *et al.*, *IEDM*, 2016. [2] M.-J. Lee *et al.*, *IEDM*, 2017. [3] K. Morimoto *et al.*, *IEDM*, 2021. [4] S. Shimada *et al.*, *IEDM*, 2021.

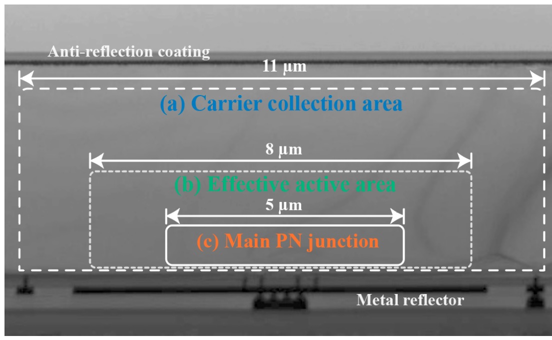

Fig. 1. Transmission electron microscopy (TEM) image of the back-illuminated SPAD: (a) carrier collection area, (b) effective active area, and (c) main junction.

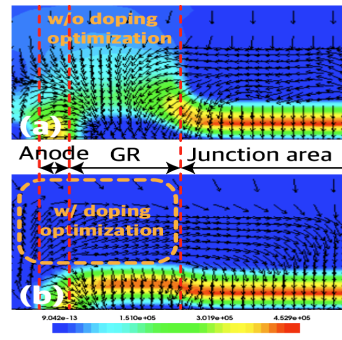

Fig. 2. TCAD simulation results for the back-illuminated SPADs: E-field profiles at $V_E = 2.5$ V.

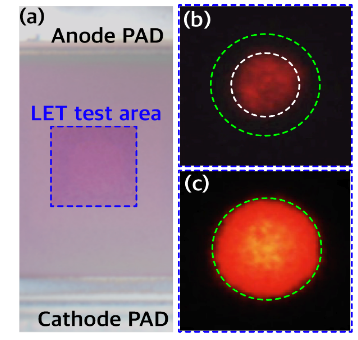

Fig. 3. (a) Micrograph of the back-illuminated SPAD and light-emission-test results (b) without and (c) with doping optimization.

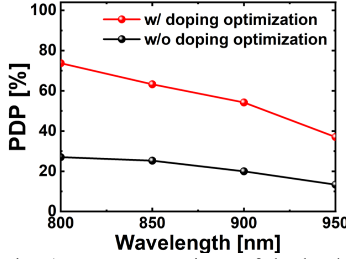

Fig. 4. PDP comparison of the back-illuminated SPADs with and without doping optimzation at $V_E = 2$ V.

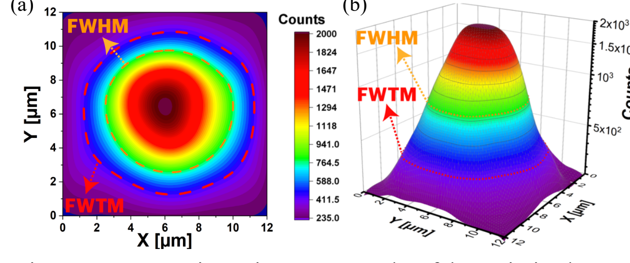

Fig. 5. Laser-scanning-microscope results of the optimized SPAD: (a) 2D contour and (b) 3D plot obtained at above its V_B.

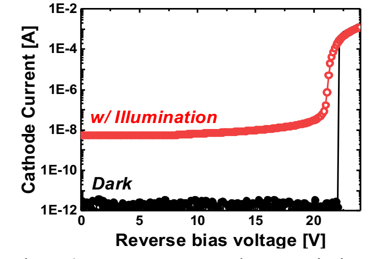

Fig. 6. SPAD I-V characteristics under the dark and illumination conditions at room temperature.

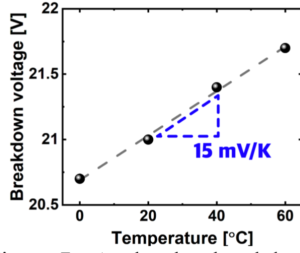

Fig. 7. Avalanche breakdown voltage variation of the SPAD as a function of temperature.

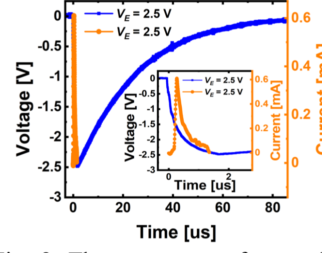

Fig. 8. The output waveforms of the SPAD: voltage and current pulses at $V_E = 2.5$ V.

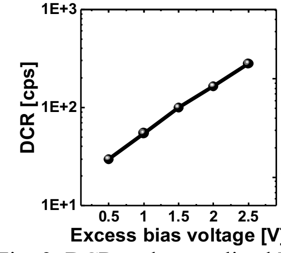

Fig. 9. DCR and normalized DCR as a function of V_E at room temperature.

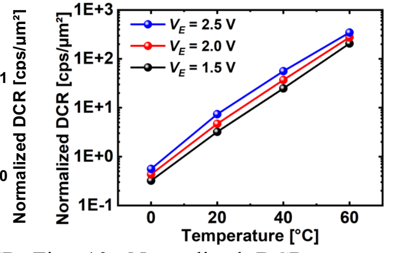

Fig. 10. Normalized DCR as a function of temperature at the three different excess bias voltages.

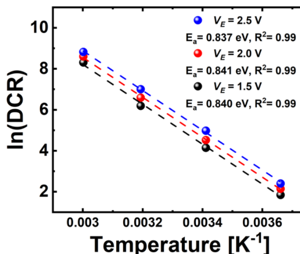

Fig. 11. Arrhenius plots with extracted activation energies and the coefficients for the curve fits at the three different excess bias voltages.

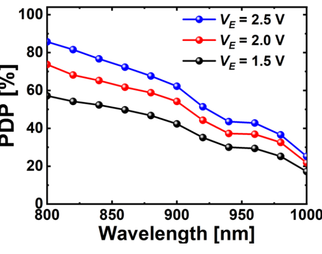

Fig. 12. NIR PDP values as a function of wavelength at the three different excess bias voltages.

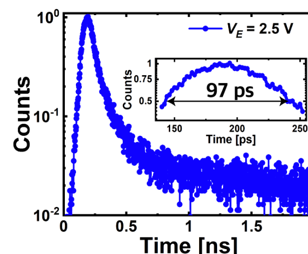

Fig. 13. Timing jitter measurement results at $V_E = 2.5$ V when using a 940 nm picosecond pulsed laser.

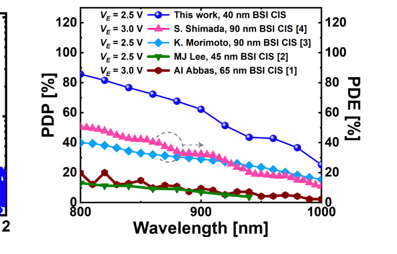

Fig. 14. PDP comparison with the state-of-the-art back-illuminated SPADs.

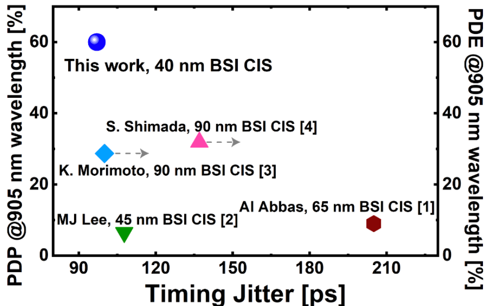

Fig. 15. Performance comparison of back-illuminated SPADs: PDP at 905 nm vs.timing jitter.

	Technology	Pixel pitch	V_B	V_E	DCR	PDP @905 nm	Timing jitter
[1]	65 nm CIS	7.83 μm	12 V	3 V	391.4 cps/μm²	9%	205 ps (@773 nm)
[2]	45 nm CIS	19.5 μm	28.5 V	2.5 V	55.4 cps/μm²	6.5%	107.7 ps (@637 nm)
[3]	90 nm CIS	6.39 μm	30 V	2.5 V	0.044 cps/μm²	28.7%*	100 ps (@940 nm)
[4]	90 nm CIS	6 μm	22 V	3 V	0.5 cps/μm²	31.9%*	137 ps (@ 940 nm)
This work	**40 nm CIS**	**11 μm**	**21.2 V**	**2.5 V**	**15 cps/μm²**	**60%**	**97 ps (@940 nm)**

*Photon detection efficiency (PDE) with microlens

Table I: The state-of-the-art SPAD performance comparison.

VLSI 2023 - Presentation

- Session: Joint Focus Session 3 - AR/VR/MR Metaverse 2

SYMPOSIUM

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Doping-Optimized Back-Illuminated Single-Photon Avalanche Diode in Stacked 40 nm CIS Technology Achieving 60% PDP at 905 nm

Eunsung Park[1,2], Won-Yong Ha[4], Doyoon Eom[1,2], Dae-Hwan Ahn[1], Hyuk An[3], Suhyun Yi[3], Kyung-Do Kim[3], Jongchae Kim[3], Woo-Young Choi[2], and Myung-Jae Lee[1]

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