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CLEO Pacific Rim 2024

August 4 ~ 9, 2024
Songdo Convensia,
Incheon, Korea

The 16th Pacific Rim Conference on Lasers and Electro-Optics

CLEO PacificRim 2024

E-Proceedings

ORGANIZER OSK 한국광학회 Optical Society of Korea

SUPPORTER Incheon Metropolitan City Incheon Tourism Organization

August 5 (Mon.)

	Room A 102	Room B 104	Room C 107	Room D 113	Room E 114	Room F 115	Room G 116	Room H 117	Room I 118	Room J 201	Room K 204	Room L 206	Lobby
	1F									2F			1F
9:30-10:00	Opening Ceremony (Grand Ballroom AB, 2F)												
10:00-10:30	Coffee Break												
	Mo1A	**Mo1B**	**Mo1C**	**Mo1D**	**Mo1E**	**Mo1F**	**Mo1G**	**Mo1H**	**Mo1I**	**Mo1J**	**Mo1K**	**Mo1L**	
10:30-12:00	Inverse Design for Metamaterials I	Ultrafast and Nonlinear Optics in Emerging Materials I	Quantum Optics and Quantum Information I	Heterogeneous Integration 1: Lithium Niobate	Optical Metrology I	Low-dimensional Photonics I	Molecular Sensing	Solid-State Lasers I	mmWare / THz / FSO Communications	Topology and Photonics I	Short-Haul Systems	Biophotonic Imaging I	
12:00-13:30	Lunch (on your own)												
	Mo2A	**Mo2B**	**Mo2C**	**Mo2D**	**Mo2E**	**Mo2F**	**Mo2G**	**Mo2H**	**Mo2I**	**Mo2J**	**Mo2K**	**Mo2L**	
13:30-15:00	Inverse Design for Metamaterials II	Ultrafast and Nonlinear Optics in Emerging Materials II	Cold Atoms I	Advances in Light Sources 1	Optical Metrology II	Metasurface	Photonic Device & Sensing I	Raman Lasers / Amplifiers	Communications based on Microwave Photonics	Topology and Photonics II	Optical Devices for Telecom Applications	Biophotonic Imaging II	Exhibition
15:00-15:15	Coffee Break												
	Mo3A	**Mo3B**	**Mo3C**	**Mo3D**	**Mo3E**	**Mo3F**	**Mo3G**	**Mo3H**	**Mo3I**	**Mo3J**	**Mo3K**	**Mo3L**	
15:15-16:45	Specialty Fibers	Ultrafast and Nonlinear Optics in Emerging Materials III	Trapped Ions and Interfaces	Advances in Light Sources 2	Dimensional Metrology I	Signal Processing based on Microwave Photonics	Photonic Device & Sensing II	Ultrafast Lasers	Laser Cutting	THz Spectroscopy	Switching Systems	Ultrahigh Intensity Laser	
16:45-17:00	Coffee Break												
	Mo4A	**Mo4B**	**Mo4C**	**Mo4D**	**Mo4E**	**Mo4F**	**Mo4G**	**Mo4H**	**Mo4I**	**Mo4J**	**Mo4K**	**Mo4L**	
17:00-18:30	Fiber Lasers	Ultrafast and Nonlinear Optics in Emerging Materials IV	Quantum Information Processing	Novel Active Devices	Dimensional Metrology II	System Applications of Microwave Photonics	Photonic Device & Sensing III	Solid-State Lasers II	Laser Surface Treatment	Infrared/THz Source and Device	Amplified Transmission Systems	High Energy Laser	
18:30-20:00	Get-Together Party (Grand Ballroom Lobby, 2F)												

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Session Title:	[Mo1K] Short-Haul Systems
Session Date:	August 5 (Mon.), 2024
Session Time:	10:30-12:00
Session Room:	Room K (204-205)
Session Chair(s)	Prof. Sunghyun Bae (Kangwon Nat'l Univ., Korea)

[Mo1K-1] [Tutorial] 10:30-11:15

Enhancing Fiber-to-The-Room (FTTR) Technologies: Addressing Key Challenges and Solutions

Gangxiang Shen, Jun Li, Jinhan Cai, Mingyuan Zan, and Shen Yu (Soochow Univ., China)

[Mo1K-2] 11:15-11:30

Precoding-assisted Inter-ONU Interference Alleviation in OFDM-NOMA-PON System

Geyang Wang (The Chinese Univ. of Hong Kong, Hong Kong S.A.R), Xiaohao Chen (The Univ. of Hong Kong, Hong Kong S.A.R), and Lian-Kuan Chen (The Chinese Univ. of Hong Kong, Hong Kong S.A.R)

[Mo1K-3] 11:30-11:45

4 x 50 Gb/s 0.85 pJ/bit PAM-4 CMOS VCSEL Driver for Linear Pluggable Optics

Jun-Seo Kim, Kihun Kim (Yonsei Univ., Korea), Tae Hwan Jin, Pyung-Su Han (Qualitas Semiconductor Co., Ltd., Korea), and Woo-Young Choi (Yonsei Univ., Korea)

[Mo1K-4] 11:45-12:00

Multi-tap DFE with State-tracking Demapper for IM-DD Systems

Zhengyu Ma, Jing Zhang, Jiahao Zhou, Xue Zhao, Rui Wang, and Kun Qiu (Univ. of Electronic Science and Tech. of China, China)

4 x 50 Gb/s 0.85 pJ/bit PAM-4 CMOS VCSEL Driver for Linear Pluggable Optics

Jun-Seo Kim[1,2], Kihun Kim[1], Tae Hwan Jin[2], Pyung-Su Han[2], Woo-Young Choi[1]
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Abstract: We present a pulse amplitude level-4 (PAM-4) CMOS VCSEL driver that can be used in linear pluggable optics (LPO) applications. Optimization of the driver IC is achieved with VCSEL equivalent circuit model.
OCIS codes: 060.0060, 060.2330.

1. Introduction

Demands for various cloud-based services including AI/ML are greatly increasing and the amount of data traffic inside the data center (DC) are rapidly growing. Since electrical interconnects based on copper channels suffer from channel loss especially for the increased data rates, the need for optical interconnect solutions inside DC are increasing. In particular, the pluggable optical modules based on the 850-nm vertical-cavity surface emitting laser (VCSEL) together with multi-mode (MM) fiber are finding greater acceptance due to their high performance and cost effectiveness [1]. Pluggable optical modules have utilized digital signal processors (DSPs) to enhance the performance, but due to the power consumption and cost requirements LPO modules without DSP are receiving a lot of R&D attention. Without DSP, however, the performance requirements for VCSEL driver ICs as well as receiver circuits are much stringent and very careful design of driver and receiver ICs are required. In this paper, we report a 50 Gb/s PAM-4 VCSEL driver IC that can compensate the VCSEL nonlinearity with a newly proposed pre-distortion scheme.

2. PAM-4 CMOS Linear Driver

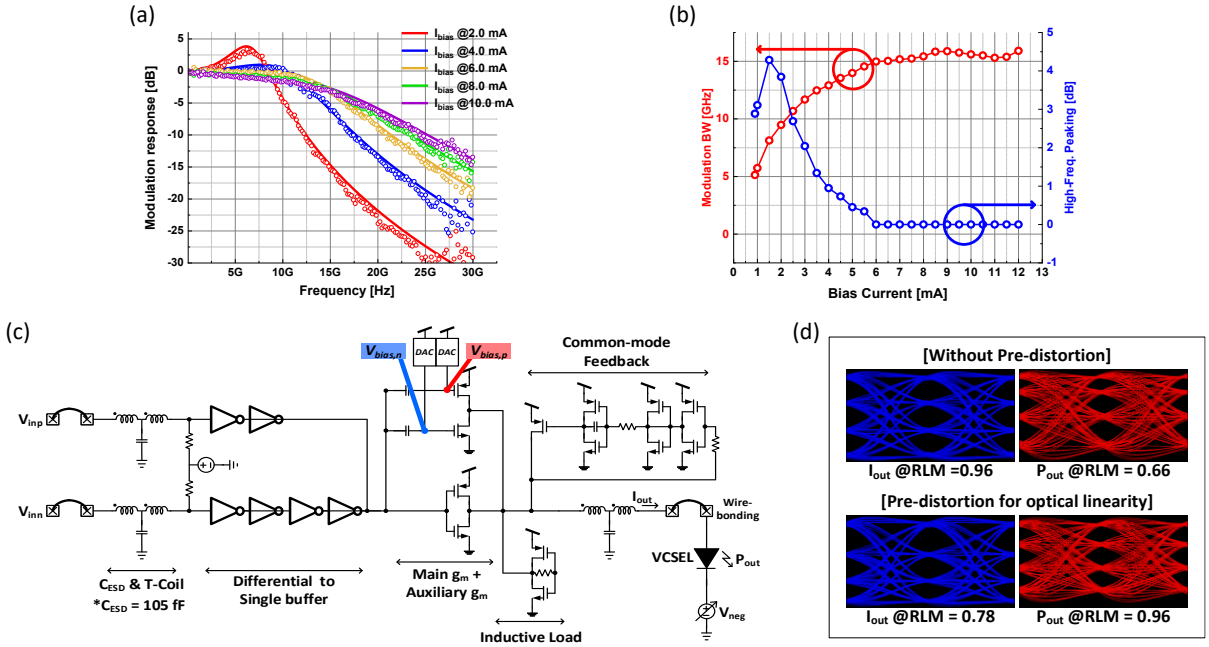

Fig. 1. (a) VCSEL modulation responses: simulated results with the VCSEL circuit model and measurement results. (b) VCSEL modulation bandwidth (red) and high-frequency peaking (blue) according to bias current. (c) VCSEL driver IC architecture. (d) 50 Gb/s PAM-4 simulation results with and without pre-distortion.

The performance of the VCSEL driver must be optimized for the target VCSEL device and for this co-simulation of the driver IC together with VCSEL in the standard IC design environment is necessary. For this, an accurate and IC-simulation-friendly VCSEL equivalent circuit model for a target VCSEL device was newly developed [2]. The target VCSEL is a commercial device with the modulation bandwidth of 15 GHz at I_{bias} = 7 mA.

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Fig. 1(a) shows the normalized modulation response of the VCSEL for different bias currents. In the figure, empty circles represent the measured results, while solid lines represent simulated results of the equivalent circuit model. At currents above 6 mA, there is no high-frequency peaking, and the bandwidth saturates as can be seen in Fig. 1(b). In order to reduce dynamic non-linearity, the driver IC was designed so that the modulation currents change in the range of 6 mA to 10 mA. Fig. 1(c) illustrates the architecture of the VCSEL driver, including electro-static discharge (ESD) protection circuit having C_{ESD} = 105 fF and T-coils used for compensating the bandwidth reduction due to C_{ESD}. The differential-to-single buffer employs the g_m/g_m buffer structure, which has low total harmonic distortion (THD) [3]. Due to the VCSEL nonlinearity, the ratio of level mismatch (RLM), a key performance parameter for PAM-4 modulation, can be degraded. In the driver IC, the core block following the buffer pre-distorts the modulating signals so that this nonlinearity can be compensated. Fig. 1(d) shows post-layout simulation results of 50 Gb/s PAM-4 eye diagrams demonstrating the effect of the pre-distortion. The blue eye-diagram represents the eyes for VCSEL modulation current, while the red eye-diagram represents the modulated VCSEL optical output. With pre-distortion, RLM is improved from 0.66 to 0.96. The limited VCSEL bandwidth is compensated by the inverter-typed inductive load. In addition, a self-referenced common mode feedback maintains the output DC voltage at VDD/2 and serves to source I_{bias} when a negative bias voltage is applied to the cathode of the VCSEL device.

3. Measurement Results

The micrograph of the 4-channel driver IC fabricated in CMOS 14 nm FinFET process can be seen in Fig. 2(a). Fig. 2(b) shows 25 Gb/s NRZ (left) and 50 Gb/s PAM-4 (right) optical measurement results of the transmitter including the driver IC and the VCSEL device. For these measurements, $V_{in\_p\text{-}p}$ = 360 mV with PRBS-7 data is supplied to the driver IC, and modulation is performed at I_{bias} = 8 mA. Measured optical modulation amplitudes (OMAs) are 3.02 dBm for NRZ, 2.55 dBm for PAM-4 with RLM = 0.96. The driver IC energy efficiency excluding the buffer is 0.85 pJ/bit.

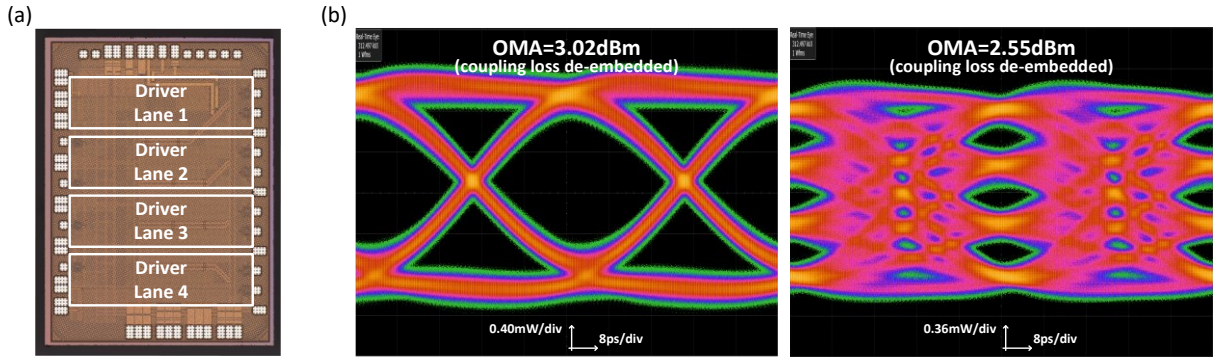

Fig. 2. (a) Micrograph of 4-channel driver IC. (b) Measurement results of 25 Gb/s NRZ (left), 50 Gb/s PAM-4 (right) optical eye-diagram for transmitter with PRBS-7 pattern, $V_{in,p\text{-}p}$ = 360 mV, I_{bias} = 8 mA.

4. Conclusion

A 4 x 50 Gb/s 0.85 pJ/bit PAM-4 VCSEL driver IC fabricated in 14-nm CMOS FinFET technology is reported that can be used in linear pluggable optics (LPO) applications. For design optimization, the driver IC was co-simulated with the new VCSEL equivalent circuit model. The driver IC contains the pre-distortion block that can compensate the VCSEL nonlinearity. With this, 50 Gb/s PAM-4 modulation with RLM = 0.96 is achieved.

References

[1] D. Mahgerefteh et al., "Techno-Economic Comparison of Silicon Photonics and Multimode VCSELs," in Journal of Lightwave Technology, vol. 34, no. 2, pp. 233-242, 15 Jan.15, 2016, doi: 10.1109/JLT.2015.2483587.

[2] K. Kim, J.-S. Kim, et al., “A Large-Signal SPICE Model for VCSEL Based on Piece-wise Linear RLC Elements”, submitted to publication.

[3] K. R. Lakshmikumar et al., "A Process and Temperature Insensitive CMOS Linear TIA for 100 Gb/s/λ PAM-4 Optical Links," in IEEE Journal of Solid-State Circuits, vol. 54, no. 11, pp. 3180-3190, Nov. 2019, doi: 10.1109/JSSC.2019.2939652