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ADVANCE PROGRAM

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Session	**10: Advanced Wireline Transceiver Techniques**
Time	Tuesday, Nov. 7th, 10:50-12:30
Venue	Coral Hall
Session Chair	Peng Liu, Zhejiang University
Session Co-Chair	Ilmin Yi, GIST

10-1 **10:50~11:15**

A 4×112-Gb/s PAM-4 Silicon-Photonic Transceiver Front-End for Linear-Drive Co-Packaged Optics

Han Liu[1'2], Nan Qi[1'2], Donglai Lu[1'2], Zizheng Dong[1], ZhihanZhang[1'2], Jian He[1], Guike Li[1'2], Leliang Li[1'2],

Ye Liu[3], Ziyue Dang[3],Daigao Chen[3'4], Zhao Zhang[1'2], Jian Liu1'2, Nanjian Wu[1'2], XiXiao[3'4], Liyuan Liu[1'2]

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10-2 **11:15~11:40**

A 80Gb/s/pin Single-Ended PAM-4 Transmitter with an Edge Boosting Auxiliary Driver and a 4-Tap FFE in 28-nm CMOS

Dae-Won Rho[1], Jae-Koo Park[12], Seung-Jae Yang[1] and Woo-YoungChoi[1]

[1]Yonsei University

[2]Samsung Electronics

10-3 **11:40~12:05**

A 2 × 24Gb/s Single-Ended Transceiver with Channel-Independent Encoder-Based Crosstalk Cancellation in 28nm CMOS

Hongzhi Wu, Weitao Wu, Liping Zhong, Xuxu Cheng, Xiongshi Luo, Zhenghao Li, Dongfan Xu, Quan Pan

Southern University of Science and Technology

10-4 **12:05~12:17**

A Time-Based PAM-4 Transceiver Using Single Path Decoder and Fast-Stochastic Calibration Techniques

Dong-Hyun Yoon[1], He Junsen[1], Kwang-Hyun Baek[2], Youngdon Choi[3], Jung-Hwan Choi[3], Tony Tae-Hyoung Kim[1]

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A 80Gb/s/pin Single-Ended PAM-4 Transmitter With an Edge Boosting Auxiliary Driver and a 4-Tap FFE in 28-nm CMOS

Dae-Won Rho[1*], Jae-Koo Park[12*], Seung-Jae Yang[1] and Woo-Young Choi[1]

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The demands for the higher-bandwidth memory access are continuously increasing for many applications such as data centers, HPC, and AI processors. With this, the importance of high-speed memory interfaces is increasing as well and a number of technical approaches are being pursed in order to overcome the channel bandwidth limitation. Especially, the pulse amplitude modulation 4 (PAM-4) technique is actively investigated [1-4]. PAM-4 can reduce the symbol rate by half but at the cost of the reduced signal-to-noise ratio (SNR), resulting in the increased bit error rate (BER)[5]. To minimize the SNR decrease, the level-separation mismatch ratio (RLM) should be optimized. Furthermore, the performance of equalizers should be well optimized for inter-symbol interference (ISI) reduction. This article presents the technique of achieving a 80Gb/s transmitter (TX) with a PAM-4 single-ended voltage mode (VM) driver implemented in 28-nm CMOS technology, which includes a reconfigurable 4-tap feed-forward equalizer (FFE) and an edge-boosting auxiliary driver for channel equalization.

Fig. 1 illustrates the overall TX structure. It receives 10GHz clock from an external source, which goes through the poly phase filter (PPF) and is divided into four-phase clocks ($C4_{I/Q/IB/QB}$). Each of these clocks passes through a duty cycle corrector (DCC) and a quadrature error corrector (QEC), resulting in the quadrature clock with the precise phase difference and duty cycle. Subsequently, these clocks are divided into the octal-rate clocks ($C8_{I/Q/IB/QB}$) and applied to each data path. The data path begins with the generation of PRBS31 data in the pattern generator, which undergo thermometer encoding, resulting in three distinct data signals. Prior to being introduced into the serializers, re-timers are employed to ensure an optimal timing margin. The serialized data then pass through an 8:4 multiplexer (MUX) and a 4:1 MUX, with each output signal directed to five bundles of drivers. Within these bundles, one driver is designed to be tunable with the calibration code, enabling the precise adjustment for the RLM of PAM-4 data and ensuring 50-ohm impedance matching. In the case of the FFE, the data selection from the 8:4 MUX permits the generation of a total of four-tap data, each of which can be directed into a segmented driver. To boost the data output bandwidth, an auxiliary driver having the same structure as the single slice of the bundle driver is implemented. This auxiliary driver accepts data with transition information encoded within, thereby reducing rising and falling times during transitions without distorting the output level.

To generate PAM-4 data, the driver can be configured with MSB and LSB drivers. However, for the structural symmetry, it is common to utilize two instances of the MSB driver and one instance of the LSB driver [1-3]. Moreover, when applying binary-to-thermometer encoding to the MSB and the LSB data, the data toggle, which is the main contributor to power consumption in the VM driver, can be reduced**.** Fig. 2 (a) depicts a conventional low-voltage swing terminated logic (LVSTL) PAM-4 driver, which allows the efficient driver size and the impedance control. However, its critical path stage, operating at the high speed, consists of three stages, leading to poor power-supply-induced jitters (PSIJ). In contrast, Fig. 2 (b) illustrates the driver structure of a single slice used in our design. It employs a 2-stack structure for the impedance control, reducing the critical path to two stages and improving PSIJ. Within the driver's data path, quarter-rate data ($D4_{(PU/PD)\_(A/B/C)}$) are fed into the pull-up and the pull-down drivers in opposite signs. Similarly, the ZQ calibration code is split into pull-up and pull-down codes for each of A, B, C cases, with a resolution of 5 bits each ($ZQ_{(PU/PD)\_(A/B/C)}$[4:0]). By calibrating each thermometer-encoded ZQ code, it becomes possible to achieve both 50-ohm impedance matching and RLM control simultaneously [6].

Fig. 3 illustrates the components for constructing an edge-boosting auxiliary driver, including an encoder, timing examples, and the 4:1 MUX at the front end of the auxiliary driver. The encoder is composed of logic gates, shown in Fig. 3. By sequentially inputting the parallel data of 9 bits (D8[7:0], $D8_{PRE}$[7]) into the logic gates, we can obtain data that carry information about data transitions ($D8_{R/F}$[7:0]). The obtained data are then serialized through the 4:1 MUX. During this process, the pulse width of the 4-phase quadrature clock ($C4_{I/Q/IB/QB}$) can be adjusted using delay cells, allowing the control over the pulse width time (t_{PW}) of $D8_{R/F}$[7:0]. This enables the generation of input data for the edge-boosting auxiliary driver and provides the ability to finely adjust the pulse width, ensuring the precise control over the timing characteristics.

Fig. 4 illustrates the specific architecture of the 8:4 MUX, its timing diagrams, and the table for the relevant output of the data selector. 8 data signals with 1/8 speed of the output signal are generated in parallel. By selecting the appropriate data in the data selector for each case of 4 taps and sampling them at the correct timing, quarter-rate data can be obtained. To enhance the bandwidth, 4 UI pulse generators are used instead of a 3-stacked MUX. Furthermore, by not using a clock selector for timing margin optimization, the loading of the octal rate clock is reduced, which results in power consumption reduction.

Fig. 5 (a) and (b) display the measured eye diagrams of PRBS31 40Gb/s NRZ and PRBS31 80Gb/s PAM-4 single-ended outputs, respectively. The PAM-4 output exhibits a voltage swing of 297mV, with an eye opening of approximately 45mV in the worst case. Fig. 5 (c) illustrates a closed 64Gb/s eye diagram without FFE, passing through a channel with approximately -6.16dB loss at around 16GHz, while Fig. 5 (d) shows the output with equalization achieved with the FFE for the same channel loss. Although the swing is reduced about 15%, the worst eye opening is 37mV, indicating an improved performance. The total power consumption is 246mW, resulting in the energy efficiency of 3.07pJ/bit at 80Gb/s.

In Fig. 6 (a), the measured S21 of the channel is shown. Fig. 6. (b) provides a detailed power break-down. 4:1 MUX and driver consume the largest portion of power (137.5mW), followed by 10GHz clock distribution (43.3mW), 8:4 MUX (33.5mW), and pattern generator with encoder (31.7mW). Fig. 6 (c) presents a comparison table of our measurement results with the published state-of-the-art TXs. Our work achieves the highest data rate among all single-ended TXs.

Acknowledgments

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References:

[1] Z. Toprak-Deniz *et al*., "A 128-Gb/s 1.3-pJ/b PAM-4 Transmitter With Reconfigurable 3-Tap FFE in 14-nm CMOS," *IEEE JSSC,* vol. 55, no. 1, pp. 19-26, Jan. 2020.

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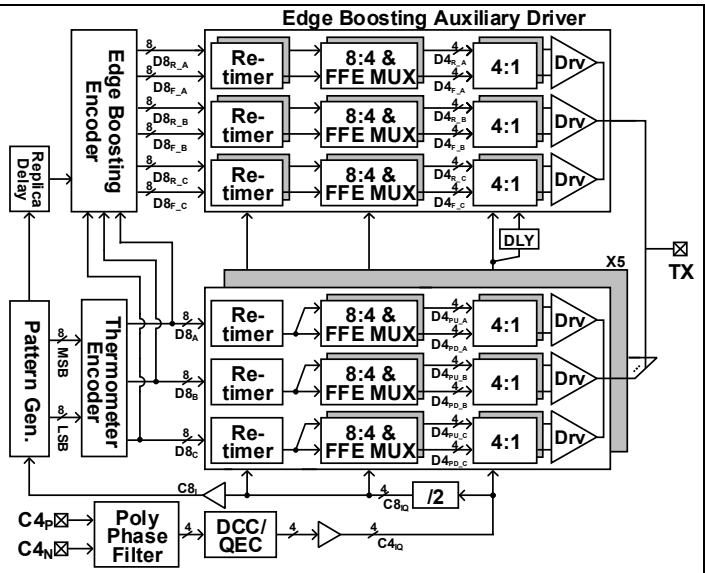


Fig. 1. Top block diagram of transmitter.

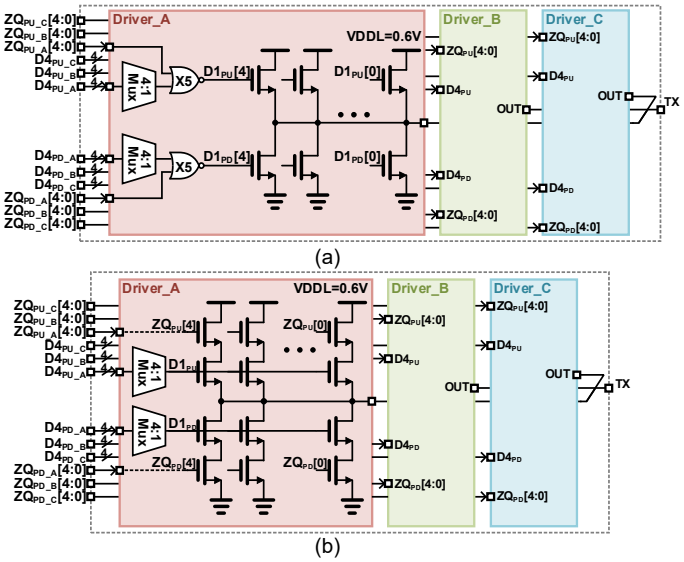


Fig. 2. (a) Structure of the conventional LVSTL driver, (b) proposed design.

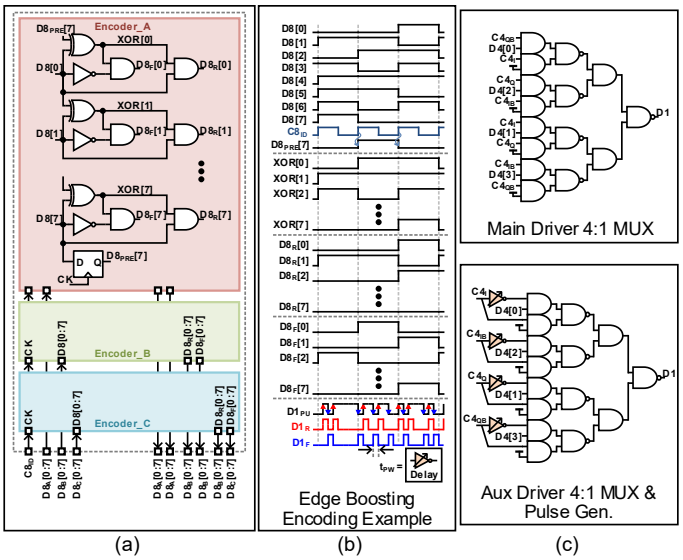
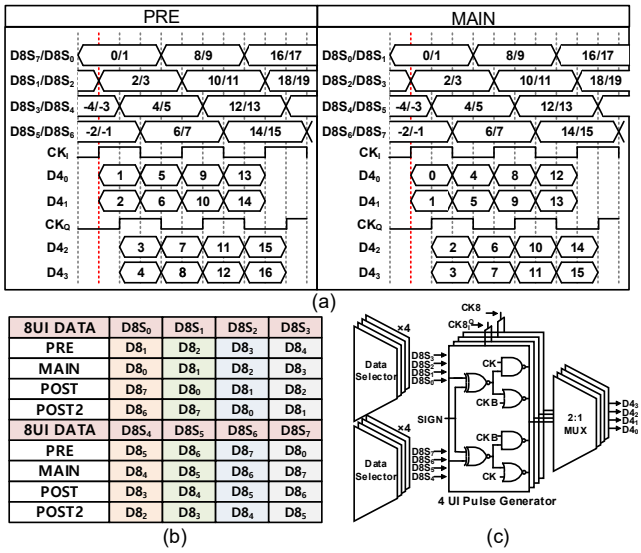


Fig. 3. (a) Implementations for the edge boost encoder, (b) Timing diagram, and (c) 4:1 MUX with pulse generator.



8UI DATA	$D8S_0$	$D8S_1$	$D8S_2$	$D8S_3$
PRE	$D8_1$	$D8_2$	$D8_3$	$D8_4$
MAIN	$D8_0$	$D8_1$	$D8_2$	$D8_3$
POST	$D8_7$	$D8_0$	$D8_1$	$D8_2$
POST2	$D8_6$	$D8_7$	$D8_0$	$D8_1$
8UI DATA	$D8S_4$	$D8S_5$	$D8S_6$	$D8S_7$
PRE	$D8_5$	$D8_6$	$D8_7$	$D8_0$
MAIN	$D8_4$	$D8_5$	$D8_6$	$D8_7$
POST	$D8_3$	$D8_4$	$D8_5$	$D8_6$
POST2	$D8_2$	$D8_3$	$D8_4$	$D8_5$

Fig. 4. (a) Comparison of timing diagrams for pre and main tap, (b) Data selection table based on tap types, and (c) Architecture of 8:4 MUX.

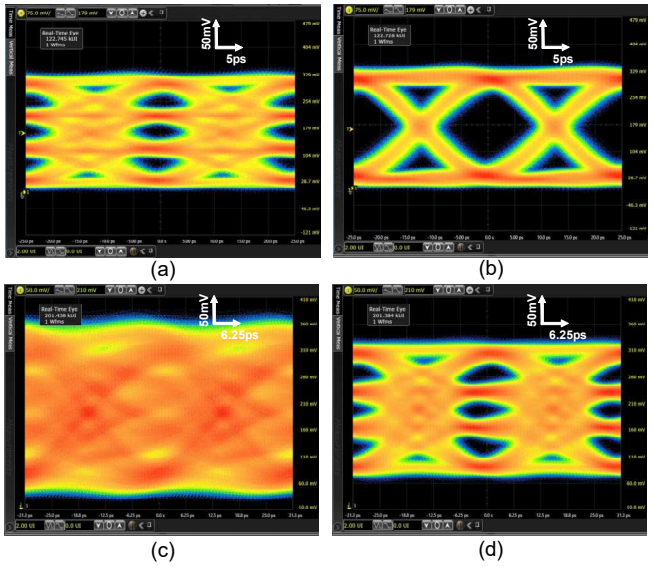
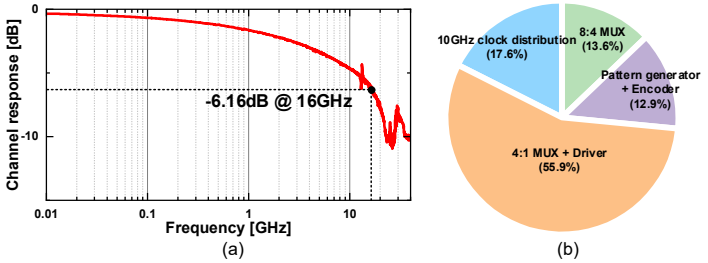


Fig. 5. (a) Measured 80Gb/s PAM-4 eye diagram, (b) 40Gb/s NRZ, (c) 64Gb/s eye without FFE, with -6.16dB loss channel, (d) 64Gb/s eye with FFE, with -6.16dB loss channel.



	[1] JSSC'20	[2] JSSC'21	[3] JSSC' 22	[6] JSSC'21	[7] ISSCC' 23	This work
Technology	14nm FinFET	40nm CMOS	10nm FinFET	65nm CMOS	40nm CMOS	28nm CMOS
Supply(V)	1.2	1.0/1.2	0.85/1.0/1.5	1.0/0.6	1.0/0.6	1.0/0.6
Data rate per pin (Gb/s/pin)	64	56	112	28	32	80
Signaling	Differential PAM-4	Differential PAM-4	Differential PAM-4	Single-ended PAM-4	Single-ended NRZ	Single-ended PAM-4
Driver type	CML (tailless)	VM (SST)	CML	VM (LVSTL)	VM (PN-over-NP)	VM (LVSTL)
Equalization	3-tap	4-tap	8-tap	2-tap assymetric	2-tap edge boosting	4-tap reconfigurable + edge boosting
Clock source	External	On-chip PLL	On-chip PLL	External	External	External
Output swing(V)	1.0	1.0	1.0	0.3	0.3	0.3
Energy efficiency (pJ/bit)	1.3	3.89	1.88	0.64	0.51*	3.1
TX Area(mm²)	0.048	0.56	0.088	0.03	0.005*	0.045

*with external input data

(c)

Fig. 6. (a) S21 of -6.16dB loss channel, (b) Precise power break

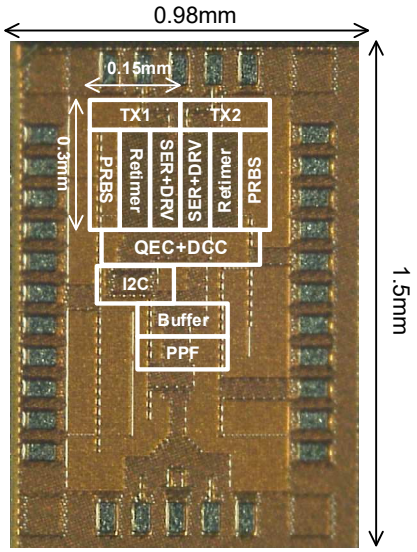


Fig. 7. Die micrograph of the TX fabricated in 28nm CMOS technology

A 80Gb/s/pin SinIge-Ended PAM-4 Transmitter With an Edge Boosting Auxiliary Driver and a 4-Tap FFE in 28-nm CMOS

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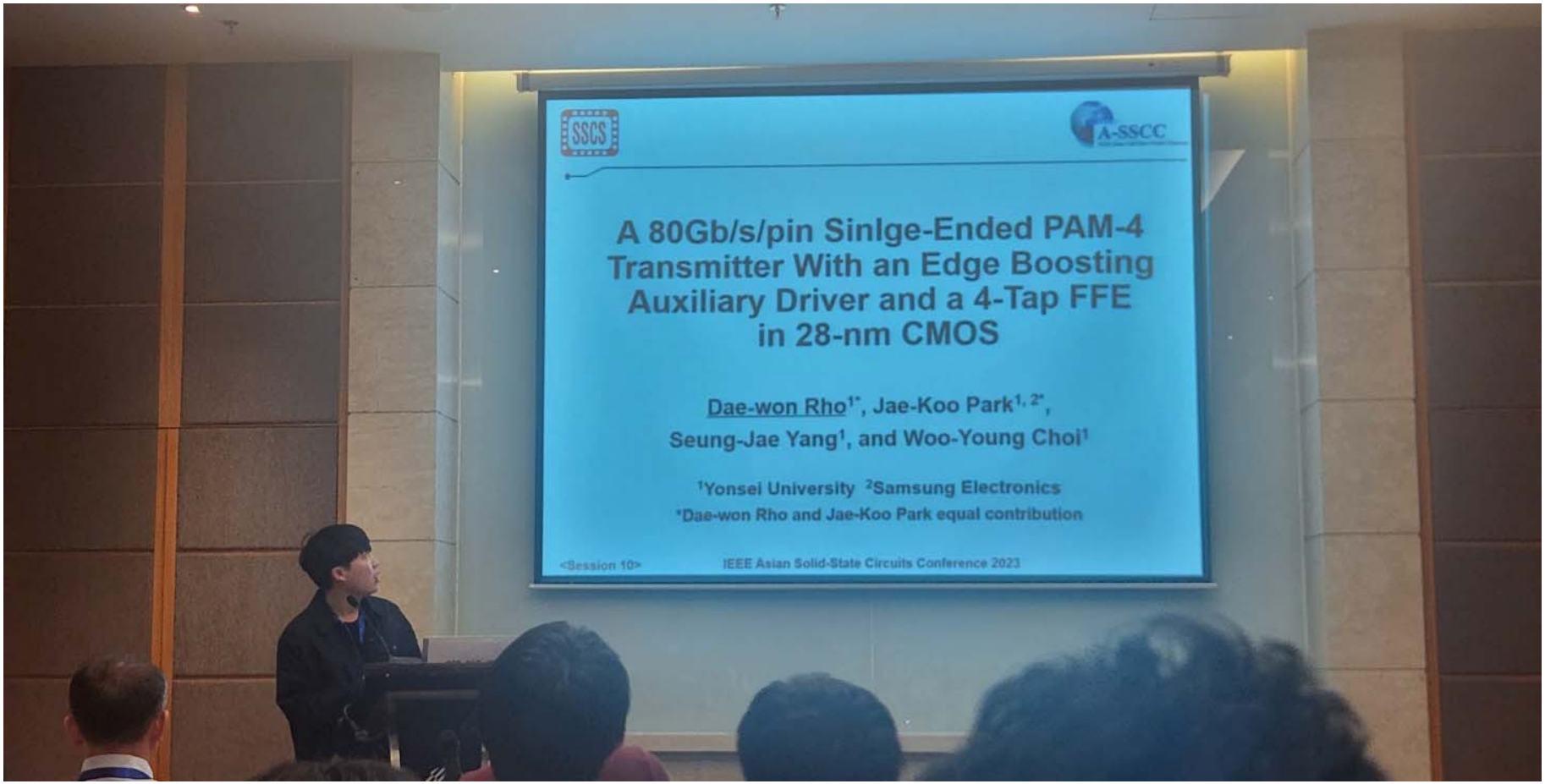
*Dae-won Rho and Jae-Koo Park equal contribution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<Session 10>
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