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Room 6F	Room 7	Room 8	Room 9
Plenary Session Coffee Break, *Upper Level, Ballroom 20 Lobby*			
Plenary Session, *Ballroom 20BCD*			
Unopposed Exhibit-only Time, *Exhibit Hall (coffee service 10:00–10:30)*			
Exhibition and Show Floor, *Exhibit Hall (concessions available)* **OFC Career Zone Live,** *Exhibit Hall B2*			
OFC and Co-Sponsors Awards and Honors Ceremony and Luncheon *Upper Level, Ballroom 20A*			
T3H • Silicon Photonics Applications	**T3I • Short-reach Systems II**	**T3J • Orchestration and Control**	**T3K • Intra Data Center Networks I**
Coffee Break, *Exhibit Hall*			
T4H • Quantum Dots and Novel III-V Devices	**T4I • Long-haul Systems and Non-linear Mitigation**	**T4J • Multi-core Fibers**	
Exhibitor Happy Hour, *Center Terrace*			
Celebrating 50 Years of Light-speed Connections, Keynote Presentation, *Ballroom 20BCD*			
Celebrating 50 Years of Light-speed Connections, Conference Reception, *Sails Pavilion*			
Rump Session: When Will Co-packaged Optics Replace Pluggable Modules in the Datacenter? *Room 6F*			

Exhibit Hall Theater I	Exhibit Hall Theater II	Exhibit Hall Theater III
Exhibit Hall Opens 10:00		
■ **MW Panel I: State of the Industry** 10:30–12:00 ■ **MW Panel II: 5G and Re–thinking Access Networks** 12:30–14:00 ■ **MW Panel III: Optical Interconnect and Computing for Scaling Machine Learning (ML) Systems** 14:30–16:00 **OIDA Roadmap on Quantum Photonics** 16:15–17:00	**Ethernet Interoperability and Deployments – New and Legacy Solutions Work Together** *Ethernet Alliance* 10:15–11:15 ■ **Data Center Summit: Keynote and Panel** *Session sponsored by InnoLight* 11:30–13:45 **Preparing the Transport Network for 5G** *Session sponsored by Juniper Networks* 13:50–14:50 **Embedded Optics and How They Should Be Done to Support the OEM Eco–system – Panel Debate** 15:00–17:00	**Product Showcase -** *Huawei Technologies Canada Co., Ltd.* 10:15–10:45 **AIM Photonics Member Successes and Updates** *AIM Photonics* 11:00–12:00 **5G Architectures and Service Considerations** 12:15–13:15 **400ZR Specification Update** *OIF* 13:30–14:30 **Standards Update on 5G Transport (and more)** *ITU-T SG15* 14:45–15:45 **Accelerating ROI on the Road to SDN** *SDN* 16:00–17:00
Exhibit Hall Closes 17:00		

Room 6E	Room 6F	Room 7	Room 8	Room 9
T3G • Panel: As we Approach Shannon Limit, How do we Precisely Assess the Performance of Coherent Transponders for Field Deployment?—Continued	**T3H • Silicon Photonics Applications—Continued**	**T3I • Short-reach Systems II—Continued**	**T3J • Orchestration and Control—Continued**	**T3K • Intra Data Center Networks I—Continued**
	T3H.7 • 15:45  **A Fully Integrated 25 Gb/s Si Ring Modulator Transmitter with a Temperature Controller,** Minkyu Kim[1], Min-Hyeong Kim[1], Youngkwan Jo[1], Hyun-Kyu Kim[1], Stefan Lischke[2], Christian Mai[2], Lars Zimmermann[2,3], Woo-Young Choi[1]; *[1]Department of Electrical and Electronics Engineering, Yonsei Univ., Korea (the Republic of); [2]IHP, Germany; [3]Technische Universitaet Berlin, Germany.* We realized a fully integrated 25Gb/s Si ring modulator transmitter containing a temperature controller that guarantees the optimal ring modulator temperature against any temperature perturbation. The transmitter is implemented with a 0.25-μm photonic BiCMOS technology.		**T3J.6 • 15:45** **Intent Defined Optical Network: Toward Artificial Intelligence-based Optical Network Automation,** Kaixuan Zhan[1], Hui Yang[1], Qiuyan Yao[1], Xudong Zhao[1], Ao Yu[1], Jie Zhang[1], Young Lee[2]; *[1]State Key Laboratory of Information Photonics and Optical Communications, Beijing Univ. of Posts and Telecommunications, China; [2]Huawei Technologies Co., Ltd, China.* Toward AI-based optical network automated operation, we propose an intent defined optical network (IDON) architecture with self-adapted generation and optimization (SAGO) policy. The feasibility and efficiency are verified on the enhanced SDN testbed.	**T3K.7 • 15:45** **Scaling HPC Networks with Co-packaged Optics,** Pavlos Maniotis[1], Laurent Schares[1], Benjamin Lee[1], Marc Taubenblatt[1], Daniel Kuchta[1]; *[1]IBM TJ Watson Research Center, USA.* We propose an HPC network architecture with co-packaged optics enabling 128-port 51.2-Tb/s switches. Simulations for a >34,000-accelerator system show up to 11.2x throughput improvement over the Summit supercomputer, opening the way to direct-network-attached GPUs.

16:00–16:30 Coffee Break, *Upper Level Corridors and Exhibit Hall*

Show Floor Programming Continued

■ **MW Panel III: Optical Interconnect and Computing for Scaling Machine Learning (ML) Systems**
14:30–16:00, *Theater I*

Standards Update on 5G Transport (and more)
ITU-T SG15
14:45–15:45, *Theater III*

Embedded Optics and How They Should Be Done to Support the OEM Eco–system – Panel Debate
15:00–17:00, *Theater II*

Accelerating ROI on the Road to SDN
SDN
16:00–17:00, *Theater III*

OIDA Roadmap on Quantum Photonics
16:15–17:00, *Theater I*

A Fully Integrated 25 Gb/s Si Ring Modulator Transmitter with a Temperature Controller

Minkyu Kim[1], Min-Hyeong Kim[1], Youngkwan Jo[1], Hyun-Kyu Kim[1], Stefan Lischke[2], Christian Mai[2], Lars Zimmermann[2,3], and Woo-Young Choi[1]
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Abstract: We realized a fully integrated 25Gb/s Si ring modulator transmitter containing a temperature controller that guarantees the optimal ring modulator temperature against any temperature perturbation. The transmitter is implemented with a 0.25-μm photonic BiCMOS technology. © 2020 The Author(s)

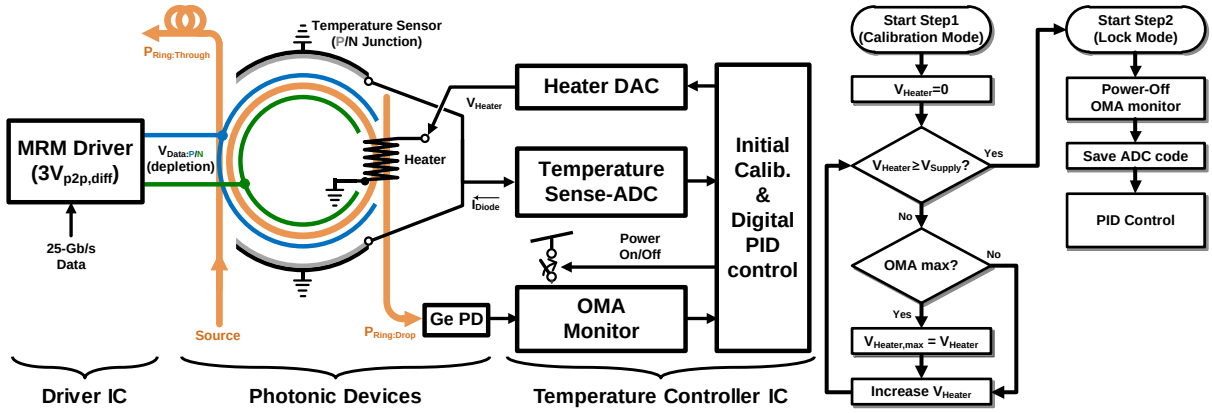
1. Introduction

Silicon photonic transmitters based on Si ring modulators (RMs) are very attractive for numerous optical interconnect applications as they provide high-bandwidth and energy-efficient operation with much smaller footprints compared to Si Mach-Zehnder modulators. Recently, 112 Gb/s RM has been reported for 400G data center applications [1]. Furthermore, next-generation photonic switch systems are expected to rely on ring filters with their WDM-compatibility and small sizes. However, due to their resonance characteristics, ring modulators and filters suffer from severe thermal sensitivity and process variation problems. Consequently, the use of on-chip heaters and temperature control circuits [2–6], which provide temperature required for the optimal device performance, is essential for any practical application of ring modulators and filters. In [2,3], the average power of the modulated RM signal is controlled with the closed-loop feedback, but the target average power has to be set externally. In [4], the optical modulation amplitude (OMA) is directly monitored by high-speed sampling of designated modulation pattern with slope quantization. But high-speed sampling consumes a large amount of power when the data rate is high. OMA maximization based on bit-statistics based on the training data sequence can achieve low-power operation with precise control [5]. But in this implementation, maintaining the optimal condition when temperature and/or optical input power changes from the initial calibration can be a problem. In order to alleviate these problems, we have previously reported a custom-designed temperature control IC with which the optimal OMA condition is determined in the calibration mode and is maintained in the locking mode with the digital 1-bit dithering technique [6]. But this IC is not monolithically integrated with the RM and consumes a fair amount of power due to its OMA monitoring block.

In this paper, we present a fully integrated RM transmitter containing a new type of temperature controller with reduced power consumption. The new temperature control IC uses the power-hungry OMA monitor block only in the initial calibration mode. With an on-chip temperature sensor, the temperature control remembers the temperature for the optimal OMA and maintains the RM at this temperature with on-chip digital PID controller and heater. To the best of our knowledge, this is the first report of the fully integrated 25 Gb/s silicon photonic transmitter with a temperature controller in the C-band.

2. Ring Modulator Temperature Controller

Figure1(a) shows the block diagram of our custom-designed silicon photonic transmitter IC. It consists of three parts: modulator driver, photonics devices (Si RM and monitor Ge PD), and temperature controller. The driver amplifies $600mV_{pp,diff}$ input NRZ data to deliver $3V_{pp,diff}$ to the depletion-type RM. The driver performance is optimized by co-simulation with the large-signal SPICE model for the RM [7,8] in the design stage. The radius of RM is 12μm and its waveguide width is 500nm. It contains a drop port, to which a monitor Ge PD is connected. An N-doped heater is placed within the ring waveguide, which can provide the tuning range of about 40% of the FSR. To sense the RM temperature, a PN-junction-based temperature sensor is placed outside the RM. The temperature controller has 4 blocks: OMA monitor, heater DAC, temperature-sensing ADC, and synthesized digital block which performs calibration and maintains the optimal condition. The OMA monitor block has trans-impedance amplifier (TIA) with 48dBΩ gain and 20GHz bandwidth, high-pass filter, power detector, track-and-hold (T/H) circuit, and comparator [6]. The digital synthesized block controls the heater DAC and turns on the OMA monitor only when needed so that power can be saved.



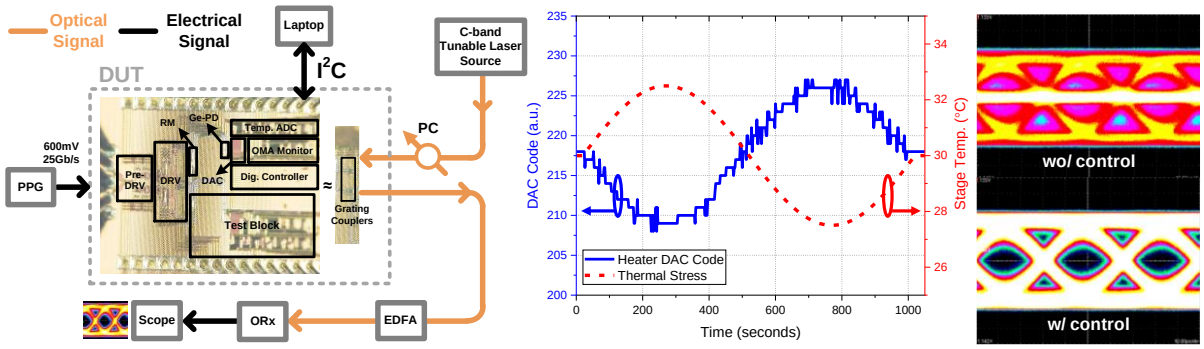
(a) (b)

Fig. 1. (a) Block diagram of the monolithic silicon photonic transmitter with temperature controller and (b) flow-chart of the control algorithm

Figure1(b) shows the RM temperature control scheme in a flow chart. It has two modes. In the calibration mode, the heater voltage is swept, the heater voltage producing the maximum OMA is determined, and that heater voltage is saved as a digital code for the DAC. In the locking mode, the OMA block is turned-off to reduce power consumption, and the temperature ADC code is saved as a reference with which the optimal temperature is maintained by the digital PID control. In this way, the RM can maintain its optimal operation against any temperature perturbation.

3. Measurement Results

Figure2(a) shows the photo of our electronic-photonic integrated circuit transmitter, realized with IHP's 0.25-μm photonic BiCMOS technology [9], and the measurement setup. Input light is coupled into the chip through a grating coupler, and the modulated output light is coupled out with another grating coupler. The driver amplifies 600-$mV_{pp,diff}$ input 25Gb/s PRBS 2^{31}-1 NRZ data and delivers them to the RM. The modulated output optical signal is amplified with an EDFA, and the commercial optical receiver converts the optical signal to electrical signal for the eye measurement. I^2C bus is used for externally controlling and monitoring the digital block during the measurement. The temperature sensor and OMA monitor block consumes 2.6-mW and 1.5-mW, respectively, but the OMA monitor block is turned-off after the calibration mode. The synthesized digital block consumes 0.725-mW.



(a) (b) (c)

Fig. 2. (a) Measurement setup, (b)thermal stress measurement and (c) 25 Gb/s eye-diagram with thermal stress

Figures 2(b) and 2(c) show the results of the thermal stress test in which the chip-stage temperature is intentionally changed with a 5°C sine-wave having period of 1000 seconds as shown in red dotted line in Fig. 2(b). With temperature controller OFF, the eye closes completely as shown in the top of Fig. 2(c). With temperature controller ON, the controller produces DAC codes in response to the chip temperature change as shown with a blue line in Fig. 2(b). As expected, the heater voltage changes in the opposite direction to the chip temperature change so that the desired RM temperature can be always maintained. The bottom figure in Fig. 2(c)

shows the accumulated eye maintaining near 5.2dB extinction ration (ER) for 16 minutes while the chip temperature changes.

Table I compares the performances of recently reported RM temperature control ICs. As can be seen in the table, only [5] and our works determine the optimum condition without any external reference setting and are fully integrated. Although the power consumption reported in [5] is much smaller than our result, it is due to the much advanced SOI CMOS technology used in [5] not in the temperature control algorithm employed. In addition, the performance of our temperature control scheme should not depend on the data rate as is the case for [4]. We believe our approach based on photonic BiCMOS technology should find wide applications for high-performance transceivers based on RMs and next-generation photonic switch systems based on WDM ring filters.

Table I. Performance Comparison

	[2] 16' JSSC	[3] 18' ISSCC	[4] 16' JSSC	[5] 16' JSSC	[6] 19' JLT	This Work
Process	130nm SOI SiPh + 65nm CMOS	100nm SOI SiPh + 65nm CMOS	130nm SOI SiPh + 40nm CMOS	45nm CMOS SOI	0.25μm BiCMOS	0.25μm Photonic BiCMOS
Wavelength	1550nm	1310nm	1550nm	1180nm	1550nm	1550nm
Demo. data-rate	25 Gb/s	10 Gb/s	2 Gb/s	5 Gb/s	25 Gb/s	25Gb/s
Driver Integration	O (Wire-bonded)	O (3D face-to-face)	O (Wire-bonded)	O (Monolithic)	X	O (Monolithic)
Controller Integration	X (Off-chip PD)	O (3D face-to-face)	X (Off-chip DAC)	O (Monolithic)	X (Off-chip PD)	O (Monolithic)
Control Scheme	Average Power	Analog closed-loop w/ digital reconfig.	OMA monitor w/ slope quantization	Bit-statistics	OMA monitor w/ power detector & 1-bit dithering	OMA monitor w/ Temp. sensing & PID control
Manual Reference Setting	O	O	X	X	X	X
Resonance wavelength tuning range	N/A	N/A	5 nm	2.5 nm	0.55 nm	3.27 nm
Controller Power (Except heater)	0.17mW	0.15mW	2.9mW	0.72mW	3.91mW	3.325mW

4. Acknowledgement

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5. References

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