ISOCC 2020
17th International SoC Design Conference

October 21-24, 2020
Sono Calm Yeosu Hotel, Yeosu, Korea

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** COVID-19 Update

The organizing committee is closely monitoring the situation associated with the ongoing COVID-19 pandemic. For the safety and health of all conference participants, **ISOCC 2020 will be held as a hybrid conference offering the on-site and virtual versions, October 21-24.** Further details will be posted on the website as they become available. We appreciate your commitment and interest.

Time Table

WEDNESDAY_ OCTOBER 21, 2020						
From	Till	Lobby	LOBBY 1F	GRAND BALLROOM2 1F	SAPPHIRE1 2F	SAPPHIRE2 2F	SAPPHIRE3 2F
12:00	13:00	On-site Registration					
13:00	14:30			Tutorial 1			
14:30	16:00			Tutorial 2			
16:00	17:30			Tutorial 3			
17:30	18:00		Break Time (30min.)				
18:00	20:00	Welcome Reception (Grand Ballroom 1)					

THURSDAY_ OCTOBER 22, 2020												
From	Till	Lobby	LOBBY 1F	GRAND BALLROOM2 1F		SAPPHIRE1 2F		SAPPHIRE2 2F		SAPPHIRE3 2F	
08:30	08:40	On-site Registration	Chip Design Contest (CDC) Poster 1			CDC Oral					
08:40	08:50										
08:50	09:00										
09:00	09:10										
09:10	09:20										
09:20	09:30		Break Time (10min.)								
09:30	09:45		Opening Ceremony (Grand Ballroom1)								
09:45	10:25		Keynote Speech-1 (Grand Ballroom1)								
10:25	11:05		Keynote Speech-2 (Grand Ballroom1)								
11:05	11:20		Break Time (15min.)								
11:20	12:00			Keynote Speech-3 (Grand Ballroom1)							
12:00	13:15			Lunch, WiCAS (5F Lily 1)							
13:15	13:30		Chip Design Contest (CDC) Poster 2	DC	16	DCAS1	216	ML1	236	SS1	1
13:30	13:45				181		134		186		3
13:45	14:00				86		220		200		6
14:00	14:15				99		97		218		12
14:15	14:30				101		111		52		112
14:30	14:45			Break Time (15min.)							
14:45	15:00			RF1	51	WLN	137	SoC1	8	SS3	23
15:00	15:15				74		163		9		66
15:15	15:30				184		162		109		67
15:30	15:45				193		211		168		68
15:45	16:00				203		223		195		227
16:00	16:15		Chip Design Contest (CDC) Poster Exhibition								
16:15	16:30										
16:30	16:45					ET1	88	ML2	183	SS2	15
16:45	17:00						47		81		19
17:00	17:15						188		92		27
17:15	17:30						78		225		30
17:30	17:45						230		91		45
17:45	18:00	Break Time (15min.)									
18:00	20:00	Banquet									

WLN Wireline

Chair: Dong-Woo Jee (Ajou University, Korea)

14:45~16:00, THURSDAY_OCTOBER 22, 2020

Sapphire 1 (2F)

WLN 1 (137)
14:45-15:00

A 8.4Gb/s Low Power Transmitter with 1.66 pJ/b using 40:1 Serializer for DisplayPort Interface

Woosong Jung, Jinhyung Lee, Kwangho Lee, Hyojun Kim, and Deog-Kyoon Jeong

Seoul National University, Korea

WLN 2 (163)
15:00-15:15

Optical Receiver Front-end for Active Optical Cable in 180 nm CMOS

Daehyun Koh[1], Deog-Kyoon Jeong[1], Dainel Jeong[2], and Jeongho Hwang[3]

[1]Seoul National University, Korea
[2]Ayar Labs Incorporation, USA
[3]Cadence Design Systems Incorporation, USA

WLN 3 (162)
15:15-15:30

A Fast Locking Duty Cycle Corrector with High Accuracy

Eun-Young Jung and Won-Young Lee

Seoul National University of Science and Technology, Korea

WLN 3 (211)
15:30-15:45

5 Gb/s Optical Transceiver for MEMS Tunable HCG-VCSEL in 65 nm CMOS

Sean Kane Lloyd M. Quintans, Francesca Bea V. Narcida, Janelle Eira A. Tordesillas, Maria Patricia Rouelli G. Sabino, Anastacia B. Alvarez, Maria Theresa G. de Leon, John Richard E. Hizon, Christopher G. Santos, and Marc D. Rosales

University of the Philippines, Philippines

WLN 3 (223)
15:45-16:00

Performance Optimization of Silicon Photonic Ring Switch with CMOS Driver

Daewon Rho, Minkyu Kim, Hyun-Kyu Kim, and Woo-Young Choi

Yonsei University, Korea

Performance Optimization of Silicon Photonic Ring Switch with CMOS Driver

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***Abstract*— Crosstalk and insertion loss of a Si photonic 2 x 2 ring switch are optimized and a CMOS circuit that can control this ring switch is designed.**

Keywords*— optical switch; ring resonator; insertion loss; crosstalk; co-simulation; CMOS; driver; optimization;

I. INTRODUCTION

With the rapid development of AI technology and various cloud services, data centers are becoming more and more important both technologically and socially. A great amount of research and development efforts are being made in order to realize higher-performance data centers with more less energy efficiency. One key aspect for improving data center performance is the interconnect technology. As the requirements for data throughput, interconnect distances, and switching complexity continuously increase, the electrical interconnect technology is reaching its limit and optical solutions are finding their applications in data centers. Faster and longer interconnects based on optical fiber are routinely used in present-day data centers and, with this, there is a growing need for optical switching solutions that can provide higher throughput than what is available with electrical switches [1-4].

Figure 1(a) schematically shows an N x N optical switch. For its implementation, efficient 2 x 2 optical switch units are needed along with a controller IC which controls the operation of each switch unit. For the goal of realizing an efficient N x N optical switch as well as its controller, we realize a 2 x 2 optical switch based on Si photonic ring resonator and design a CMOS circuit which optimally drives the optical switch

II. 2 x 2 RING–RESONATOR SWITCH

We are interested in a 2 x 2 optical switch based on Si photonic ring resonator, as it has a small size and can be realized with CMOS fabrication technology. Figure 1(b) shows a typical ring-resonator 2 x 2 switch along with its Bar and Cross operations. The optical spectra for Bar and Cross operations are shown in Figure 2. In order to obtain the

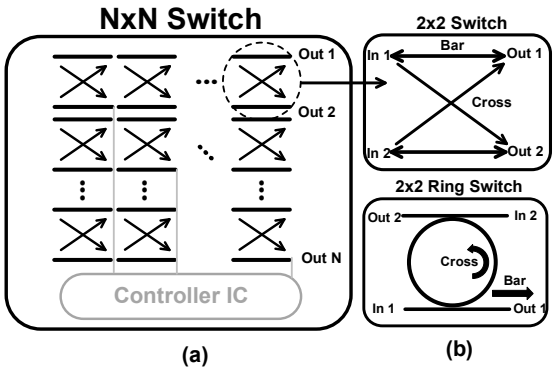

Figure 1. (a) NxN switch schematic, (b) unit 2x2 Switch and implementing it as a ring resonator

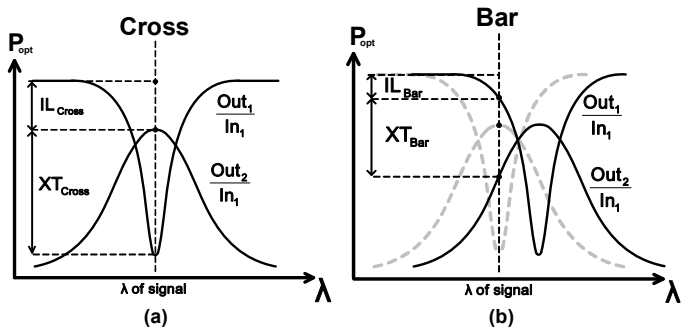

Figure 2. (a) Characteristic curve of Cross, (b)Bar

maximum extinction ratio for Cross, the input wavelength should be at the resonance wavelength of the ring resonator, which should satisfy $m\lambda_{res} = n_e L$, where m is an integer, λ_{res} is the resonance wavelength, n_e is the effective refractive index, and L is the circumference of the ring. Since n_e depends on temperature, the Bar or Cross state of the ring resonator 2 x 2 switch can be controlled by an on-chip heater, which shifts λ_{res}. Figure 2 graphically explains Insertion Loss (IL) and Crosstalk (XT), the two key parameters for 2 x 2 optical switch operation. As can be seen in the figure, the amounts for IL and XT change as the resonance wavelength shifts.

Figure 3(a) is a photo of 2 x 2 ring-resonator switch chip manufactured with IHP's Si Photonic Integrated Circuit technology. Input optical signal is introduced through a grating coupler. Figure 3(b) shows the transmission and the reflection spectra at various temperatures controlled by the on-chip heater. As can be seen in the figure, the resonance wavelength shifts linearly according to the input electrical power delivered to the heater. Figure 4(a) shows the product of insertion loss and crosstalk per power at various heater powers. Since smaller insertion loss and the larger the absolute value of the crosstalk are desired, we decide the 'insertion loss x power' and the 'crosstalk / power' as performance parameters. Insertion loss and the crosstalk values used in the figure are based from the measurement results. As power increases, 'Insertion loss x power' tends to increase and 'XT / power' has a parabolic shape with a minimum. Therefore, the first point at which the two graphs intersect can be determined as the optimal point. The heater power at this point is about 2.96mW, corresponding to about 1.5V with the used on-chip heater. As shown in Figure 5(b), the heater resistance under this condition is about 0.38kΩ. Finally, the 3-dB bandwidth of the ring resonator is about 25GHz, sufficient for transmitting the target 25Gbps NRZ optical data.

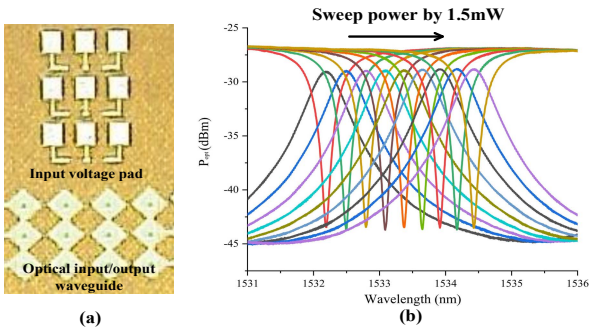

Figure 3. (a) Chip Photo, (b) measurement result in order to sweep voltage

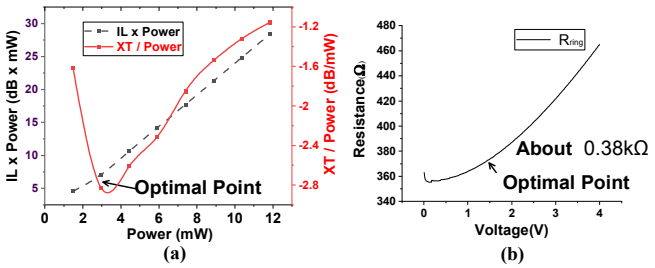

Figure 4. (a) IL, XT according to input power, (b) resistance result

III. DRIVER AND THE OVERALL PERFROMANCE

Based on above determined switch characteristics, the behavioiral model of the ring-resonator 2 x 2 switch is implemented in Verilog-A, and a switch driving circuit is designed. Figure 5(a) shows the overall block diagram for co-simulation, and Figure 5(b) schematically shows the driving circuit designed in 28nm CMOS technology. Figure 6(a) shows the transient simulation results. When 'Vctrl' is 'high' or 'low', the input optical signal goes through channel 1 or channel 2, respectively. Figure 6(b) is the eye-diagram of the transmitted data. The driver consumes about 2.9mW.

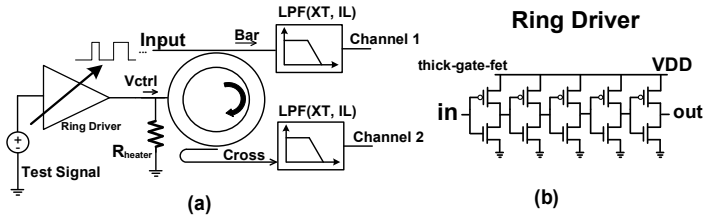

Figure 5. (a) Overall Block Diagram of 2x2 Ring Switch, (b) Schematic of Driver

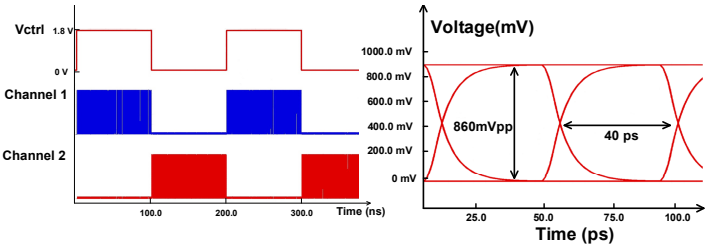

Figure 6. (a) Transient results of simulation, (b) eye diagram at 25Gbps

ACKNOWLEDGMENT

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