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Optical Interconnects Conference 2019 Program-at-a-Glance

<table>
<tr><th>WEDNESDAY,
24 APRIL</th><th>THURSDAY,
25 APRIL</th><th>FRIDAY,
26 APRIL</th></tr>
<tr><td colspan="3">8:00 am-8:30 am
Breakfast/Coffee Break – Canyon Ballroom</td></tr>
<tr><td>8:30 am-9:00 am
WA: Opening Remarks
Session Chair: C. Sun</td><td>8:30 am-9:15 am
ThA: Novel Developments/Experiments I
Session Chair: L. Gantz</td><td rowspan="2">8:30 am-9:45 am
FA: Topology Optimization Studies & Simulations I
Session Chair: R. McCormick</td></tr>
<tr><td>9:00 am-9:45 am
WB: RF/High-Speed Testing I
Session Chair: J. Bovington</td><td>9:15 am-9:45 am
ThB: Novel Developments/Experiments II
Session Chair: TBD</td></tr>
<tr><td colspan="3">9:45 am – 10:15 am
Coffee Break/Exhibits – Canyon Ballroom</td></tr>
<tr><td>10:15 am-12:00 pm
WC: RF/High-Speed Testing II
Session Chair: P. Sun</td><td>10:15 am-12:00 pm
ThC: Novel Developments/Experiments III
Session Chair: TBD</td><td>10:15 am-12:00 pm
FB: Topology Optimization Studies & Simulations II
Session Chair: A. Seyedi</td></tr>
<tr><td colspan="2">12:00 pm-1:30 pm
Lunch Break (ON OWN)</td><td rowspan="4">Registration- Canyon Ballroom Foyer
Wednesday, 24 April- 7:30 am-6:00 pm
Thursday, 25 April- 7:30 am-6:00 pm
Friday, 26 April- 8:00 am-12:00 pm</td></tr>
<tr><td>1:30 pm-3:00 pm
WD: RF/High-Speed Testing III
Session Chair: D. Kutcha</td><td>1:30 pm-3:00 pm
ThD: Hyperscale DC Requirements
Session Chair: J. Stewart</td></tr>
<tr><td colspan="2">3:00 pm-3:30 pm
Coffee Break/Exhibits – Canyon Ballroom</td></tr>
<tr><td>3:30 pm-5:30 pm
WE: Workshop on 5G
Session Chair: S. Lessard</td><td>3:30 pm-5:30 pm
ThE: Workshop on Co-packaged Optics
Session Chair: K. Schmidtke</td></tr>
<tr><td>5:30 pm-6:30 pm
Welcome Reception
Canyon Ballroom</td><td colspan="2">All sessions are in the Mesa Ballroom</td></tr>
</table>

04-24-2019

08:00 - 08:30 **Breakfast/Coffee Break** **Canyon Ballroom**

WA

08:30 - 09:00 **Opening Remarks** **Mesa Ballroom**

Moderation: C. Sun, CA/US

WB

09:00 - 09:45 **RF/High-Speed Testing I** **Mesa Ballroom**

Moderation: J. Bovington, CA/US

09:00 - 09:45 **WB1 - Advancements and Challenges for Electrical Interfaces from 56 Gbps to 112 Gbps and Beyond**

M.P. Li, CA/US

09:45 - 10:15 **Coffee Break/Exhibits** **Canyon Ballroom**

WC

10:15 - 12:00 **RF/High-Speed Testing II** **Mesa Ballroom**

Moderation: P. Sun, CA/US

10:15 - 10:45 **WC1 - ULTRA-HIGH-SPEED OPTICAL TRANSMITTERS USING DIGITAL-PREPROCESSED ANALOG-MULTIPLEXED DAC**

H. Yamazaki[1], M. Nagatani[1], H. Wakita[1], Y. Ogiso[1], S. Kanazawa[1], M. Nakamura[1], F. Hamaoka[2], M. Ida[1], T. Hashimoto[1], H. Nosaka[1], Y. Miyamoto[1]; [1]Atsugi, JP, [2]Yokosuka, JP

10:45 - 11:00 **WC2 - A 112 GB/S PAM4 CMOS OPTICAL RECEIVER WITH SUB-PJ/BIT ENERGY EFFICIENCY**

G. Balamurugan[1], H. Li[1], M. Sakib[2], O. Dosunmu[2], A. Liu[2], H. Rong[2], J. Jaussi[1], B. Casper[1]; [1]Hillsboro, OR/US, [2]Santa Clara, CA/US

11:00 - 11:15 **WC3 - LOW-VOLTAGE 60GB/S NRZ AND 100GB/S PAM4 O-BAND SILICON RING MODULATOR**

Y. Ban[1], J. Verbist[2], M. Vanhoecke[2], J. Bauwelinck[2], P. Verheyen[1], S. Lardenois[1], M. Pantouvaki[1], J. Van Campenhout[1]; [1]Heverlee, BE, [2]Ghent, BE

11:15 - 11:30 **WC4 - A 50GBIT/S NET ERROR-FREE NRZ 850NM VCSEL BASED OPTICAL INTERCONNECT**

L. Chorchos[1], N. Ledentsov Jr.[2], M. Agustin[2], J. Kropp[2], V.A. Shchukin[2], V..P. Kalosha[2], J..P. Turkiewicz[1], N..N. Ledentsov[2]; [1]Warsaw, PL, [2]Berlin, DE

11:30 - 11:45 **WC5 - A 4X25-GBPS MONOLITHICALLY INTEGRATED SI PHOTONIC WDM TRANSMITTER WITH RING MODULATORS**

M. Kim[1], K. Park[2], W. Oh[2], C. Mai[3], S. Lischke[3], L. Zimmermann[3], W. Choi[1]; [1]Seoul, KR, [2]KR, [3]DE

11:45 - 12:00 **WC6 - NON-LINEAR SYSTEM IDENTIFICATION SCHEME FOR THE DESIGN OF EFFICIENT COMPENSATORS AND CALIBRATIONS**

H. Faig[1], S. Cohen[1], D. Sadot[1], L. Gantz[2]; [1]IL, [2]Yokneam, IL

12:00 - 13:30 **Lunch Break (ON OWN)**

WD

13:30 - 15:00 **RF/High-Speed Testing III** **Mesa Ballroom**

Moderation: D. Kuchta, US

13:30 - 14:00 **WD1 - A 112 Gb/s Optical Link Based on Silicon Photonics and CMOS Electronics**

H. Rong[1], H. Li[2], G. Balamurugan[2], M. Sakib[1], R. Kumar[1], H. Jayatilleka[1], O. Dosunmu[1], A. Liu[1], J. Jaussi[2], B. Casper[2]; [1]Santa Clara, CA/US, [2]Hillsboro, OR/US

14:00 - 14:15 **WD2 - SELF-HOMODYNE 16-QAM SCHEME FOR LOW COMPLEXITY 200 GBPS DATA CENTER INTERCONNECTS**

R. Kamran, S. Naaz, S. Manikandan, S. Goyal, R. Ashok, S. Gupta; Mumbai, IN

14:15 - 14:30 **WD3 - REAL-TIME DIGITAL SUBCARRIER CROSS-CONNECT BASED ON DISTRIBUTED ARITHMETIC DSP ALGORITHM**

T. XU[1], R. Hui[2]; [1]KS/US, [2]Lawrence, AL/US

14:30 - 15:00 **WD4 - HIGH-SPEED ATTO-JOULE PER BIT PHOTONIC CRYSTAL NANOCAVITY MODULATOR**

E. Li, A. Wang; Corvallis, OR/US

15:00 - 15:30 **Coffee Break/Exhibits**

WE

15:30 - 17:30 **Workshop on 5G** **Mesa Ballroom**

A 4x25-Gbps Monolithically Integrated Si Photonic WDM Transmitter with Ring Modulators

Minkyu Kim[1], Kangyeob Park[2], Won-Seok Oh[2],
Christian Mai[3], Stefan Lischke[3], Lars Zimmermann[3] and Woo-Young Choi[1]
[1]Department of Electrical and Electronic Engineering, Yonsei University, Seoul, South Korea
[2]SoC Platform Research Center, Korea Electronics Technology Institute, Seongnam 13509, South Korea
[3]IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany
minkyu226@yonsei.ac.kr

Abstract: We demonstrate a 100-Gbps (4x25-Gbps) Si Photonic WDM transmitter containing monolithically integrated Si ring modulators (RMs) and BiCMOS driving circuits. Our transmitter is designed with the large-signal circuit model for the Si RM, which allows easy and accurate optimization of the entire WDM transmitter.

Depletion-type Si ring modulators (RMs) attract a great amount of research and development interests because they provide high modulation bandwidth along with the small footprint and the wavelength-division multiplexing (WDM) capability [1,2]. These advantages can be further enhanced by the monolithic integration of RMs and driving circuits especially for the high-performance computing interconnect application. For this application, it is highly desirable if the entire WDM transmitter performance can be simulated in the standard IC design environment. We reported an accurate and easy-to-use large-signal circuit model for a RM [3] and, in this paper, present a 4x25-Gbps WDM transmitter whose performance is optimized based on the SPICE simulation of the RMs and the driving circuits.

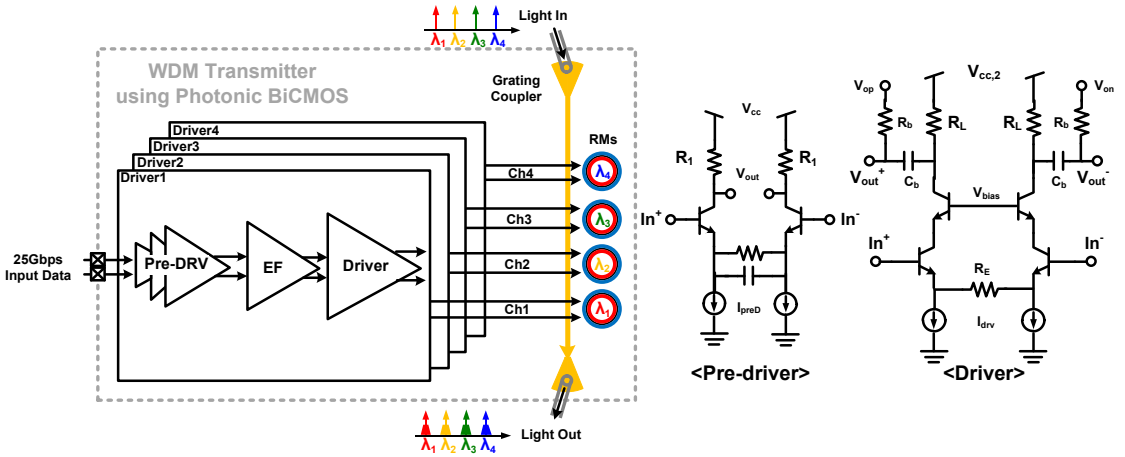

Fig. 1 Block diagram and schematic of the monolithic WDM transmitter

Fig. 1 shows the block diagram of our monolithic WDM Si transmitter containing pre-drivers, emitter-follower (EF) buffers, modulator driver circuits, and Si RMs. The target FSR of the Si RMs is 12nm and the target WDM channel spacing is 3nm around λ=1310nm. Since the RM's resonance wavelength changes due to the process variation and operation conditions, an on-chip heater is integrated next to each Si RM so that the RM resonance wavelength can be thermally tuned. Fig. 1 also shows the schematics for driver circuits implemented with SiGe BiCMOS technology. The pre-driver uses RC degeneration for high-speed operation. The driver has resistive degeneration and is connected to the Si RM with capacitive coupling. The cascade structure is used so that the driver can deliver up to 4-$V_{p2p,diff}$ swing to the RM from 4.5V supply without transistor breakdown.

Fig. 2(a) shows the measured normalized transmission characteristics at three different bias voltages for one of the RMs used in the transmitter. With 4-V_{p2p} driving voltage, it has about 8dB extinction ratio. From these measurement results, we can extract numerical values for three key parameters of Si RM: n_{eff} for the ring waveguide effective index, τ and τ_l for the decay time constant of the energy amplitude in the coupled and the uncoupled ring resonator, respectively [4]. These parameters can be converted into circuit parameters for the Si RM equivalent circuit model shown in Fig. 2(b), details of which can be found in [3]. Table I lists the numerical values for the key parameters and circuit parameters.

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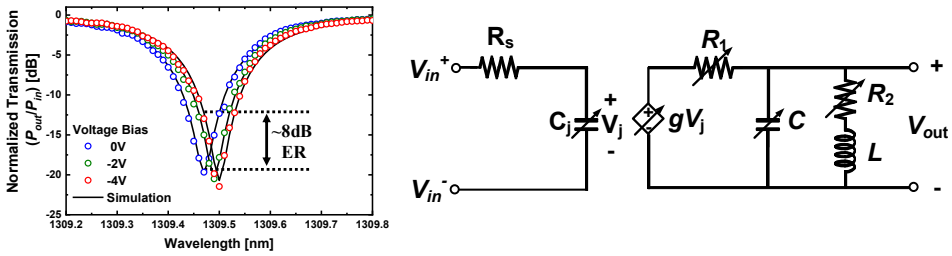


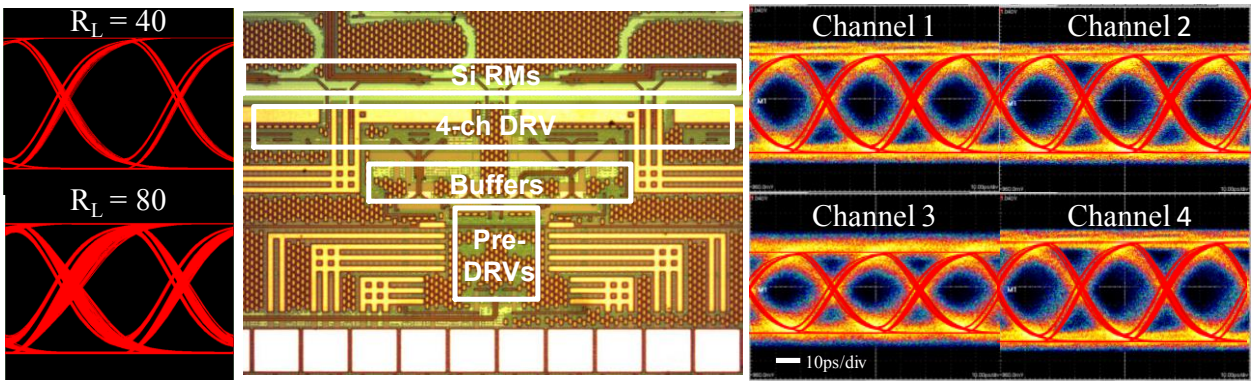
(a) (b)

Fig. 2(a) Measured and simulated transmission characteristics of Si RM for different V_{Bias} and (b) large-signal equivalent circuit model for Si RM

TABLE I: EXTRACTED SI RM PARAMETER VALUES AND CALCULATED RLC VALUES FOR CIRCUIT MODEL

V_{Bias} (V)	n_{eff}	τ_1 (ps/rad)	τ (ps/rad)	R_1 (kΩ)	R_2 (kΩ)	C (fF)	L (nH)
0	2.730962	22.27	7.11	8.181	10.27	0.97	114.413
-2	2.731004	22.82	7.17	9.474	10.02	0.84	
-4	2.731024	23.11	7.19	10.452	9.90	0.76	

Using the RM circuit model, the monolithic Si WDM transmitter is designed and fabricated by IHP's Photonic BiCMOS foundry service, which provides high-performance 0.25-μm SiGe BiCMOS circuits and Si photonic components on the same wafer [5]. For the optimization of the transmitter performance, careful selection of the load impedance (R_L) for each driver circuit is important since it determines the driver bandwidth as well as the power consumption. Fig. 3(a) shows the simulated eye diagrams for the entire transmitter having two different R_L values. Although larger R_L provides smaller power consumption, it limits bandwidth of the whole transmitter as shown in the eye diagram. The total power consumption for 100-Gbps operation is 1126mW, excluding the external laser and heater power. The transmitter performance optimization can be easily done in the SPICE environment as the RM behavior is accurately modeled with the RM equivalent circuit. Fig. 3(b) shows the photo of the fabricated chip whose active area is 0.16mm^2. Fig. 3(c) shows the measured 25-Gbps NRZ eye diagrams. Also shown are the SPICE simulated eye diagrams which agree well with the measured results. More details of our design optimization and measured results will be presented.



(a) (b) (c)

Fig. 1(a) Simulated eye diagram for 25-Gbps with different load resistance of the driver circuit, (b) Chip photo of our WDM transmitter, and (c) 25-Gbps NRZ measured results for four different channels with simulated results (solid)

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[2]A. H. Atabaki *et al.*, "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip," *Nature*, vol. 556, no. 7701, pp. 349–354, 2018.
[3]M. Kim *et al.*, "A Large-signal Equivalent Circuit for Depletion-type Silicon Ring Modulators," in *Optical Fiber Communication Conference*, 2018, vol. 1, no. c, p. Th2A.13.
[4]B. E. Little, S. T. Chu, H. A. Haus, J. Foresi, and J.-P. Laine, "Microring resonator channel dropping filters," *J. Light. Technol.*, vol. 15, no. 6, pp. 998–1005, Jun. 1997.
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