

제25회 한국반도체학술대회

The 25th Korean Conference on Semiconductors
2018년 2월 5일(월) ~ 7일(수) | 강원도 하이원리조트 컨벤션 호텔

Semiconductor Technology for the Paradigm Shift

사전등록, 숙박 예약을 서둘러 주시기 바랍니다.

사전 등록 마감일: 2018년 1월 12일 (금)
숙박 예약 마감일: 2018년 1월 25일 (목)

*사전등록 및 숙박예약 마감일을 확인하시어, 진행 해주시기 바랍니다.
*숙박예약은 선착순으로 진행되어, 조기 마감 될 수 있습니다.

등록 바로가기
숙박 바로가기

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초록접수마감
2017. 11. 3 (금) |
초록채택통보
2017. 12. 15 (금) |
사전등록마감
2018. 1. 12 (금) | <ul style="list-style-type: none"> ▶ 모집분야 http://kcs.cosar.or.kr/2018/cfp.jsp ▶ KCS 2018 Poster http://kcs.cosar.or.kr/2018/program.jsp ▶ 사전등록 안내 http://kcs.cosar.or.kr/2018/registration.jsp ▶ 행사장 안내 http://kcs.cosar.or.kr/2018/accommodation.jsp ▶ KCS 2018 Poster Download http://kcs.cosar.or.kr/2018/download/KCS2018Poster.pdf ▶ KCS 2018 Venue http://kcs.cosar.or.kr/2018/venue.jsp |
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초대의 글

국내 반도체 분야를 세계적인 수준으로 발전시키는데 크게 기여한 반도체인의 전치, 한국반도체학술대회가 2018년에 어느덧 25회를 맞이하게 되었습니다. 1994년 첫 대회 이후 매년 1,300여명이 참석하는 한국반도체 분야의 최대 행사인 제 25회 한국반도체학술대회가 2018년 2월 5일(월)부터 7일(수)까지...
[+ 더보기 \(welcome.jsp\)](#)

제 25회 한국반도체학술대회 (KCS 2018)

오늘	2018년 2월							인체	주	월	일
28	29	30	31	2월 1일	2	3					
4	5	6	7	8	9	10					
제 25회 한국반도체학술											
11	12	13	14	15	16	17					
18	19	20	21	22	23	24					
25	26	27	28	3월 1일	2	3					

다음 시간대로 표시된 일정: 서울 캘린더

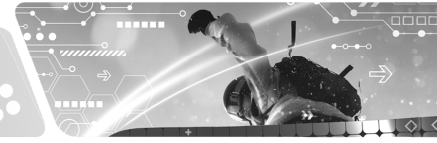


주관 서강대학교 SOGANG UNIVERSITY http://www.sogang.ac.kr/index.do	주최 KSIA 한국반도체산업협회 https://www.ksia.or.kr/ COSAR 한국반도체연구조합				
대한전자공업협회 http://www.ieek.or.kr/ 반도체설계교육센터 http://www.idec.or.kr/					
대전광역시 유성구 배울1로, 273 (우)34036, (주)제니컴 TEL 042-472-7460 FAX 042-472-7459 E-mail kcs@ksia.or.kr mailto:kcs@ksia.or.kr					
제25회 한국반도체학술대회 The 25 th Korean Conference on Semiconductors					

Program at a Glance

제 25회 한국반도체학술대회 (KCS 2018)
2018년 2월 5일(월)-7일(수) / 강원도 하이원리조트 컨벤션 호텔

2월 5일(월)	5층			5층			5층			5층	
	컨벤션홀 L			태백룸			함백룸				
14:00-18:00	[Short Course 1] 뉴로모픽(Neuromorphic) 기술의 이해			[Short Course 2] Quantum Computing			[Short Course 3] SI-PI-EMI Analysis of Advanced Semiconductor Packaging Technologies				
2월 6일(화)	5층				6층						5층
	Room A 태백I	Room B 태백II+III	Room C 함백I	Room D 함백II+III	Room F 봉래I	Room G 봉래II+III	Room H 청옥I	Room I 청옥II+III	Room J 육백I	Room K 육백II	
08:15-09:00				TD0-S Chip Design Contest							
09:00-10:45	TA1-A Emerging Interconnect	TB1-I Gas/Chemical Sensors	TC1-D Oxide Thin Film Transistor	TD1-R 고성능 스토리지 기술	TF1-F Neuromorphic Device and Application	TG1-G Advanced Devices I - Technology and Simulation	TH1-J Graphene Related Nano Materials	TI1-K ReRAM I - Preparing for Mass Production	TJ1-M RF and Wireless System and Circuits I	TK1-Q Metrology & Inspection	전시
10:45-10:55	휴식 (& 커피, 다과)										
10:55-11:00	개회식 [컨벤션홀 K+W / 5층]										
11:00-12:00	기조강연 1: Prof. Sanjay Banerjee (University of Texas at Austin) "Electronics in Flatland" [컨벤션홀 K+W / 5층]										
12:00-13:00	점심 [포레스트볼룸 / 4층]										
13:00-14:00	기조강연 2: 김진형 원장 (AIR(인공지능연구원)) "인공지능의 능력과 한계" [컨벤션홀 K+W / 5층]										
14:00-14:10	휴식 (& 커피, 다과)										
14:10-15:55	TA2-A FOWLP & Reliability	TB2-I Advanced Sensor Systems	TC2-D Emerging Thin Film Technology	TD2-R 시스템 소프트웨어 응용	TF2-F Intergration Technology	TG2-G Modeling and Simulation I - Nano Devices	TH2-J Two Dimensional Nano Materials	TI2-K Devices for Neuromorphic Computing	TJ2-M RF and Wireless System and Circuits II	TK2-Q Nanoanalysis	
16:00-17:30											포스터세션1 [TP1]
17:40-20:00	만찬 [컨벤션홀 K+W / 5층]										
20:00-	[Rump Session 1] 한국 시스템 반도체 산업의 미래		[Rump Session 2] 한국 메모리 반도체의 미래/차세대 메모리 반도체 기술								
2월 7일(수)	5층				6층						5층
	Room A 태백I	Room B 태백II+III	Room C 함백I	Room D 함백II+III	Room F 봉래I	Room G 봉래II+III	Room H 청옥I	Room I 청옥II+III	Room J 육백I	Room K 육백II	
09:00-10:30	WA1-C Material Growth and Characterization I	WB1-SS Special Session: 인공지능	WC1-D ALD/CVD Process (2D Materials)	WD1-R 다양한 소프트웨어 최적화 기술	WF1-F Steep-Slope I: Tunnel-FET	WG1-G Advanced Devices II - Simulation and Reliability	WH1-B 리소그래피 및 플라즈마에칭	WI1-K Topics Related to Memory Design	WJ1-LM Analog & RF Circuits	WK1-Q Inspection & Yield Enhancement	전시
10:30-10:45	휴식 (& 커피, 다과)										
10:45-12:15	WA2-C Material Growth and Characterization II	WB2-SS Special Session: IoT I	WC2-D Thin Films for Memories and Transistors I	WD2-E III-V Emerging Device	WF2-F Reliability	WG2-G Advanced Devices III - Simulation and Reliability	WH2-J Nano Materials and Nano Structures	WI2-K ReRAM II - New Technologies	WJ2-L Analog Circuit Design	WK2-O VLSI System Design and Application I	
12:15-13:15	점심 [포레스트볼룸 / 4층]										
13:15-14:45	WA3-P Device for Solar Energy Conversion	WB3-SS Special Session: IoT II	WC3-I Flexible Sensor Systems	WD3-E GaN Device	WF3-F Photonics and Nanowire Technology	WG3-G Modeling and Simulation II - Device and Process	WH3-J CNT Related Nanotechnology	WI3-K FeRAM and Transparent ReRAM	WJ3-N IoT & SoC Methodology	WK3-O VLSI System Design and Application II	
14:45-16:15	휴식 (& 커피, 다과)				휴식 (& 커피, 다과)						포스터세션2 [WP1]
16:15-17:30	WA4-P Fabrication for Functional Energy Device	WB4-H Display and Imaging	WC4-D Thin Films for Memories and Transistors II	WD4-E SiC Device	WF4-F Steep-Slope II: NC-FET	WG4-G Memory and TFT - Modeling and Characterization	WH4-J General Nano Technology	WI4-K Phase-Change Memory	WJ4-N Test & Reliability		전시
17:30-17:40	폐회식 및 경품추첨 [6층, 육백룸]										



2018년 2월 7일(수), 13:15-14:45

Room K (육백II, 6층)

O. System LSI Design **분과**

[WK3-O] VLSI System Design and Application II

좌장: 김경기 교수(대구대학교), 김수연 교수(동국대학교)

WK3-O-1 13:15-13:30	Design of FMCW Radar Signal Processor for Drone Altitude Measurement Yongchul Jung, Euibeen Lim, Sora Jin, and Yunho Jung <i>School of Electronics and Information Engineering, Korea Aerospace University</i>
WK3-O-2 13:30-13:45	Design of a High Precision Ramp Generator for a 14-bit Single-Slope ADC Hyeonseob Noh, Sooyoun Kim, and Minkyu Song <i>Department of Semiconductor Science, Dongguk University</i>
WK3-O-3 13:45-14:00	Efficient Reconfigurable Architecture to Accelerate Descriptor Extraction in SURF Algorithm Yoonjin Kim and Haelim Jung <i>Department of Computer Science, Sookmyung Women's University</i>
WK3-O-4 14:00-14:15	A 25-Gbps Low-Power PAM-4 Transmitter in 28-nm CMOS <u>Minkyu Kim, Dae-Hyun Kwon, Sung-Geun Kim, and Woo-Young Choi</u> <i>Department of Electrical and Electronic Engineering, Yonsei University</i>
WK3-O-5 14:15-14:30	Radiation Hardened Microprocessor Design Using Spatial and Temporal Dual Modular Redundancy Jun Sung Go, Jong Kang Park, Jong Tae Kim <i>School of Electronic and Electrical Engineering, Sungkyunkwan University</i>
WK3-O-6 14:30-14:45	Reducing FPGA Area Using Nano-Switch Devices in Inter and Intra-Logic Routing Aidyn Zhakatayev and Jongeun Lee <i>School of Electrical and Computer Engineering, UNIST</i>

[WK3-O-4]

A 25-Gbps Low-Power PAM-4 Transmitter in 28-nm CMOS

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With the required amount of data transmission for many applications continuously increasing, the use of multiple data levels has become an efficient solution for increasing transmission capacity without bandwidth increase. In particular, PAM-4 signaling is now widely considered for many electrical and optical wireline applications due to its enhanced spectral efficiency [1]. This paper reports a 25-Gbps PAM-4 transmitter realized in 28-nm CMOS technology. Fig. 1(a) and (b) show the block diagram of our transmitter as well as a chip photo. A built-in PRBS generator generates 8-parallel 1.5625 Gb/s 2^7-1 PRBS data using 1.5625 GHz clock signal produced by an on-chip PLL. The serializer serializes these parallel data using data transition information for power consumption reduction [2]. The voltage-mode driver provides PAM-4 output with 120-mV peak-to-peak swing. The entire transmitter consumes only 29mW, much smaller than the previous reports [3]. Fig. 1(c) shows the measured eye diagram.

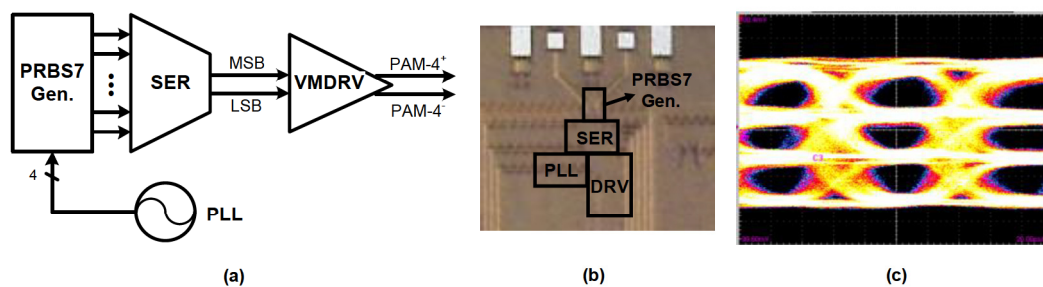


Fig 1. (a)Block diagram and (b)chip photo of PAM-4 transmitter, and (c)measured eye-diagram

Acknowledgments

This work was supported in part by Samsung Electronics and the National Research Foundation of Korea grant funded by the Korean Ministry of Science, ICT and Future Planning (No. 2015R1A2A2A01007772). Authors are thankful to IC Design Education Center (IDEC) for EDA support.

References

- [1] M. Bassi, F. Radice, M. Bruccoleri, S. Erba, and A. Mazzanti, "3.6 A 45Gb/s PAM-4 transmitter delivering 1.3Vppd output swing with 1V supply in 28nm CMOS FDSOI," *IEEE Int. Solid-State Circuits Conf.*, Feb. 2016, pp. 66–67.
- [2] S.-G. Kim, T. Kim, D.-H. Kwon, and W.-Y. Choi, "A 5–8 Gb/s low-power transmitter with 2-tap pre-emphasis based on toggling serialization," in *2016 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2016, pp. 249–252.
- [3] C. Menolfi *et al.*, "A 25Gb/s PAM4 transmitter in 90nm CMOS SOI," in *ISSCC. 2005 IEEE International Digest of Technical Papers. Solid-State Circuits Conference, 2005.*, 2005, pp. 77–78.