An Asymmetrically-Sampling 10-Gb/s CDR Circuit for Optical Receiver Performance Enhancement

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Abstract

We demonstrate a new type of optical receiver that contains a clock and data recovery (CDR) circuit having asymmetric samplers for electronic-photonic integrated circuit applications. The CDR directly samples pseudo-differential signals provided by the transimpedance amplifier (TIA) without any need for offset cancellation. This results in the reduction of the optical receiver power consumption and chip area. An optical receiver containing an equivalent circuit for the photodetector, TIA, and asymmetrically sampling CDR is implemented in 65-nm CMOS technology and the measurement results confirm the advantage of our new structure.

Keywords: Clock and Data Recovery (CDR); Electronic and Photonic Integrated Circuits (EPIC); Optical Receiver; Transimpedance Amplifier (TIA)

1. Introduction

There are a great amount of research and development interests for optical interconnect technology as the need for higher-bandwidth serial interfaces is continuously increasing and the conventional electrical interconnect technology is facing serious bandwidth, power, and footprint limitations. Furthermore, it is now possible to realize electronic and photonic integrated circuits (EPICs) for optical interconnect applications as photonic devices can be realized on Si platform with the Si processing technology [1, 2]. For successful implementation of Si EPICs, high-performance Si photonic devices are needed along with high-speed, power-efficient analog front-end circuits such as modulator drivers and transimpedance amplifiers (TIAs). Furthermore, serializer/deserializer (SerDes) circuits should be implemented in such a way that they are optimized for the target optical interconnect applications.

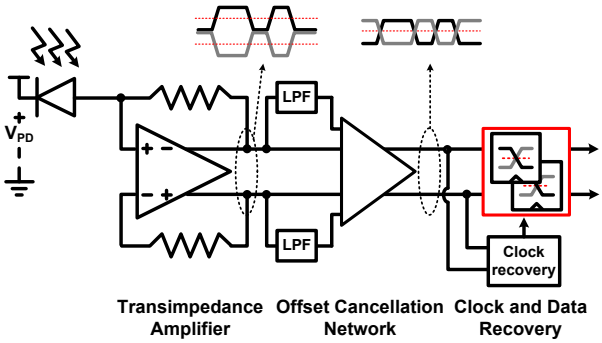

Fig. 1. Block diagram of conventional optical receiver.

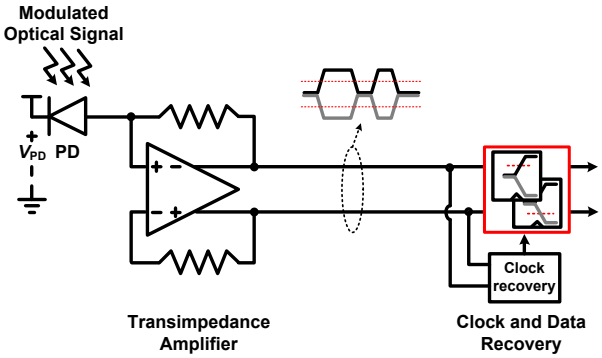

Fig. 2. Block diagram of proposed optical receiver.

Fig. 1 shows the architecture of the conventional optical receiver that includes a photodetector (PD), TIA, offset cancellation network (OCN), and a clock and data recovery (CDR) circuit [3]. A limiting amplifier is not included here since for optical interconnect applications TIA alone can provide sufficient signal levels required by CDR. For the high-speed operation required for the optical interconnect applications, differential-type TIA is preferred. However, since received optical signals are singled-ended, the PD provides single-ended signals to TIA. Consequently, an OCN [4, 5] is needed, which cancels the DC offset and converts pseudo-differential signals to fully differential signals for CDR as shown in Fig. 1. However, OCN should

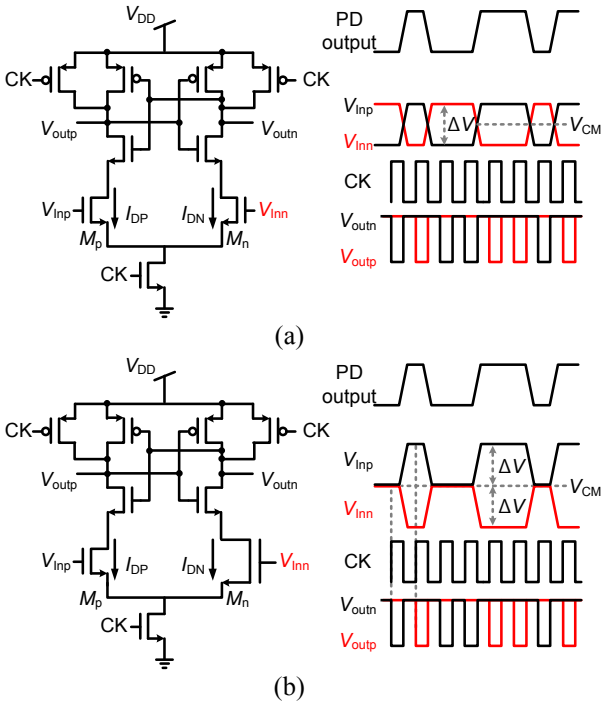

Fig. 3. Schematics of the sense-amplifier for (a) symmetric and (b) asymmetric sampler.

have a lower cutoff frequency to avoid the time-domain "droop" problem [6], which requires large resistance and capacitance, resulting in increased chip area. In addition, the OCN consumes a significant amount of power as it has to provide sufficient bandwidth. In this paper, we propose a novel architecture that allows the elimination of OCN. As shown in Fig. 2, the proposed architecture is based on CDR with an asymmetric sampler that can directly sample pseudo-differential signals provided by TIA with different decision thresholds for each of two differential input pairs. We demonstrate that such CDR can provide enhanced optical receiver performance in terms of power consumption and chip area.

2. Optical Receiver Circuits

A sense amplifier [8] (SA) is used for the CDR sampler since it has advantages in power consumption and sensitivity. In addition, it can be easily analyzed when DC voltages are applied to differential input pairs [9]. In the conventional SA as shown in Fig. 3(a), the sampler is pre-charged to V_{DD} when the clock is off, and it discharges the currents corresponding to the input voltage level when the clock is on. Current imbalance caused by the input voltage level difference results in different output levels, which with the positive feedback produces the desired output. These SA characteristics can be used for sampling pseudo-differential signals by making

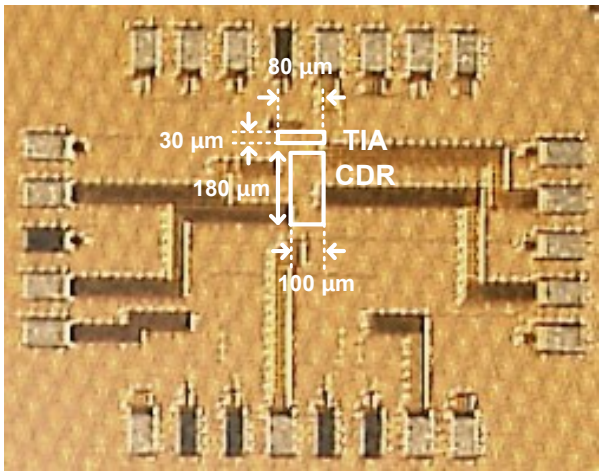

Fig. 4. Chip microphotograph of optical receiver with asymmetrically-sampling CDR.

the sizes of input MOSs different.

In Fig. 3(b), the size of M_n ($=W_n/L_n$) should be larger than that of M_p ($=W_p/L_p$) while $W_p \times L_p = W_n \times L_n$ is maintained so that two inputs provide the same load capacitance to the TIA. When there is no input light, the pseudo-differential input signals have the same voltage level. In this case, V_{outn} is discharged to ground when the clock is on, because I_{DN} is larger than I_{DP}. When there is input light, the pseudo-differential input signals have difference of $2\Delta V$. In this case, the discharged output should be V_{outp} rather than V_{outn} in order to avoid any errors. This requires I_{DP} larger than I_{DN}.

$$I_{DP} > I_{DN} \tag{1}$$

$$\text{where } I_{DP} = \frac{1}{2}\mu_n C_{OX}\frac{W_p}{L_n}\left(V_{GS,M_p} - V_{TH,M_p}\right)^2 \tag{2}$$

$$\text{and } I_{DN} = \frac{1}{2}\mu_n C_{OX}\frac{W_n}{L_n}\left(V_{GS,M_n} - V_{TH,M_n}\right)^2 \tag{3}$$

Substituting Eq. (2) and (3) into Eq. (1),

$$\frac{W_p \times L_n}{L_p \times W_n} > \frac{\left(V_{CM} - V_S - \Delta V - V_{TH,M_n}\right)^2}{\left(V_{CM} - V_S + \Delta V - V_{TH,M_p}\right)^2}. \tag{4}$$

With Eq. (4), we can determine input MOS sizes for target ΔV.

10-Gbps optical receivers having quarter-rate CDR with two different asymmetric samplers satisfying Eq. (4) are designed in 65-nm CMOS technology. One sampler has M_p/M_n ratio of 0.5625, or W_p/L_p=7.5 μm/80 nm and W_n/L_n=10 μm/60 nm, and the other sampler has M_p/M_n ratio of 0.25, or W_p/L_p=5 μm/120 nm and W_n/L_n=10 μm/60 nm. Both optical receivers contain an identical TIA which

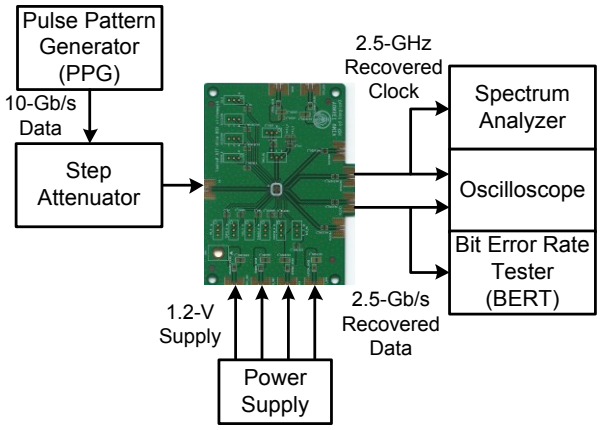

Fig. 5. Measurement setup for optical receiver.

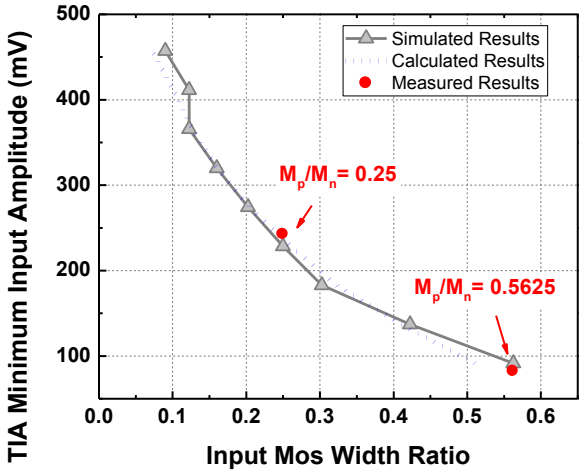

Fig. 6. Input sensitivity of proposed optical receiver with simulation and calculation results.

employs the shunt-feedback topology [7] and the equivalent circuit for the photodetector consisting of 30-fF capacitor and 2-kΩ resistor along with 50-Ω termination resistor needed for measurement.

3. Measurement Results

Fig. 4 shows the microphotograph of the fabricated optical receiver. The TIA core area is 0.0024 mm^2 (30 μm×80 μm) and that of CDR is 0.018 mm^2 (100 μm×180 μm).

Fig. 5 shows the measurement setup for evaluating the optical receiver circuit performance. The fabricated chip is mounted on printed circuit board (PCB) and wire bonded. A pulse pattern generator (PPG) provides 10-Gb/s 2^7-1 PRBS patterns to the optical receiver. Spectrum analyzer and oscilloscope are used to measure the recovered clock and data. Bit error rate tester (BERT) is used to confirm the CDR does not generate any error.

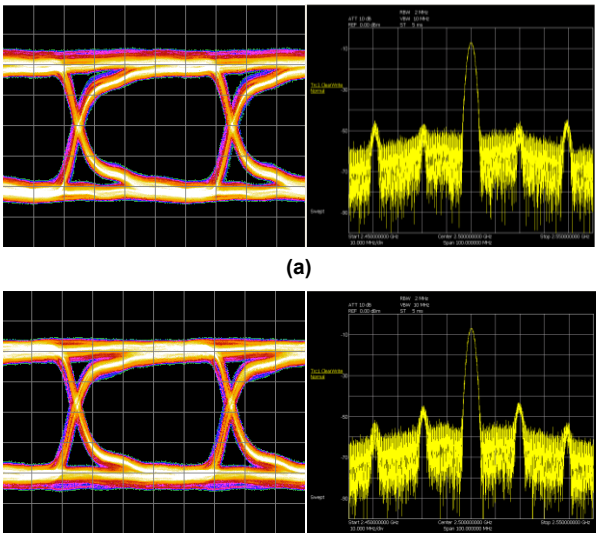

Fig. 7. (a) M_p/M_n=0.5625 and (b) M_p/M_n=0.25, 2.5-Gb/s retimed data eye-diagram and 2.5-GHz retimed clock spectrum.

Table 1: Performance summary

Data-rate [Gb/s]	10
Receiver architecture	PD model + TIA + CDR
Power consumption [mW]	10 (CDR core) 10 (VCO) 8 (TIA)
TIA minimum input amplitude [mV]	82 (M_p/M_n=0.5625) 242 (M_p/M_n=0.25)
Jitter of retimed data (RMS) [ps]	8.19 (M_p/M_n=0.5625) 7.56 (M_p/M_n=0.25)
Area [mm^2]	0.0024 (TIA) 0.018 (CDR)

Fig. 6 shows the measured minimum TIA input voltages for optical receivers having two different samplers when the BER is less than 10^{-12}. SPICE simulation and calculated results based on Eq. (4) are also shown in Fig. 6. Measured results agree very well with the simulated and calculated results.

Fig. 7 shows the measured retimed data eye-diagrams and retimed clock spectra for CDRs having two different samplers. Table I summarizes the performance of our circuit. In order to determine how much power consumption and chip-area is reduced with our new structure, we also designed OCN used for 10-Gbps optical receiver with symmetrically sampling CDR in the same 65-nm CMOS technology. The designed OCN consumes 5 mW and its area is

0.002 mm^2. This indicates that our new structure provides roughly 15% power and 9% area reduction.

The slight difference in measured jitter characteristics is due to the difference in loop gain for two types of CDR circuits caused by different input amplitudes.

4. Conclusion

A 10-Gb/s optical receiver circuit with asymmetrically sampling CDR is demonstrated in 65-nm CMOS technology. Our optical receiver circuit can directly sample pseudo-differential signals provided by TIA, resulting in reduced power consumption and chip area.

Acknowledgments

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