
kcs.cosar.or.kr
제23회 한국반도체학술대회
The 23rd Korean Conference on Semiconductors
대회개요 프로그램 초록제출 초록발표 참가등록 전시/후원 장소/숙박 커뮤니티
• 발표안내 • 역대 발표초록 검색
제23회 한국반도체학술대회
The 23rd Korean Conference on Semiconductors
2016년 2월 22일(월)~24일(수) | 강원도 하이원리조트
"Over the Barrier, Toward the Next"
D- -4
초록접수마감 2015.11.20(금)
2015.11.13(금)
초록채택통보 2015.12.23(수)
2015.12.18(금)
사전등록마감 2016.01.29(금)
모집분야 프로그램
초록작성 숙박안내
사전등록 뉴스레터
Call for Paper
Call for Participation
공지사항
KCS 2016에 대한 최근 소식
• 온라인 등록시스템이 오픈되었습니다.
• 온라인 초록접수가 성황리에 마감되었습니다.
• 호텔/리조트 예약은 12월 1일부터 가능합니다.
• Tentative Program이 업데이트 되었습니다.
KCS
46 개 좋아요
페이지 좋아요
공유하기
친구 중 제일 먼저 좋아요를 클릭하세요
KCS
2015년 12월 23일
제23회 한국반도체학술대회 사무국입니다.
오늘은 크리스마스 이브입니다.
모두 행복 가득하고, 따뜻한 크리스마스 보내시길 바랍니다.^^
**초록채택통보는 12월 23일~24일 개별 메일로 통보진행되었으니
확인을 부탁 드립니다.... 더 보기
FAQ
자주 묻는 질문과 답변
1. 논문은 몇 번 제출하나요?
2. 사무국 연락처는 무엇인가요?
장소안내
주관
성균관대학교 SUNGKYUNKWAN UNIVERSITY
KSIA 한국반도체산업협회
COSAR 한국반도체연구조합
주최
KPS 한국물리학회 The Korean Physical Society
MRS 한국재료학회 Materials Research Society of Korea
대한전기학회
IEIE 대한전자공학회 The Institute of Electronics and Information Engineers
IDEC 반도체설계교육센터 IC DESIGN EDUCATION CENTER
후원
GWCVB 강원컨벤션뷰로

[제23회 한국반도체학술대회_Program at a Glance]

2월 22일(월)	Room A 태백룸(5층)	Room B 함백룸(5층)
14:00-18:00	[Short Course 1] 3차원 집적 기술: 원리와 응용	[Short Course 2] 차세대 저전력소자의 개발과 설계

2월 23일(화)	Room A	Room B	Room C	Room D	Room E	Room F	Room G	Room H	Room I	Room J	Room K	Room L
	5층					6층						5층
	태백I	태백II+III	함백I	함백II+III	컨벤션홀L	봉래I	봉래II+III	욱백I	욱백II	청옥I	청옥II+III	로비
08:30-10:30	[TA1-L] Analog Design I	[TB1-D] 1D/2D Materials & Devices	[TC1-F] Novel Si Devices and Integrated Circuits (4)	[TD1-G] Device Physics and Characterization 1 : Field-effect		[TF1-I] High efficiency sensors and devices	[TG1-F] Novel Si Devices and Integrated Circuits (1)	[TH1-J] Nanofabrication for Application		[TJ1-K] Memory processing and RRAM operation	[TK1-R] Interaction of system SW and semiconductor	
10:30-10:40	휴식 (& 커피, 다과)											
10:40-12:40	[TA2-L] Analog Design II	[TB2-D] Oxide Semiconductors	[TC2-M] RFIC and smart RFID tags	[TD2-G] Reliability Analysis : Thin-film transistors and field-effect transistors		[TF2-O] VLSI System Design for Communications	[TG2-F] Novel Si Devices and Integrated Circuits (2)	[TH2-J] Nanofabrication for Application	CDC	[TJ2-K] NAND, PCRAM, and MRAM	[TK2-R] Little more faster, and even better reliability	
12:40-13:40	점심 [포레스트볼룸 / 4층]											Chip Design Contest & 전시
13:40-14:20	기조강연 1 : Prof. Akira Toriumi (The University of Tokyo) "Materials Innovation for Versatile Electron Devices in IoT Era" [컨벤션홀 K+W / 5층]											
14:20-15:00	기조강연 2 : 박재근 교수 (한양대학교) " Nonvolatile Memory Technology beyond 20nm : Dilemma & Challenge" [컨벤션홀 K+W / 5층]											
15:00-15:10	휴식 (& 커피, 다과)											
15:10-17:10	[TA3-A] A2: Enabling packaging technologies	[TB3-D] Process Technology for Thin Films	[TC3-H] Display and Imaging Technologies	[TD3-G] Device Modeling and Simulation 1 : RF, teraherz, low-power, and		[TF3-Q] Metrology and Inspection I	[TG3-F] Novel Si Devices and Integrated Circuits (3)	[TH3-J] Graphene and Related Carbon Nanostructures	[TI1-N] Advances in Design Technology	[TJ3-K] Circuit related topics and memory selectors	[TK3-E] Advanced GaN Technology	
17:10-18:30					포스터 세션1 [TP1]							
18:30-20:00	만찬 [컨벤션홀 K+W / 5층]											
20:00-	Rump Session 1 : 스케일링 한계 극복을 위한 미래 반도체 기술 [태백룸 / 5층] Rump Session 2 : 초연결 사회의 반도체 기술 전망과 과제 [함백룸 / 5층]											

2월 24일(수)	Room A	Room B	Room C	Room D	Room E	Room F	Room G	Room H	Room I	Room J	Room K	Room L
	5층					6층						5층
	태백I	태백II+III	함백I	함백II+III	컨벤션홀L	봉래I	봉래II+III	욱백I	욱백II	청옥I	청옥II+III	로비
08:30-10:00	[WA1-A] A1: Contact and thin film technologies for high performance	[WB1-D] Thin Films for Emerging Devices I	[WC1-C] Materials Growth & Characterization : Emerging new electrical	[WD1-G] Device Physics and Characterization 2 : Memory devices		[WF1-Q] Metrology and Inspection II	[WG1-F] Materials and Processing Technologies	[WH1-J] Two-Dimensional Materials beyond Graphene	[WI1-N] Architecture-Level Design Techniques	[WJ1-K] Unconventional approaches in memory research	[WK1-E] GaN Power Device	
10:00-10:10	휴식 (& 커피, 다과)											
10:10-11:40	[WA2-A] A3: Novel interconnect and packaging technologies for emerging	[WB2-D] Thin Films for Emerging Devices II	[WC2-C] Materials Growth & Characterization : III-Nitrides and Si	[WD2-G] Device Modeling and Simulation 2 : Ab-initio and theoretical study		[WF2-O] VLSI System Design and Applications	[WG2-F] Si and Group-IV Photonics	[WH2-J] Two-Dimensional Materials / Spintronics	[WI2-B] Patterning	[WJ2-P] Device for Energy (Solar Cell, Power Device, Battery, etc.)	[WK2-E] III-V Device	전시
11:40-13:00					포스터 세션2 [WP1]							
13:00-	점심 [포레스트볼룸 / 4층]											

[Panel]
CDC_201501054 **주파수 체배기가 집적된 CMOS 기반 G-band 신호원**
주저자: 김정수
지도교수: 이재성
고려대학교

[Panel]
CDC_201501055 **5-GHz Phase-Locked Loop Using Pseudo-Differential Delay Cell With Linear VCO Gain**
주저자: 김민규
지도교수: 최우영
연세대학교

[Panel]
CDC_201501056 **Multi-channel neural recording system**
주저자: 장정우
지도교수: 송윤규
서울대학교

[Panel]
CDC_201501057 **Application of the Common-Centroid Layout Method for High Randomness of PUF**
주저자: 최강운
지도교수: 홍종필
충북대학교

[Panel]
CDC_201501058 **High gain and low noise switched capacitor TIA for sensor readout circuits**
주저자: 정훈주
지도교수: 정훈주
금오공과대학교

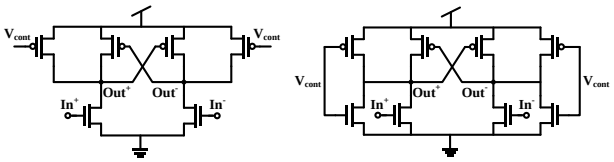
[Panel]
CDC_201501059 **Cross Coupled VCO의 구조에 따른 FoM 분석**
주저자: 고가연
지도교수: 박창근
숭실대학교

[Panel]
CDC_201501060 **0.3-V Supply Charge pump circuit for 65 nm CMOS**
주저자: Heesauk Jhon
지도교수: 최우영
서강대학교

5-GHz Phase-Locked Loop Using Pseudo-Differential Delay Cell With Linear VCO Gain

Minkyu Kim, Tongsung Kim and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University
Seodaemun-gu, Seoul 120-749, Korea
minkyu226@yonsei.ac.kr

There are great amounts of researches and development interests in high-performance phase-locked loop (PLL) circuits. Voltage-controlled oscillators (VCOs) with pseudo-differential delay cells have advantages of low jitter, low power, and multi-phase output [1]. However, they have non-linear gain characteristics. In this study, we modified delay cell structures for the goal of linearizing VCO gain characteristics. Fig. 1 shows the schematics of the conventional delay cell and newly-proposed pseudo-differential delay cells. Fig. 2 shows post-layout simulation result for VCO gain characteristics for both structures.



(a) (b)

Fig1. Schematic of (a) conventional (b) proposed delay cell

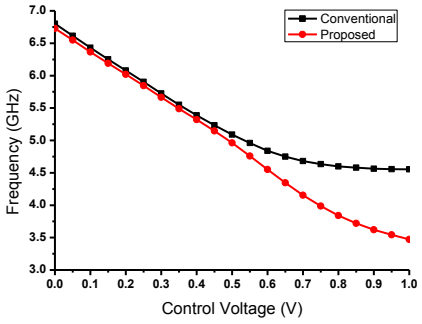


Fig2. Simulated VCO output frequency

Fig. 3 shows the overall PLL block diagram, which produces 5-GHz clock signals with 156.25-MHz reference clock. Our PLL circuit is implemented in standard 65-nm CMOS technology. Fig. 4 shows the microphotograph of the fabricated chip. Fig. 5 shows measured VCO gain characteristics and time-domain output signals. These results prove that pseudo-differential delay cell has linearized VCO gain. The PLL consumes 4mW and have 4.1ps RMS jitter with 5-GHz output clock.

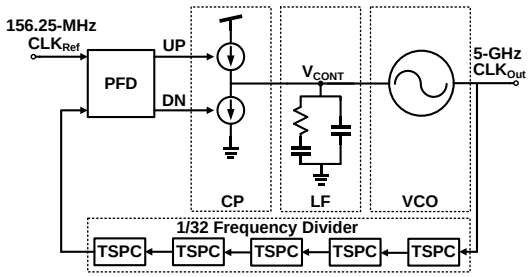


Fig3. Block diagram of designed PLL

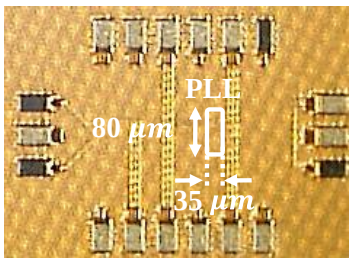
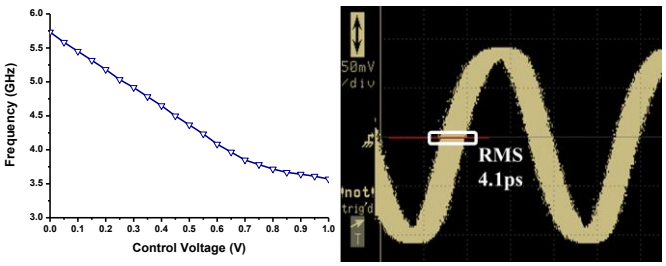


Fig4. Chip microphotograph of PLL



(a) (b)

Fig5. Measured (a) VCO output frequency (b) eye diagram

REFERENCE

[1] S.-J. Lee, et al., "A Novel High-Speed Ring Oscillator for Multiphase Clock Generation Using Negative Skewed Delay Scheme", *IEEE J. Solid-State Circuits*, vol. 32, no. 2, Feb. 1997

This work was supported by the National Research Foundation of Korea grant funded by the Korea government (MEST) [2015R1A2A2A01007772]. The authors are also thankful to IDEC for MPW and EDA software support.

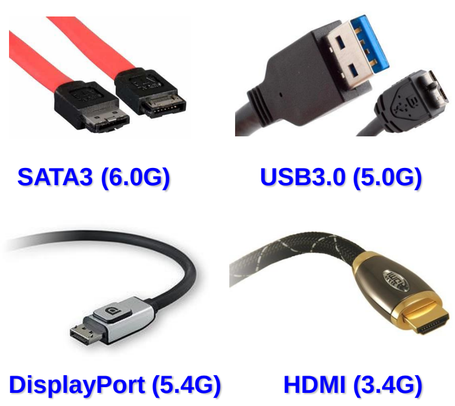
The 23rd Korean Conference on Semiconductor(KCS 2016)

5-GHz Phase-Locked Loop Using Pseudo-Differential Delay Cell With Linear VCO Gain

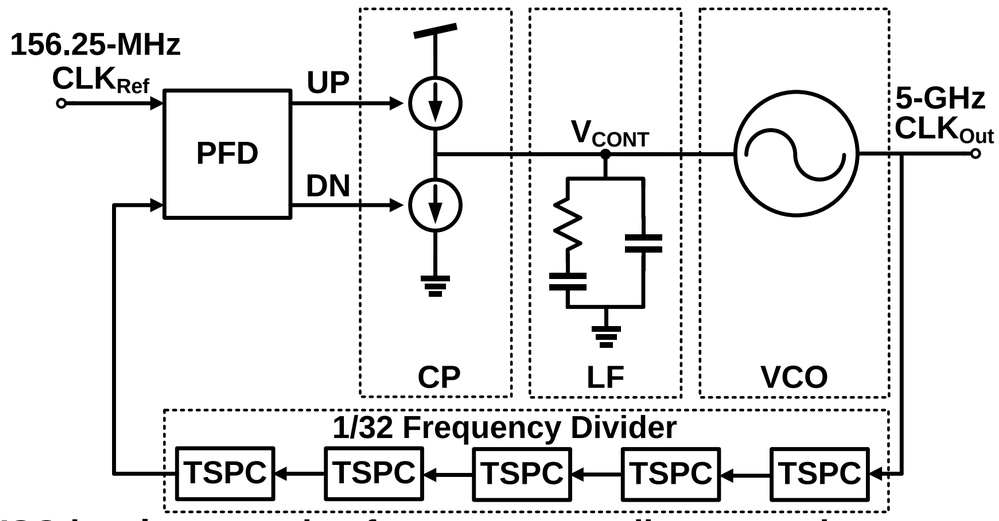
Minkyu Kim, Tongsung Kim and Woo-Young Choi
Department of Electrical and Electronic Engineering, Yonsei University, Seoul, Korea

PLL with Linear K_{VCO} for High-Speed Interconnect Application

High-Speed Interconnect Applications



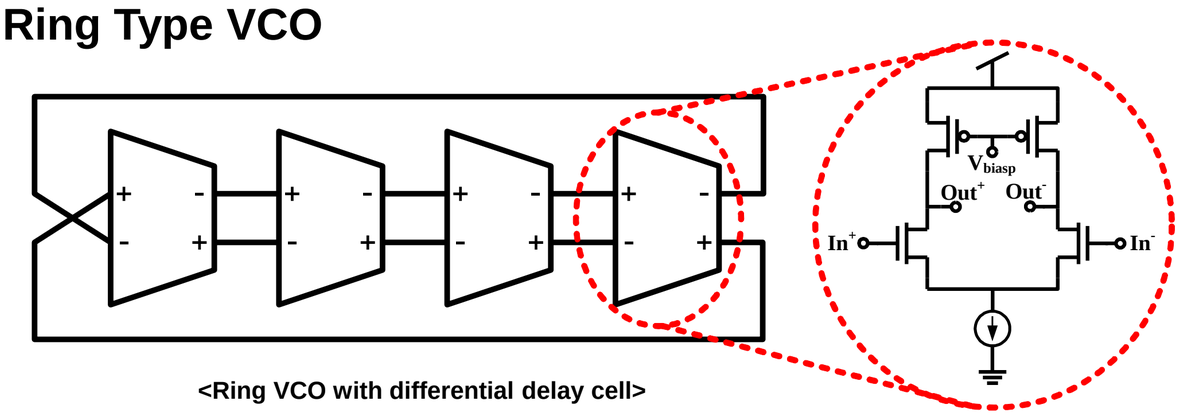
- ✓ High-speed electronic interconnect applications
  - USB, SATA, DisplayPort, HDMI, etc.
- ✓ Low-power, low-jitter PLL at transmitter required



- ✓ VCO has large portion for area, power, jitter, speed
- ✓ Small-area, high-speed, low-power, low-jitter VCO is described

Design of Linear K_{VCO}

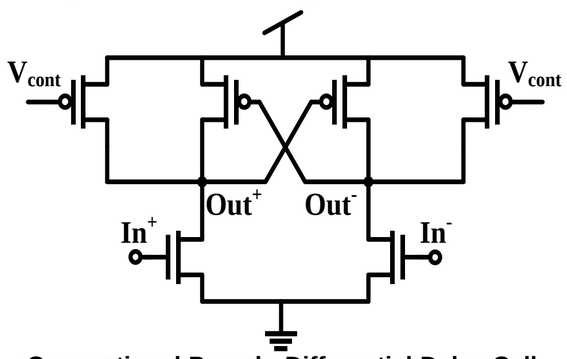
- **Ring Type VCO**



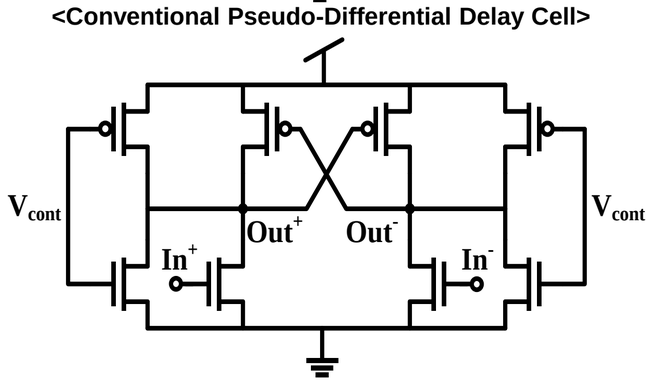
<Ring VCO with differential delay cell>

- ✓ Ring type VCO with differential delay cell is used widely for small-area, high-speed operation, *but static-power*
- ✓ Low-power VCO can be achieved by pseudo-differential delay cell, *but non-linearity* in certain control voltage range

- **Proposed Delay Cell**

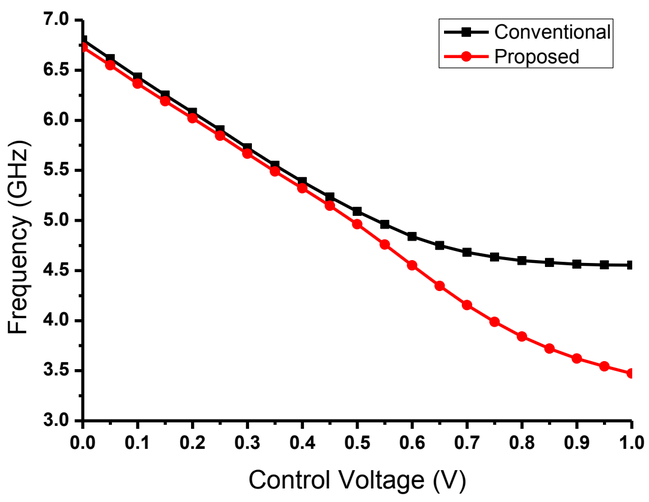


<Conventional Pseudo-Differential Delay Cell>



<Proposed Pseudo-Differential Delay Cell>

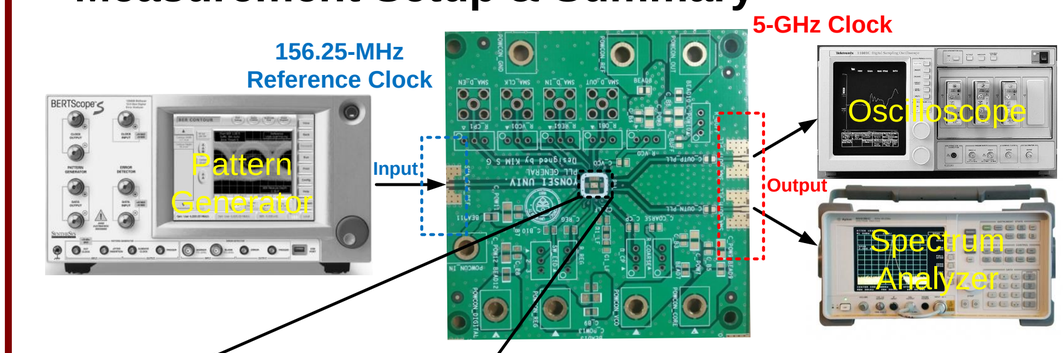
- **Simulation Result**

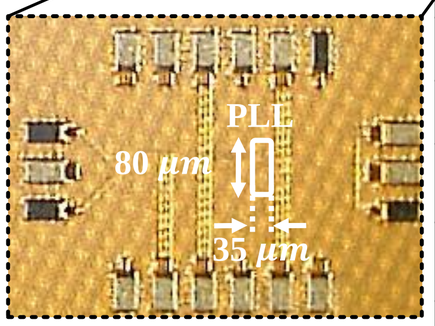


- ✓ Only PMOS control
  ➔Non-linear for higher control voltage
- ✓ Addition of NMOS control
  ➔Linear in wide range

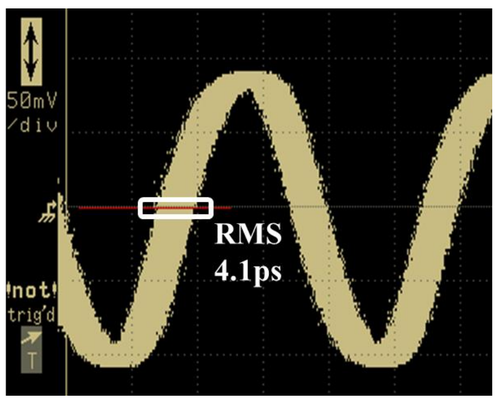
Measurement Results

- **Measurement Setup & Summary**

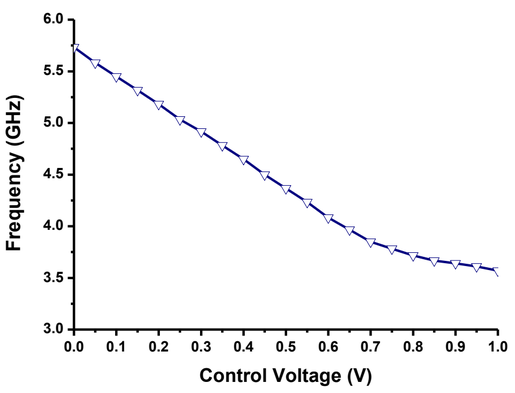




Clock Speed [GHz]	5
Technology	Standard CMOS 65-nm process
VCO architecture	Ring VCO with pseudo-differential delay cell
Power consumption [mW]	4 (PLL core)
RMS jitter [ps]	4.1
Area [mm²]	0.0028



<Measured eye diagram>



<Measured VCO output frequency>

- ✓ Linear pseudo-differential delay cell
  ➔High-speed, low-power, low-jitter PLL is achieved

Conclusion

❖ **5-GHz PLL with linear VCO gain in wide control voltage range is realized**