CALL FOR PAPERS

12th International SoC Design Conference

November 2-5, 2015 Hotel Hyundai, Gyeongju, Korea

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Host City: Gyeongju, Korea

Gyeongju is a coastal city in the far southeastern corner of North Gyeongsang Province in South Korea. Gyeongju was the capital of the ancient kingdom of Silla (57 BC - 935 AD). A vast number of archaeological sites and cultural properties from this period remain in the city. Gyeongju is often referred to as "the museum without walls". Among such historical treasures, Seokguram grotto, Bulguksa temple, Gyeongju Historic Areas, and Yangdong Folk Village are designated as World Heritage Sites by UNESCO. The many major historical sites have helped Gyeongju become one of the most popular tourist destinations in South Korea.

General Purpose of the Conference

International SoC Design Conference (ISOCC) aims at providing the world' s premier SoC design forum for leading researchers from academia and industries. Prospective authors are invited to submit papers of their original works emphasizing their own contributions. ISOCC 2015 is technically co-sponsored by IEEE CAS Society and accepted papers will be published on IEEE Xplore. We also welcome proposals for special sessions.

Conference Theme

The theme of ISOCC 2015 is "**SoC for Internet of Everything (IoE)**". The advent of IoE brings challenges and opportunities, especially for the entire silicon community. We will gather together for better solutions to make IoE possible. SoC solutions for IoE services require new approaches to march into the next level. ISOCC 2015 is looking for novel SoC solutions to open the IoE era.

Paper Submission

A complete **2-page manuscript** must be submitted electronically in PDF format (in Standard IEEE double-column format posted on the conference website). Only electronic submission will be accepted. For more information, please refer to the conference website: http://www.isocc.org

Important Dates

- Submission of special session proposals: June 30, 2015
- Notification of acceptance of special session proposals: July 10, 2015
- Submission of regular session full papers: ~~July 15, 2015~~ July 29,2015
- Submission of chip design contest papers: August 14, 2015
- Submission of special session full papers: July 31, 2015
- Notification of acceptance (for all submitted papers): September 1, 2015
- Submission of final papers (for all accepted papers): September 15, 2015
- Author and early-bird registration: September 15, 2015

Conference Venue-Hotel Hyundai Gyeongju

- Address: 336, Bomun-ro, Gyeongju-si, Gyeongsangbuk-do, Korea
- Website: https://www.hyundaihotel.com/gyeongju_en/
- Tel: +82-54-748-2233

Topics of Interest

Topics include, but are not limited to:

- Analog/RF/Mixed-Signal Circuits
- Analog Circuits
- Data Converters
- High-Speed Interface and Wireline ICs
- Wireless and RF ICs

- Power and Energy Circuits
- Power Management Circuit
- Energy Harvesting Circuits
- Power and Energy Circuits and Systems

- Digital VLSI Circuits and Systems
- Digital Integrated Circuits and VLSI Architectures
- Memory Circuits & Systems
- Multimedia Systems & Applications
- Digital Signal Processing Systems & Applications
- Circuits & Systems for Communications
- Processor, Embedded Systems & Software

- SoC Design Methodology
- HW-SW Co-design
- SoC Testing
- Design Verification
- Signal Integrity / Interconnect Modeling and Simulation

- Circuits and Systems for Emerging Technologies
- Sensory Circuits and Systems
- Biomedical Circuits and Systems
- Automotive Circuits and Systems
- IoT/IoE Circuits and Systems
- Nanoelectronics and Gigascale Circuits and Systems
- 3-D ICs and SoC Packages

From Incheon International Airport to Gyeongju
(1) Direct KTX (Korea Train Express) is available to Singyeongju Station.
(2) Selected shuttle bus service from Incheon International Airport to ISOCC.

Website : http://www.isocc.org
Contact : secretary@isocc.org

Monday ~ Tuesday, November 2~3, 2015

The Orange color boxes are invited papers.

Nov. 2 Monday		
Loby	Crystal	Jade
Registration	Tutorial 1-1	Tutorial 2-1
	Break	
	Tutorial 1-2	Tutorial 2-2

Time	
From	Till
9:00	9:15
9:15	9:30
9:30	9:45
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18:00	18:15
18:15	19:00
19:00	20:00

Nov. 3 (Tue) Tuesday										
Lobby	Convention A	Convention B & C	Sapphire	Geumgang	Diamond	Crystal	Jade	Emerald	Ruby
Registration	CDC Demo & Panel 1					CDC-1	CDC-2	CDC-3		
					Break					
					Opening Ceremony					
					Keynote-1					
					Keynote-2					
					Keynote-3					
					Lunch					
	CDC Demo & Panel 2		SoC1	394	ARM1	396	Digital1	404	SS1	378	SS2	068	13:30~
				372								122	
				121		075		078		338		165	
				159		178		143		381		392	
				247		234		156		371		395	
				251		275		221				397	System IC R&D Workshop (COSAR)
				295		380		298				399	
					Break								
			SoC2	230	ARM2	401	Digital2	272	SS3	387	SS4	304	
				106						386		334	
				192		016		402		377		388	
				194		067		409		382		391	
				284		074		049		374		393	
				296		097		198				405	
						240		273				406	
					Break								
					Banquet								

SoC1 Design Verification
SoC2 SoC Testing and HW-SW Codesign
ARM1 RF Circuits and Transceivers
ARM2 Analog Circuit Techniques
Digital1 Circuits and Systems for Communications
Digital2 Memory and Digital Circuits

CDC Chip Design Contest
SS# (Invinted Special Session)
SS1 Solutions for Mobile and Normally-off Computing Systems
SS2 SIC2015 Project - Vision/Multimedia SoC
SS3 Design, Analysis and Tools for Integrated Circuis and Systems(DATICS)
SS4 SIC2015 Project - Mobile/Automotive SoC

Anrtisu Session

RF Circuits and Transceivers

Nov. 3, 13:45~15:30 Geumgang

Chair: Kang-Yoon Lee (*Sungkyunkwan University, Korea*)

▶ *Invited Paper* RF Receiver Design for IOE Applications

Joung Won Park
Qualcomm Technology Inc., USA.

▶ A Low-Voltage PLL with a Current Mismatch Compensated Charge Pump

Sung-Geun Kim, Jinsoo Rhim, Dae-Hyun Kwon, Min-Hyeong Kim, and Woo-Young Choi
Yonsei University, Korea

▶ A 10 Gbps SerDes For Wireless Chip-to-chip Communication

Sangwoo Han[1], Taegyu Kim[1], Jintae Kim[2], and Jongsun Kim[1]
[1]*Hongik University, Korea*
[2]*Konkuk University, Korea*

▶ A design of META-VCO based-on meta-material using CMOS process

Jongsuk Lee and Yong Moon
Soongsil University, Korea

▶ A Low Power RF CMOS Direct-Conversion Transmitter Using High Conversion Gain Front end for IEEE 802.15.4 Standard

Changwon Seo[1,2], Hanjin Cho[1], Seyoung Baik[2] , Jinyong Kim[2] , Ho Jeong Jin[2], and Choon Sik Cho[2]
[1]*ETRI, Korea*
[2]*Korea Aerospace University, Korea*

▶ Design of a 40GHz PLL Frequency Synthesizer with Wide Locking Range ILFD in 65nm CMOS

Woongtae Nam, Jihoon Son, and Hyunchol Shin
Kwangwoon University,Korea

A Low-Voltage PLL with a Current Mismatch Compensated Charge Pump

Sung-Geun Kim, Jinsoo Rhim, Dae-Hyun Kwon, Min-Hyeong Kim, and Woo-Young Choi
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Seodaemun-gu, Seoul 120-749, Korea
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Abstract—**A low-voltage phase-locked loop (PLL) circuit having a charge pump (CP) with a novel negative feedback replica bias scheme for current mismatch compensation is demonstrated. A prototype 400-MHz PLL circuit operating at 0.65-V is fabricated with 180-nm standard CMOS process. Measurement results show that current mismatch compensation is successfully achieved. Our PLL consumes only 140-μW.**

Keywords-component;low voltage charge pump, phase locked loop, power efficiency, spur reduction

I. INTRODUCTION

Power consumption reduction is the key design consideration for modern integrated circuits. Lowering the supply voltage is the most effective way for achieving this goal and optimal design of mixed-signal circuits such as phase-locked loops (PLLs) operating at low supply voltages is attracting research interests [1]-[3].

With low supply voltages, transistors used for current sources become more sensitive to drain-to-source voltage (V_{DS}) variations. This can be a serious problem for the charge pump (CP) in PLL as it results in the reference spur due to CP current mismatch. Several design techniques for preventing this problem have been reported [2, 3]. In [2], dynamic-threshold CMOS is used to alleviate the voltage headroom problem but this requires special processing technology. An active loop-filter (ALF) with a single-ended two-stacked CP is used in [3], but this can suffer from inferior noise performance due to active devices in the loop-filter. Moreover, designing OP-amp used in ALF can be challenging for low supply-voltage applications.

In this paper, we present a low-voltage PLL with a novel structure for current mismatch compensating charge pump. Our PLL realized in 180-nm CMOS achieves 400-MHz operation at 0.65-V supply voltage with well-compensated CP current mismatch.

II. CIRCUIT IMPLEMENTATION

A. PLL Architecture

Fig. 1 shows the block diagram of our PLL. The CP has a two-transistor stacked gate-controlled structure and the phase-frequency detector (PFD) consists of conventional CMOS logic gates and D-flip flops (DFFs). The VCO has inverter based pseudo differential structure. The divide-by-16 frequency divider consists of an extended true-single-phase-clock (E-TSPC) DFF and three TSPC DFFs [4].

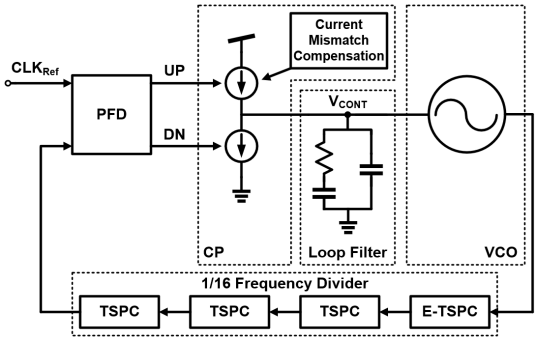

Figure 1. PLL block diagram.

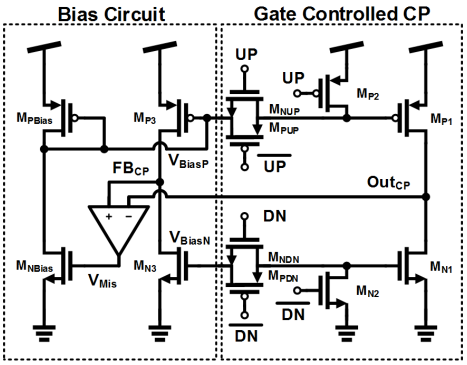

Figure 2. Two-stack gate-controlled CP with a bias circuit.

B. Charge Pump

The structure of our CP with a novel negative feedback replica bias circuit is shown in Fig. 2. The CP structure is based on two-stack gate-controlled CP for low supply-voltage operation [1]. The conventional replica bias circuit uses negative feedback by directly connecting OP-amp output to the switching node for current mismatch compensation [5]. However, this requires high slew-rate OP-amp for fast switching operating, which can consume a significant amount of power and optimal design of which can be challenging for low supply-voltage applications. In our CP, the negative feedback bias is divided into replica circuit and V_{BiasP} generator

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) [2015R1A2A2A01007772]. The authors are thankful to IC Design Education Center (IDEC) for EDA software and MPW support.

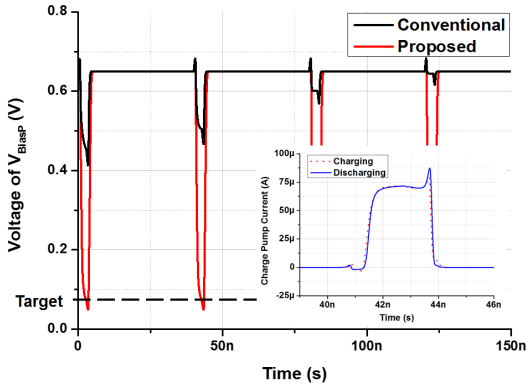

Figure 3. Transient simulation results of CP.

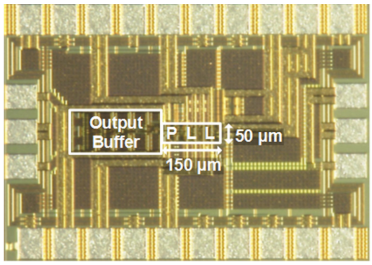

Figure 4. Microphotograph of fabricated PLL.

to avoid direct connection between OP-amp output and the switching node, V_{BiasP}. The output of OP-amp (V_{Mis}) controls the gate node of M_{NBias} and generates proper V_{BiasP}, which makes the voltage of FB_{CP} same as same as that of OUT_{CP}. The V_{BiasP} generator produces currents instead of OP-amp when switch signals come from PFD and, consequently, the burden of high slew-rate of OP-amp is eliminated.

Fig. 3 shows the transient simulation result for V_{BiasP} in 180-nm CMOS for the proposed and the conventional CPs. For simulation, PLL is locked and PFD delivers 3-ns wide pulses to CP. The same OP-amp having slew-rate of 0.124-V/µs and power consumption less than 0.2-µW is used for both types of CP simulation. V_{BiasP} in conventional CP cannot reach the target bias voltage due to the limited slew-rate of OP-amp while V_{BiasP} in our proposed CP does. Fig. 3 also shows charging and discharging currents produced by our CP. As can be seen in the figure, charging and discharging currents match very well.

III. Measurement Results

A prototype PLL circuit is fabricated in 180-nm standard CMOS technology. Fig. 4 shows the micro-photograph of the fabricated chip. The core chip area is 0.0075-mm^2, excluding output buffers. The fabricated chip is mounted and wire-bonded on FR4 printed-circuit board for measurement. The loop filter is implemented externally so that our PLL has bandwidth of 0.8-MHz. The PLL circuit consumes 140-µW for 400-MHz output at 0.65-V supply voltage.

Fig. 5 shows the measured phase noise and timing jitter of our PLL. The phase noise is -90.3-dBc/Hz at 1-MHz offset. The rms and peak-to- peak jitter at 400-MHz are 13.1-ps and

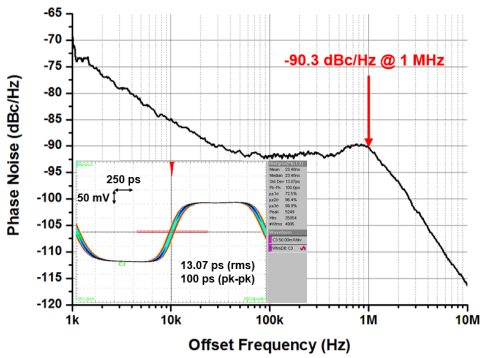

Figure 5. Measured phase noise and timing jitter of PLL.

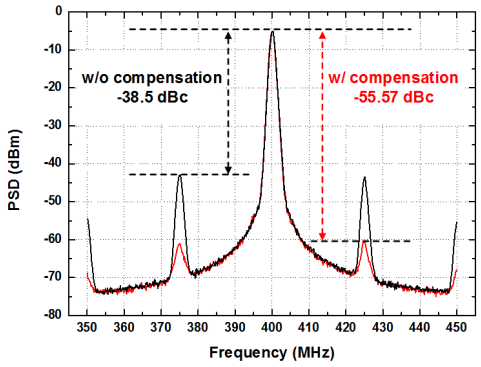

Figure 6. Measured output spectrum of PLL.

100-ps, respectively. Fig. 6 shows the measured output spectrum at 400-MHz output with and without CP mismatch compensation. The measured reference spur is -55.57-dBc with compensation and -38.5-dBc without compensation.

IV. Conclusion

A low-voltage PLL with a novel current mismatch compensated CP is demonstrated in 180-nm standard CMOS technology. The CP successfully compensates current mismatch and reduces PLL output spur by 17-dB. The entire PLL consumes 140-µW for 400-MHz output at 0.65-V supply voltage.

References

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