2014 IEEE 11th International Conference on Group IV Photonics

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The IEEE International Conference on Group IV Photonics (GFP) is one of the leading international conferences focused on Silicon Photonics and other group IV element based photonic materials and devices. The 10th IEEE International Conference on Group IV Photonics will be held at the Cite Internationale Universitaire de Paris in the beautiful city of Paris France from 27-29 August 2014. The conference is planned as a single track conference and will include both oral and poster sessions of contributed and invited papers comprising reviews on a number of important and timely topics. A post-deadline session will feature the most recent and exciting results. Technical results on group IV element photonic materials and devices, including integration and fabrication technologies are welcomed. The success of the GFP conference depends on a large extent on your contributions and active participation.

Conference Details

Dates	27 Aug - 29 Aug 2014
Location	Cite Internationale Universitaire de Paris 17, bd Jourdan Paris, France
Web site	www.gfp-ieee.org
Contact	Megan Figueroa IEEE Photonics Society 445 Hoes Lane Piscataway NJ USA 08854 732 562 3895 m.figueroa@ieee.org 732 562 8434 (fax)
Conference #	33188
Attendance	180
Publications	Download conference papers from IEEE*Xplore*

Please see the conference Web site for full details.

Call for Papers for Conference Authors

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Final submission deadline: 18 Mar 2014

Notification of acceptance date: 17 May 2013

Features

- Exhibits

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Final Program

Wednesday, 27 August 2014

All Sessions to be held in Space Adenauer

8:15 AM - 10:00 AM
Session WA: Welcome/Plenary Session
Session Chair: Laurent Vivien, University of Paris-Sud, France

8:15 AM - 8:30 AM **Introduction/Welcome**

WA1 8:30 AM - 9:15 AM (Plenary)

Revolutionizing Computing and Communications with Silicon Photonics, Mario Paniccia, *Intel Corporation, USA*

TBD

WA2 9:15 AM - 10:00 AM (Plenary)

Recent Progress on Silicon Photonics R & D and Manufacturing on 300mm Wafer Platform, Frederic Boeuf, *ST Microelectronics, France*

TBD

10:00 AM - 10:30 AM **AM Coffee Break/Exhibits- Salon Honnorat**

10:30 AM – 12:15 PM
Session WB: Silicon Modulators
Session Chair: Lars Zimmermann, IHP, Germany

WB1 10:30 AM - 11:00 AM (Invited)

An Efficient MOS-Capacitor based Silicon Modulator and CMOS Drivers for Optical Transmitters, M. Webster, P. Gothoskar, V. Patel, D. Piede, S. Anderson, R. Tummidi, D. Adams, C. Appel, P. Metz, S. Sunder, B. Dama and K. Shastri, *Cisco Systems, Inc., Allentown, USA*

We present an efficient MOS-capacitor based silicon modulator. In an MZI configuration, a 9dB extinction ratio at 28 Gbps is achieved from the 1V output of a low-power CMOS inverter driver IC.

WB2 11:00 AM - 11:15 AM

Evaluation of the Performances of a Silicon Optical Modulator Based on a Silicon-Oxide-Silicon Capacitor, A. Abraham, S. Olivier, *Cea, Leti, Grenoble, France*, D. Marris-Morini and L. Vivien, *Ief, Cnrs, Université Paris-Sud XI, Orsay, France*

We report results of a parametric study performed on a capacitive silicon modulator. The trade-off between modulation efficiency, optical losses and modulator speed was analysed.

WB3 11:15 AM - 11:30 AM

Low-aVpL 25-Gb/s Silicon Modulator Based on Forward-Biased Pin Diodes, T. Baba, S. Akiyama, and M. Imai, *Photonics Electronics Technology Research Association (PETRA) and Institute for Photonics-Electronics Convergence System Technology (PECST), Tsukuba, Japan,* T. Horikawa, *National Institute of Advanced Industrial Science and Technology (AIST) and Institute for Photonics-Electronics Convergence System Technology (PECST),* and T. Usuki, *Photonics Electronics Technology Research Association (PETRA) and Institute for Photonics-Electronics Convergence System Technology (PECST)*

We developed a 25–Gb/s silicon modulator with 9.83-dB•V aVpL, which is smallest of those operated at 25 Gb/s and higher. We used forward-biased diode operations, which enables small VpL with moderately doped low-loss waveguides.

WB4 11:30 AM - 11:45 AM

A Behavior Model for Silicon Micro-Ring Modulators and Transmitter Circuit-Level Simulation Using It, J. Rhim, Y. Ban, J. Lee, *Yonsei University, Seoul, Korea*, S. Cho, *Samsung Advanced Institute of Technology, Gyeonggi-do, Korea* and W. Choi, *Yonsei University, Seoul, Korea*

We implement and verify Si micro-ring modulator (MRM) behavioral model based on the dynamic coupled-mode theory. We also perform circuit-level simulation of the entire Si photonic transmitter including the driver electronics and the Si MRM.

WB5 11:45 AM - 12:00 PM

Peaking in Ring Modulators and Application to ISI Reduction, J. Witzens, J. Mueller, F. Merget, S. Sharif Azadeh, J. Hauck and S. Romero-Garcia*, Integrated Photonics Laboratory, RWTH Aachen University, Aachen, Germany*

A small signal analytical expression of peaking in the electro-optic response of ring modulators is derived which closely matches experimental results. E/O-bandwidths above 40 GHz are obtained. The peaking is used to open ISI-penalized eye diagrams with results reported at 32, 40 and 44 Gbps.

A Behavior Model for Silicon Micro-Ring Modulators and Transmitter Circuit-Level Simulation Using It

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Abstract: We implement and verify Si micro-ring modulator (MRM) behavioral model based on the dynamic coupled-mode theory. We also perform circuit-level simulation of the entire Si photonic transmitter including the driver electronics and the Si MRM.
Keywords: Micro-ring modulator, behavioral model, dynamic coupled-mode theory, circuit-level simulation

Optical interconnects are attracting lots of research interests as electrical interconnects are facing bandwidth, power, and footprint limitations [1]. Recently, electronic-photonic integrated circuits (EPICs) on Si platform have become possible and several fully-integrated EPIC transceivers have been reported [2-3]. For successful realization of such EPICs, the importance of accurate and easy-to-use simulation in the design stage cannot be overemphasized. Although there are many simulation tools that produce accurate results for photonics devices, they are often not compatible with standard Electronic Design Automation (EDA) tools that are routinely used in the semiconductor industry. Because of this, photonic devices and electronic circuits are often simulated separately, which is highly undesirable for design of large-scale EPICs. As one of solutions for this problem, we develop a behavioral model for a Si micro-ring modulator (MRM), which is extensively investigated as a key component for low-power, small-size, large-bandwidth optical interconnect applications [4] and demonstrate that the entire transmitter including driver electronics and the Si MRM can be simultaneously simulated on SPICE.

Fig. 1(a), (b), and (c) show the structure, microphotograph, and cross-sectional view of a Si MRM used in our investigation, respectively. The Si MRM is fabricated by IME through OpSIS [5]. Modulation is achieved by modulating the bias voltage of the reverse-biased PN junction. Using the dynamic coupled-mode theory, the characteristics of MRM can be described by the following equations [6]:

$$\frac{d}{dt}a = \left(j\omega_0 - \frac{1}{\tau}\right)a - j\mu E^i \text{ and } E^t = E^i - j\mu a, \tag{1}$$

where a is the energy amplitude stored inside the ring, E^t and E^i are the transmitted and incident wave E-field, respectively, ω_0 is the resonance angular frequency, $1/\tau$ is the rate of the decay for the energy amplitude inside the ring due to loss and coupling out, and μ is the mutual coupling coefficient between the ring and the bus waveguide. The above differential equation can be iteratively solved for given v_{in}, the modulator driving voltage, using the following equation:

$$a_{n+1} = (a_n - B_n \exp(j\omega t))\cdot \exp(\frac{j\omega - 1/\tau}{n_{eff}(v_{in})}\cdot \Delta t) + B_n \exp(j\omega(t+\Delta t)), \text{where } B_n = \frac{-jQ\sqrt{n_{eff}(v_{in})}}{j\omega(n_{eff}(v_{in})-1)+\frac{1}{\tau}}, \tag{2}$$

where n_{eff} is the effective group index and Δt is the time-step used for the simulation. Above equation can be implemented in Verilog-AMS, an analog extension of Verilog-HDL, which is widely used for IC design and fully compatible with such circuit simulators as SPICE and Spectre.

Fig. 2 (a), (b), and (c) show the measured and simulated transmission spectrum, small-signal frequency response, and transient responses of our MRM, respectively. Our simulation is done on SPICE, and MRM parameter values needed for simulation that are shown in fig. 2(a) are extracted from the measured MRM transmission spectrum. Measurements for A, B and C in Fig. 2(b) and (c) are done at the corresponding wavelengths indicated in Fig. 2(a). We can clearly observe the dependence of MRM small-signal frequency and large-signal transient responses on the wavelength, and agreement between simulation and measurement is fairly good.

The real advantage of our behavior model is that simulation of the entire transmitter including driver electronics and the Si MRM can be done on a single platform. Fig. 3 shows the simulated eye diagrams for the transmitter at different wavelengths. The driver is designed in 65-nm standard CMOS technology. The equivalent circuits for wire bonding and the electrical effects of the Si MRM are also included. The capability of simultaneous simulation of electronic circuits and photonic device should further enhance the potential of Si photonic devices and EPICs.

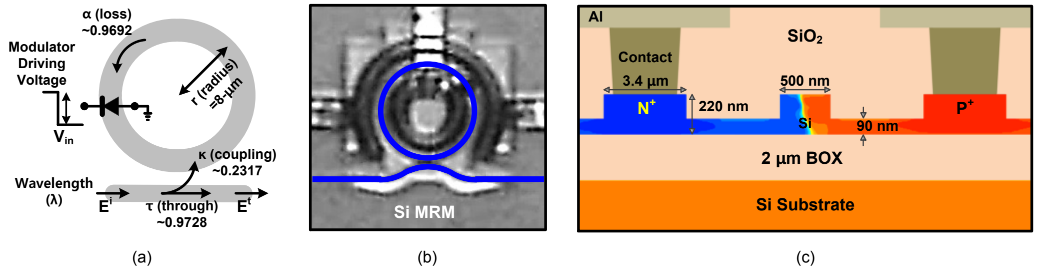

Fig. 1. Micro-ring modulator (a) structure (b) microphotograph (c) cross-sectional view

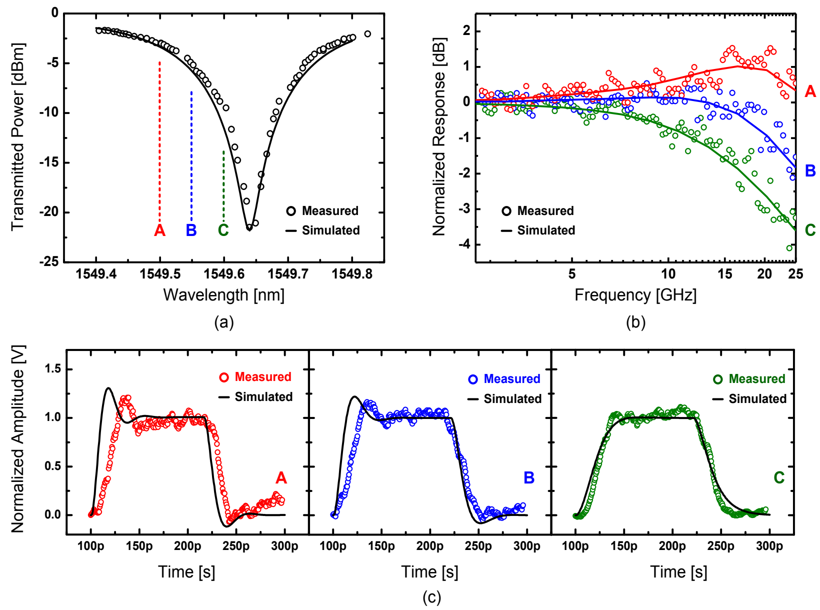

Fig. 2. Simulated and measured micro-ring modulator (a) transmission spectra (b) frequency response (c) transient response

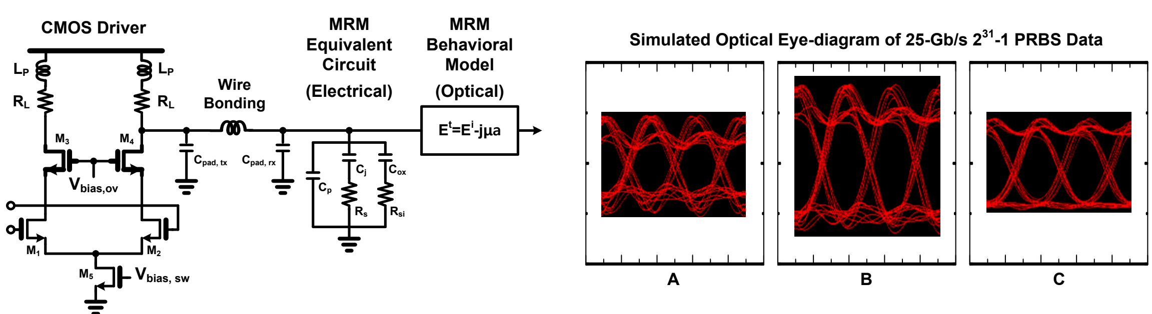

Fig. 3. Simulated eye diagrams of Si photonic transmitter at different wavelength

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