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M-01 **A Robust Parasitic-Insensitive Successive Approximation Capacitance-to-Digital Converter**, Hesham Omran, Muhammad Arsalan, Khaled N. Salama, King Abdullah University of Science and Technology (KAUST)

We present a capacitive sensor interface circuit using true capacitance-domain successive approximation that is independent of supply voltage. The interface circuit is insensitive to parasitic capacitances, offset voltages, and charge injection, and is not prone to noise coupling. The design achieves very low temperature sensitivity of 25ppm/oC and digitizes a wide capacitance range of 16pF with 12.5-bit resolution in a compact area of $0.07mm^2$.

M-02 **Configurable Incremental Sigma-Delta ADC for DC Measure and Audio Conversion**, Zhengyu Wang, Tay(Hui) Zheng, Dongtian Lu, Sasi Kumar, Xicheng Jiang, Broadcom Corporation

A configurable three-level sigma-delta ADC for both DC measurement and audio conversion is implemented. Dynamic Element Matching (DEM)is avoided. Three-level quantizer uses only one set of summer/comparator to save power and area. A simple formula accurately predicts DC measurement noise is presented. The ADC achieves 83dB SNR for audio, and 11-bit for DC measurements, at power of 0.5mW.

M-03 **A Hybrid SAR-VCO ΔΣ ADC with First-Order Noise Shaping**, A. Sanyal, K. Ragab, L. Chen, T. R. Viswanathan, S. Yan*, N. Sun, The University of Texas at Austin, *Silicon Labs

A scaling-friendly, hybrid, two-stage ADC with a 5-bit SAR as first stage and a VCO as second stage is presented in this work. Since the VCO can provide fine quantization for small signals in the time-domain, it is used to directly quantize the SAR residue without OTA-based residue amplification. Also, having a small input swing obviates the need for VCO non-linearity calibration. The VCO phase overflow problem is solved by using a counter to record the number of overflows, thus allowing a variable sampling rate. Since the VCO phase and counter are never reset, the VCO's first-order noise-shaping capability is retained. A prototype ADC in an 180 nm process achieves 73 dB SNDR over 2.2 MHz bandwidth and consumes 5mW from a 1.8V supply while sampling at 35 MHz.

M-04 **A 0.45mW 12b 12.5MS/s SAR ADC with Digital Calibration**, W. Li, T Wang*, J. A. Grilo**, G. C. Temes, Oregon State University, *Broadcom, **MaxLinear

This paper presents a 12-bit 12.5-MS/s SAR ADC in 40 nm technology. A power saving strategy is proposed. Also, several foreground calibration methods are proposed to reduce the power dissipation and enhance the conversion accuracy. Measurement results showed a SFDR of 87.5 dB and a THD improvement of 24.3 dB.

M-05 **A Voltage-Scalable 10-b Pipelined ADC with Current-Mode Amplifier**, Y. Suh*, S. Choi, B. Kim, H.-J. Park, J.-Y. Sim, Pohang University of Science and Technology (POSTECH), *Samsung Electronics

This paper presents an energy-efficient 10-b pipelined ADC with a current-mode

University, **VTT Technical Research Centre of Finland

This paper presents an ASIC implementation of a 32-bit RISC CPU in 28nm CMOS employing timing-error prevention with clock stretching. Measurements show 1.67pJ/cyc energy consumption at 400mV, which corresponds to 40% energy savings and 84% EDP reduction compared to operation based on static signoff timing.

M-17   **A Coprocessor for Clock-Mapping-Based Nearest Euclidean Distance Search with Feature Vector Dimension Adaptability**, Fengwei An, Toshinobu Akazawa, Shogo Yamazaki, Lei Chen, Hans Juergen Mattausch, Hiroshima University

A coprocessor fabricated in 180nm for word-parallel nearest-Euclidean-distance search is developed using a distance-clock-mapping concept. The test chip, for parallel search among 32 references achieves low power dissipation of 5.02 mW at 42.9MHz clock frequency and 1.8 V supply voltage. Applications with up to 2048-dimensional vectors can be handled.

M-18   **An Efficiency-Enhanced 2.4GHz Stacked CMOS Power Amplifier with Mode Switching Scheme for WLAN Applications**, Yun Yin, Baoyong Chi, Xiaobao Yu, Wen Jia*, Zhihua Wang, Tsinghua University, *Research Institute of Tsinghua University in Shenzhen

This work proposes an efficiency-enhanced CMOS PA with mode switching scheme for 2.4GHz WLAN applications, which not only improves the efficiency at high back-off power but also achieves the high output power by means of transistor stacking and self-biasing techniques, while needing the minimum area overhead for low-cost WLAN-enabled terminals.

M-19   **A Capacitive-Coupling Technique with Phase Noise and Phase Error Reduction for Multi-Phase Clock Generation**, Feng Zhao, Fa Foster Dai, Department of Electrical and Computer Eng., Auburn University

This paper presents a capacitive-coupling technique for multi-phase oscillators. The proposed capacitive coupling techniques can improve the phase noise performance while maintain good phase accuracy over wide frequency range for multi-phase oscillators. A prototype two-phase VCO is analyzed using injection-locking theory and implemented to demonstrate the effectiveness of the capacitive-coupling technique for low-power and low-noise multiple phase clock generation. The 4.3-5.3 GHz two-phase VCO prototype was implemented in a 130nm CMOS technology and achieved a measured phase noise of -120 to -124.04dBc /Hz @ 1MHz offset and a measured phase error of 0.23-0.91° across the 1GHz tuning range.

M-20   **A 127-140GHz Injection-locked Signal Source with 3.5mW Peak Output Power by Zero-phase Coupled Oscillator Network in 65nm CMOS**, Yang Shang, Hao Yu, Peng Li, Xiaojun Bi*, Minkyu Je*, Nanyang Technological University, *Institute of Microelectronics (A-STAR)

A high output-power and high-efficiency injection-locked millimeter-wave signal source is demonstrated by zero-phase coupled-oscillator-network in CMOS-65nm process. The proposed source has a compact core chip area of $0.13mm^2$, and it is measured with 3.5mW peak output power, 9.7% frequency-tuning-range centered at 133.5GHz, 2.4% power efficiency and $26.9mW/mm^2$ power density.

M-21   **A 0.4-V, 500-MHz, ultra-low-power phase-locked loop for near-threshold voltage operation**, Joung-Wook Moon, Sung-Geun Kim, Dae-Hyun Kwon, Woo-Young Choi, Yonsei University

We present a 500-MHz, ultra-low-power PLL realized with 0.4-V supply in 65-nm CMOS technology. Our PLL employs a new charge pump circuit structure that can greatly reduce up/down current mismatch and their variation with VCO control voltages. The PLL consumes only 127.8 µW, corresponding power efficiency of 0.256 mW/GHz.

M-22 **A 75mW 50Gbps SerDes Transmitter with Automatic Serializing Time Window Search in 65nm CMOS technology**, Ke Huang, Ziqiang Wang, Xuqiang Zheng, Chun Zhang, Zhihua Wang, Tsinghua University

This paper presents a 50Gbps SerDes transmitter with automatic serializing time window search. The serializing timing is guaranteed and circuits running at highest speed such as latches for retiming and clock tree buffers for delay matching are eliminated.The transmitter running at 50Gbps consumes only 75mW power under 1.2V.

M-23 **A Blind ADC-Based CDR with Digital Data Interpolation and Adaptive CTLE and DFE**, C. Ting, M. S. Jalali, A. Sheikholeslami, M. Kibune*, H. Tamura*, University of Toronto, *Fujitsu Laboratories Limited

This paper proposes replacing the analog phase interpolator in a phase-tracking ADC-based receiver with a digital data interpolator following the ADC. This allows for a blind ADC-based receiver that has a simpler adaptive DFE implementation. Our measurements from a 65nm CMOS testchip confirm 7Gb/s operation for a 17dB channel loss.

Tuesday Poster Session

Tuesday, September 16, 5:00 pm – 7:00 pm
Donner, Siskyou, Cascade Ballroom

T-01 **Linear Current-Controlled Oscillator for Analog to Digital Conversion**, K.R.Raghunandan, T.Lakshmi Viswanathan, T.R.Viswanathan, The University of Texas at Austin

Current-controlled oscillators (CCO) for A/D conversion need linear tuning-characteristics. A new CCO design in which the period of oscillation is defined by charging the timing capacitor to a reference voltage by the input current, is described. The sources of non-linearity in the tuning characteristics are identified and modeled and an analog technique of compensation is presented. The prototype circuit in 0.18um technology has 0.2% linearity from 0 - 100 degC for the frequencies upto 500 MHz.

T-02 **A Fully Integrated Translational Tracking Filter with >40dB Blocker Attenuation and >68dB Harmonic Rejection in 40nm for Digital TV Tuner Applications**, Kun-Da Chu, Ying-Tsang Lu, Chao-Wei Wang, Chih-Ming Hung, Meng-Chang Lee*, Shih-Chieh Yen, MediaTek Inc., *MStar Semiconductor Inc.

A fully integrated tunable high-Q translational tracking filter (TTF) implemented in a 40nm CMOS for Digital TV tuners is presented. Combining feed-forward cancellation and harmonic rejection in a nested translational filter matrix, >40dB blocker suppression and >68dB harmonic rejection are achieved without any calibration at low current of 25mA.

T-03 **An Area-efficient 12-bit 1.25MS/s Radix-value Self-estimated Non-binary ADC with Relaxed Requirements on Analog Components**, H. San, R. Sugawara, Masao Hotta,

A 0.4-V, 500-MHz, Ultra-Low-Power Phase-Locked Loop for Near-Threshold Voltage Operation

Joung-Wook Moon, Sung-Geun Kim, Dae-Hyun Kwon, *Student, IEEE,*
Woo-Young Choi, *Member, IEEE*

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Abstract — **We present a 500-MHz, ultra-low-power phase-locked loop (PLL) realized with the near-threshold supply voltage of 0.4 V in 65-nm CMOS technology. Our PLL employs a new charge pump (CP) circuit structure that can greatly reduce CP up/down current mismatch and their variation with voltage-controlled oscillator (VCO) control voltages. The PLL consumes only 127.8 μW, which corresponds to power efficiency of 0.256 mW/GHz.**

Index Terms — **Automatic frequency calibration (AFC), charge pump, current mismatch, current variation, near-threshold voltage (NTV), phase-locked loop (PLL), ultra-low power, ultra-low voltage (ULV).**

I. INTRODUCTION

The demand for enhanced energy efficiency is becoming more and more important for System-on-Chip (SoC) design. The most straight-forward way of reducing SoC power consumption is reducing supply voltages. However, this poses a great challenge for design of such mixed-signal circuits as phase-locked loops (PLLs) used for SoC clock generation since reduced voltage headroom does not allow many conventional circuit design techniques. Recently, several PLLs operating at 0.5-V supply voltage have been reported [1]-[3]. However, their power efficiencies defined as the power consumption per PLL output frequency are still larger than 1 mW/GHz, requiring further investigation into circuit techniques for reducing PLL power and/or increasing PLL output frequency. In this paper, we report near-threshold voltage (NTV) operation of a PLL realized in 65-nm CMOS technology. In particular, we present a novel Charge Pump (CP) structure which provides good up/down current matching characteristics as well as high output resistance so that CP currents do not change with voltage-controlled oscillator (VCO) control voltages. Moreover, we implement an Automatic Frequency Calibration (AFC) circuit which provides several VCO sub-bands spanning a wide output frequency range so that the target output frequency can be achieved even with Process, Voltage, and Temperature (PVT) variation. Each VCO sub-band is controlled with the body-bias so that the VCO gain (K_{VCO}) is small, resulting in improved phase noises
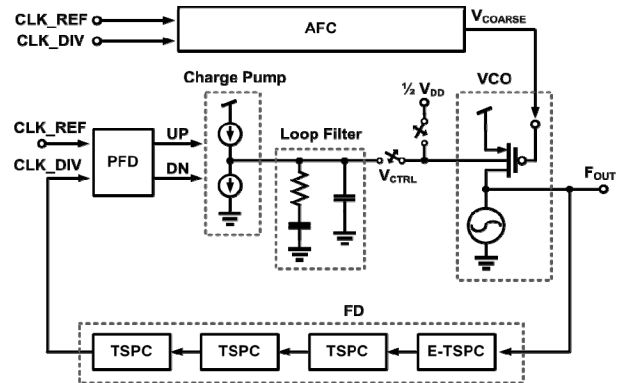

Fig. 1. Proposed PLL architecture.

characteristics. Our PLL successfully achieves 500-MHz operation with 0.4-V supply voltage with power consumption of 127.8 μW, which corresponds to power efficiency of 0.256 mW/GHz, the lowest value ever reported to the best of our knowledge.

II. PLL ARCHITECTURE

Fig. 1 shows our PLL architecture. It consists of a pass-gate type phase-frequency detector (PFD), a newly proposed CP and a second-order on-chip passive loop filter. An AFC circuit provides VCO coarse tuning voltage. The PLL has a divide-by-16 frequency divider (FD) consisting of combination of an extended true-single-phase clock DFF and three stages of true-single-phase clock DFFs for faster operating with low power consumption.

A. Charge Pump

NTV CP design is particularly challenging due to its limitation in using multiple-stacked transistors and pronounced non-ideal CP behaviors at NTV. CP up/down current mismatch increases the phase offset and reference spur level and their variation with VCO control voltages results in PLL bandwidth fluctuation. Although several single-ended CP structures that provide reduced current mismatch and variation have been reported [4]-[5], they
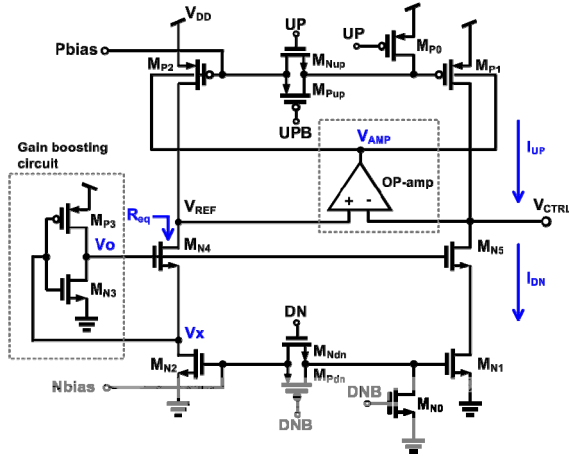
Fig. 2. Proposed CP architecture.

cannot operate with NTV supplies due to the voltage headroom limitation. Differential CP also has been reported [6] which can effectively eliminate CP current mismatch but they require multiple stacked transistors with additional compensating circuits for differential operation which consume a large amount of power. In [3], the dynamic-threshold CMOS is used to overcome the voltage headroom problem. However, this requires triple-well CMOS processes and further reduction in supply voltage is not easy. The CP reported in [7] employs a compensation technique for current mismatch operate with NTV supply but it still suffers from large current variation due to the low output impedance. These problems can be solved with a new CP structure shown in Fig. 2. It has a gate-switching structure so that the voltage headroom problem can be avoided. The OP-amp output controls the body bias of PMOS transistors, M_{P1} and M_{P2}, with a negative feedback. With this, V_{REF} follows V_{CP} and the charging current I_{UP} is always equal to the discharging current I_{DN}. Controlling the body-bias reduces OP-amp power consumption and relieves the high-slew rate burden. In order to reduce current variation of a CP, a gain-boosting technique is used to increase CP output resistance. An inverter is used as a gain amplifier, which detects V_X and regulates the gate voltages of M_{N4} and M_{N5} as shown in Fig. 2. With this, the current through M_{N4} remains constant, resulting in the large resistance for the drain of M_{N4} looked from the voltage node V_{REF}, which can be expressed as

$$R_{eq}\vert_{V_{REF}} = (g_{mN4}r_{ON4}r_{ON2}) \cdot ((g_{mP3} + g_{mN3}) \cdot (r_{OP3} \| r_{ON3})), \quad (1)$$

where g_{mN4}, g_{mP3}, and g_{mN3} are the trans-conductance of transistor M_{N4}, M_{P3}, and M_{N3}, respectively, and r_{ON4}, r_{ON2}, r_{OP3}, and r_{ON3} are the output resistance of M_{N4}, M_{N2}, M_{P3}, and M_{N3}, respectively. This technique provides the same resistance as a triple-cascode transistor but without
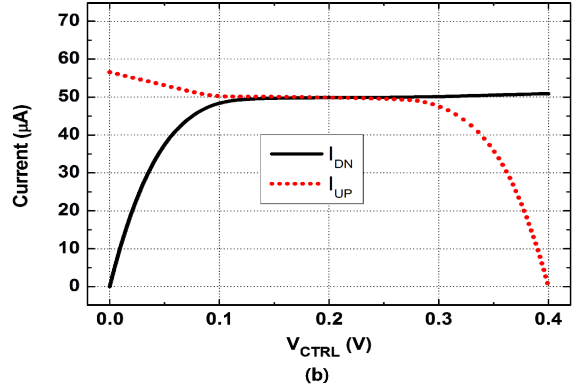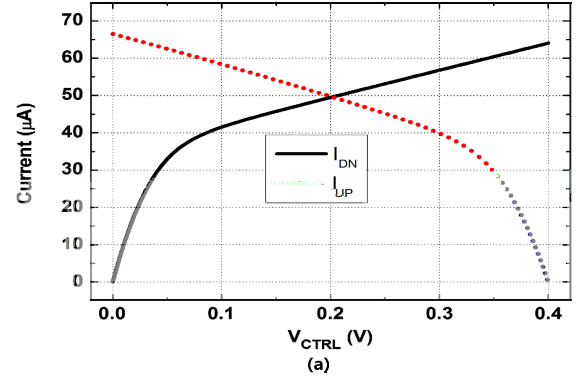

Fig. 3. Simulated CP currents (a) without compensation and (b) with compensation at 0.4-V supply.

sacrificing any voltage headroom. The compensated gate voltage of M_{N4} is copied to the gate voltage of M_{N5}, which controls the discharging current I_{DN} in the same manner. Fig. 3 (a) shows the simulation results of CPs without any compensation [2] and (b) with the proposed compensation technique for target current of 50 µA with 0.4-V supply in 65nm CMOS. It clearly shows the compensation greatly reduces CP current mismatch and its variation over a wide range of control voltages.

B. Voltage Controlled Oscillator and Automatic Frequency Calibrator

Our VCO is based on ring oscillators. Although an LC-VCO provides high noise rejection, it requires a much larger chip area limiting its applicability. Two challenges in designing a ring-based VCO with NTV supplies are limitation in using multiple-stacked transistors, which restricts the VCO output frequency range, and the frequency dependence on PVT variation. Since PVT variation has a direct impact on the oscillation frequency, the VCO should provide a wide tuning range, resulting in large K_{VCO}. We solved these problems by designing the VCO with body-bias technique and adding an AFC circuit. A pseudo-differential multi-band VCO shown in Fig. 4(a) is employed in our design. The delay cell consists of two
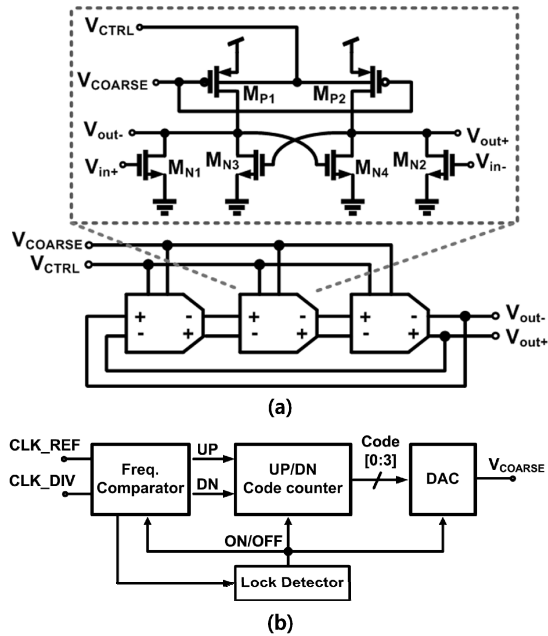
Fig. 4.   (a) VCO and (b) AFC circuit.
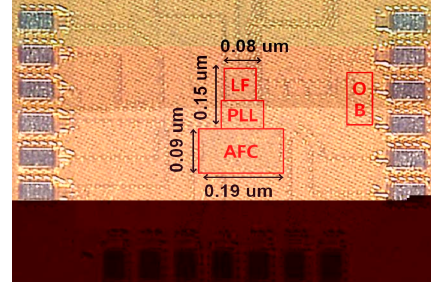

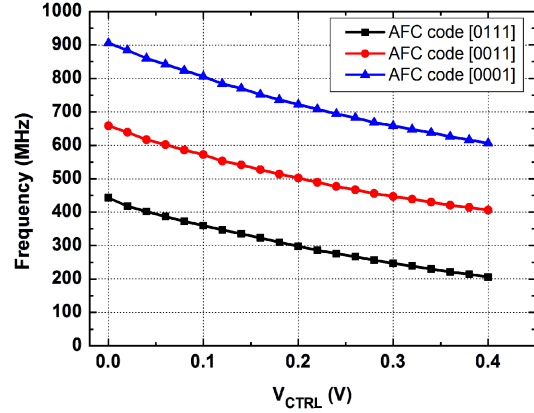Fig. 5.   Microphotograph of the PLL.

Fig. 6.   Measured VCO frequencies for sub-bands selected with different AFC codes [0001], [0011], and [0111].
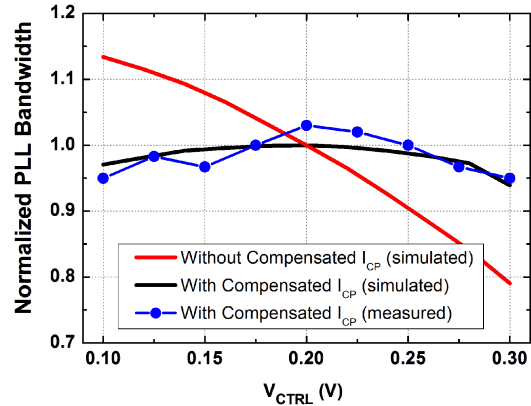

Fig. 7.   Measured and simulated PLL loop bandwidth for different VCO control voltages.

inverters with the cross-coupled pair [2]. The coarse tuning is achieved by adjusting the gate voltage of PMOS transistors M_{P1}, and M_{P2}. The gate voltage, V_{COARSE}, is provided from digitally controlled AFC to selecting an appropriate VCO sub-band. A tunable PMOS body bias, V_{CTRL}, from the CP is used for fine tuning the VCO frequency.

Fig. 4(b) shows the structure of our AFC circuit, which consists of a frequency comparator, UP/DN code counter and a digital to analog converter (DAC) and a lock detector. Initially, the PLL loop is open and V_{CTRL} is connected to the half of the supply. Then, the AFC circuit compares two input signals, CLK_REF and CLK_DIV, and generates either UP or DN signals. With these, the UP/DN code counter generates a 4-bit code, which after going through a DAC, coarsely sets the VCO frequency, selecting a desired VCO sub-band. Then, the lock detector makes the counter to stop counting and save the code. After that, the PLL automatically reconnects V_{CTRL} to the PLL loop and begins its phase locking process. The digital circuits for the AFC building block are all custom designed and laid out for 0.4V operation.

III. MEASUREMENT RESULTS

Our PLL is fabricated in 65-nm standard CMOS technology and mounted on FR4 board for measurement. 31.25-MHz reference frequency is provided by a signal generator for measurement. Fig. 5 shows a die micro-photograph. The total area is about 0.0285 mm² excluding

the output buffer. Fig. 6 shows the measured VCO frequencies for three different VCO sub-bands. For this measurement, forced the AFC codes and external voltage is supplied to the VCO input. As can be seen in the figure, our VCO provides small and constant gain for a wide frequency range. In order to verify that our CP currents do not change much with VCO control voltages, the PLL reference frequency is changed from 26.875 MHz to 37.5 MHz with corresponding PLL output frequency from
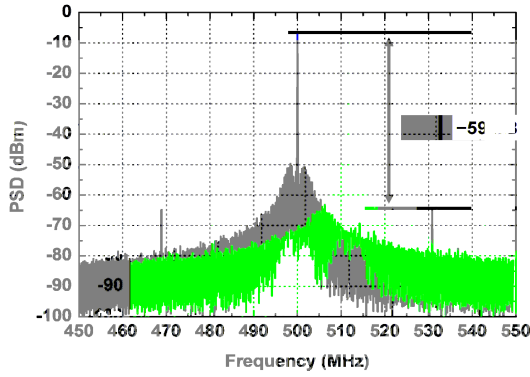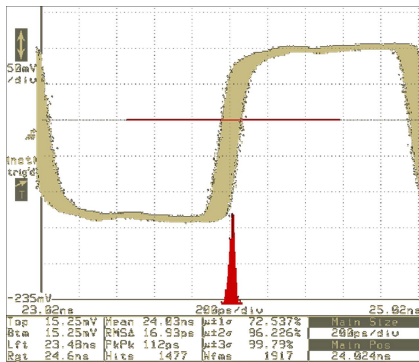
Fig. 8.   Measured output spectrum at 500 MHz.

Fig. 9.   Measured 500 MHz PLL output in time domain.

TABLE I
PERFORMANCE SUMMARY

Performance Parameter	Ref.[1]	Ref.[2]	Ref.[3]	This Work
Technology (CMOS)	130 nm	90nm	130nm	65nm
Supply Voltage (V)	0.5	0.5	0.5	0.4
VCO type	Ring	Ring	Ring	Ring
Power (mW)	1.25	0.4	0.44*	0.13
Output freq. (GHz)	0.55	0.4	0.4-0.433	0.5
Ref. Spur (dBC)	N/A	-40.28	-38.3	-59
RMS Jitter (PS)	8.01	9.62	5.5	16.9
Phase Noise @1MHz (dBC/Hz)	-95	-87	-91.5	-94
Power Efficiency (mW/GHz)	2.27	1	1.01	0.256

*: Including pulse-swallow counter.

430 MHz to 600 MHz. This causes the change of V_{CTRL} within in the same VCO sub-band. Then PLL loop bandwidth, which is directly influenced by the CP current, is measured. Fig. 7 shows the measurement results as well as the simulated results for a PLL without any CP compensation. The results clearly show that our PLL has very small CP current variation for a wide tuning range.

Fig. 8 shows measured PLL output spectrum. The spur an offset frequency of 31.25 MHz is −59 dB below the carrier frequency. The measured PLL phase noise is −94 dBc at 1-MHz offset for 500-MHz output frequency. Fig. 9 shows the measured jitter characteristics also at 500 MHz. The RMS jitter is 16.9 ps corresponding to 0.0084 unit interval. The PLL consumes 127.8 μW excluding the output buffer, resulting in power efficiency of 0.256 mW/GHz. Table I summarizes the performance of our PLL and compares it with other ULV PLLs.

IV. CONCLUSION

A 0.4 V of NTV PLL is demonstrated in standard 65-nm CMOS technology. The newly proposed CP in our PLL successfully reduces CP current mismatch and variation. The automatically calibrated VCO with a body-bias technique can provide small VCO gain for a wide range of output frequency. At the target output frequency of 500 MHz, our PLL also achieves power efficiency of 0.256 mW/GHz.

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