



2013 International SoC Design Conference

Conference Information

Papers

Sponsors

Sponsored by



<http://www.isocc.org>

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For other copying, reprint or republication permission, write to IEEE Copyrights Manager, IEEE Operations Center, 445 Hoes Lane, Piscataway, NJ 08854. All rights reserved. Copyright ©2013 by IEEE.

2013 International SoC Design Conference

CDC Panel Session 1

09:00~ 13:00 Lobby

Chair: Kyoung Rok Cho (Chungbuk National University, Korea)
Kwang Hyun Baek (Chung-Ang University, Korea)

- CDC(P)-001 A High-Efficiency PWM DC-DC Buck Converter Based on Multi-Phase Switching for Mobile Applications**
Tai-Ji An, Hyun-Sun Shim and Seung-Hoon Lee
Sogang University, Korea 1
- CDC(P)-002 All-Digital Hybrid Temperature Sensor Network for Dense Thermal Monitoring**
Seungwook Paek, Wongyu Shin, Jaeyoung Lee, Hyo-Eun Kim, Jun-Seok Park and Lee-Sup Kim
Korea Advanced Institute of Science and Technology(KAIST), Korea 2
- CDC(P)-003 A Boost Converter with Variation Tolerant MPPT Technique for Thermoelectric Energy Harvesting**
Jungmoon Kim, Minseob Shim, Junwon Jung, Heejun Kim and Chulwoo Kim
Korea University, Korea 3
- CDC(P)-004 A 12.5-Gb/s Optical Modulator Driver in 65-nm CMOS Technology**
Jinsoo Rhim and Woo-Young Choi
Yonsei University, Korea 4
- CDC(P)-005 Design of an Electrical Module for a Bio-Inspired Auditory Sensor**
Jeong Hoan Park, Jin Ho Kim, Mingyu Kang, Yoon-Kyu Song and Sung June Kim
Seoul National University, Korea 5
- CDC(P)-006 A 12b 100MS/s Three-Step Hybrid Pipeline ADC Based on Time-Interleaved SAR and Flash ADCs**
Jun-Sang Park, Woo-Jin Jang, Han-Gyeol Kim and Seung-Hoon Lee
Sogang University, Korea 6
- CDC(P)-007 Low-Power Clock- and Data-Recovery Circuit Using Analog Majority Voter**
Kang-Sub Kwak, Jong-Hyeon Ra and Oh-Kyong Kwon
Hanyang University, Korea 7
- CDC(P)-008 Dual Mode Rectifier for Piezoelectrif Energy Harvesting**
Minseob Shim, Jungmoon Kim, Junwon Jung, Heejun Kim and Chulwoo Kim
Korea University, Korea 8
- CDC(P)-009 A Digitally Modulated CMOS Power Amplifier With a 102-dB Power Dynamic Range for a RF Polar Transmitter**
Hyunseok Choi, Yumi Lee and Songcheol Hong
Korea Advanced Institute of Science and Technology(KAIST), Korea 9
- CDC(P)-010 On-Chip Temperature Sensor with Curvature Compensation using Injection Locked Oscillator (ILO)**
Wongyu Shin and Lee-Sup Kim

A 12.5-Gb/s Optical Modulator Driver in 65-nm CMOS Technology

Jinsoo Rhim and Woo-Young Choi

Department of Electrical and Electronic Engineering, Yonsei University
Seodaemun-gu, Seoul 120-749, Korea
wchoi@yonsei.ac.kr

I. INTRODUCTION

Convergence of electrical and optical interconnects is actively pursued as the needs for high-speed and high-capacity data transmission continuously increase. Integrating electrical circuits with optical components has become feasible by adopting silicon (Si) platform for photonic components [1-2]. Many research efforts are needed for developing high-speed interface circuits for Si photonics in CMOS technology. This paper presents a 12.5-Gb/s optical modulator driver circuit having 12-GHz of bandwidth with 2-V of output voltage.

II. DESCRIPTION

Fig. 1 describes the driver circuit. It is based on Current-Mode Logic (CML), which is suitable for high-speed operation. The main-driver uses 4-V supply voltage and the pre-driver uses 1-V supply voltage. In order to avoid device breakdown with 4-V supply voltage, thick-gate transistors (M3-4) are used in a cascode stage in the driver. The driver has 50- Ω termination for measurement and shunt inductors (400-pH) for bandwidth enhancement. The replica bias circuit is also integrated for amplitude calibration as well as overdrive-voltage regulation.

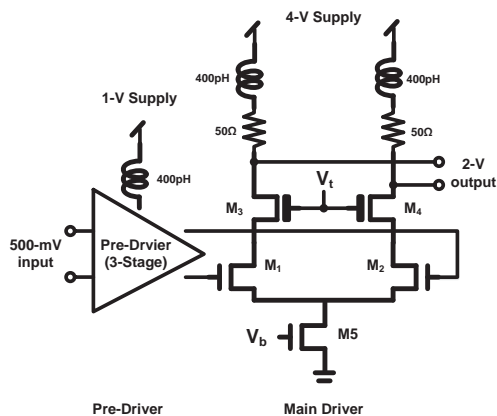


Fig 1. Modulator driver circuit

III. CHIP IMPLEMENTATION AND RESULTS

Fig. 2 shows microphotograph of our fabricated chip using 65-nm CMOS technology. Our driver circuit occupies 400- μm x 280- μm of area (100- μm x 70- μm for bias circuit) and consumes 200-mW, 40-mW with 1-V and 160mW with 4-V

supply voltages, respectively. Figure 3 shows the measured frequency response of our driver. The inset shows the measured eye-diagram for 12.5-Gb/s PRBS 2^{31} -1 data.

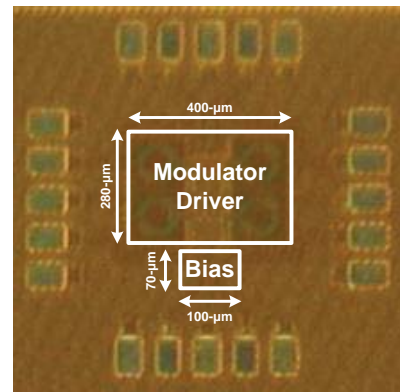


Fig 2. Micro-photograph of fabricated chip

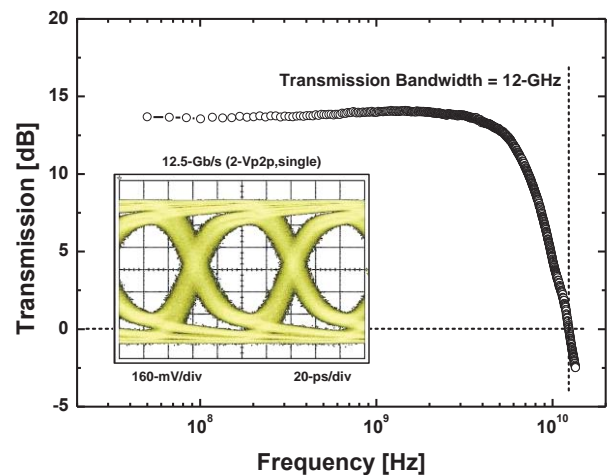


Fig 3. Measured frequency response of modulator driver. Inset shows eye-diagram of transmitted data (12.5-Gb/s)

REFERENCE

- [1] J. F. Buckwalter, X. Zheng, G. Li, et al, "A Monolithic 25-Gb/s Transceiver With Photonic Ring Modulators and Ge Detectors in a 130-nm CMOS SOI Process," *IEEE Journal of Solid-State Circuits*, Vol. 47, No. 6, June 2012, pp.1309-1322.
- [2] J.Kim, J. Buckwalter, "A 40-Gb/s Optical Transceiver Front-End in 45-nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 47, No. 3, March 2012, pp.615-626

This work [2012R1A2A1A01009233] was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST). The authors are very thankful to IC Design Education Center (IDEC) for EDA support as well as chip fabrication