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CDC Panel Session 1

09:00~13:00 Lobby
Chair: Kyoung Rok Cho (Chungbuk National University, Korea)
Kwang Hyun Baek (Chung-Ang University, Korea)

A 12.5-Gb/s Optical Modulator Driver in 65-nm CMOS Technology

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I. INTRODUCTION

Convergence of electrical and optical interconnects is actively pursued as the needs for high-speed and high-capacity data transmission continuously increase. Integrating electrical circuits with optical components has become feasible by adopting silicon (Si) platform for photonic components [1-2]. Many research efforts are needed for developing high-speed interface circuits for Si photonics in CMOS technology. This paper presents a 12.5-Gb/s optical modulator driver circuit having 12-GHz of bandwidth with 2-V of output voltage.

II. DESCRIPTION

Fig. 1 describes the driver circuit. It is based on Current-Mode Logic (CML), which is suitable for high-speed operation. The main-driver uses 4-V supply voltage and the pre-driver uses 1-V supply voltage. In order to avoid device breakdown with 4-V supply voltage, thick-gate transistors (M3-4) are used in a cascode stage in the driver. The driver has 50-Ω termination for measurement and shunt inductors (400-pH) for bandwidth enhancement. The replica bias circuit is also integrated for amplitude calibration as well as overdrive-voltage regulation.

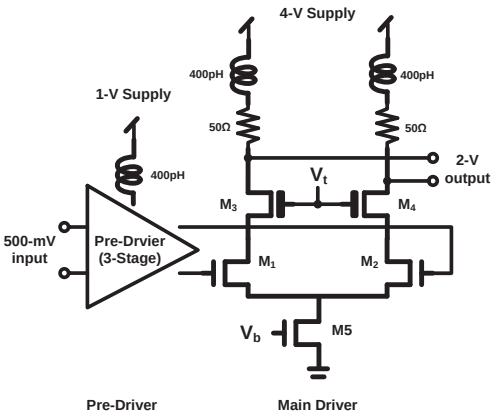

Fig 1. Modulator driver circuit

III. CHIP IMPLEMENTAION AND RESULTS

Fig. 2 shows microphotograph our fabricated chip using 65-nm CMOS technology. Our driver circuit occupies 400-μm x 280-μm of area (100-μm x 70-μm for bias circuit) and consumes 200-mW, 40-mW with 1-V and 160mW with 4-V supply voltages, respectively. Figure 3 shows the measured frequency response of our driver. The inset shows the measured eye-diagram for 12.5-Gb/s PRBS 2^{31}-1 data.

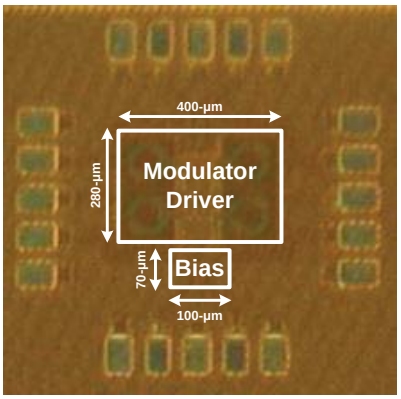

Fig 2. Micro-photograph of fabricated chip

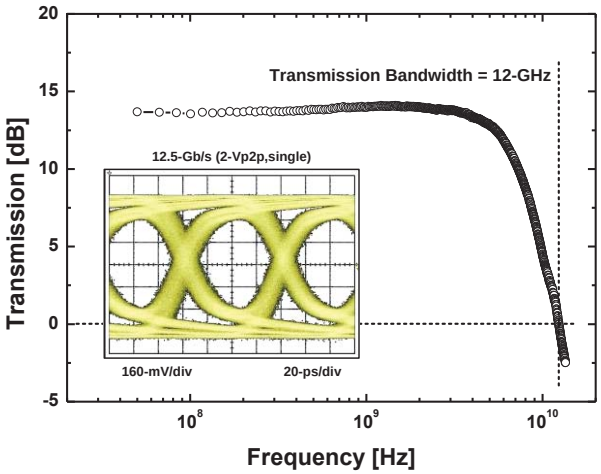

Fig 3. Measured frequency response of modulator driver. Inset shows eye-diagram of transmitted data (12.5-Gb/s)

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REFERENCE

[1] J. F. Buckwalter, X. Zheng, G. Li, et al, "A Monolithic 25-Gb/s Transceiver With Photonic Ring Modulators and Ge Detectors in a 130-nm CMOS SOI Process," *IEEE Journal of Solid-State Circuits*, Vol. 47, No. 6, June 2012, pp.1309-1322.

[2] J.Kim, J. Buckwalter, "A 40-Gb/s Optical Transceiver Front-End in 45-nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, Vol. 47, No. 3, March 2012, pp.615-626