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Conference Information

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[1] *Kwangwoon University, Korea*
[2] *Silicon R&D, Korea*
[3] *Ewha Womans University, Korea* 116

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[1] *Asian Institute of Technology, Thailand.*
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A Spur free 0.4-V 88-µW 200-MHz Phase-Locked Loop

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Abstract

An ultra-low voltage phase-locked loop (PLL) is demonstrated in standard 130-nm CMOS technology. The PLL employs a novel low-voltage charge-pump circuit which compensates current and leakage mismatches that result in suppressed reference spurs. Its voltage-controlled oscillator is realized with supply-regulated active-loop filter. Our PLL occupies 0.014 mm^2 and consumes 88 µW at 0.4-V supply for 200-MHz operation.

Keywords-component; low voltage charge pump, phase locked loop, power efficiency, spur reduction, ultra low voltage

I. Introduction

There are increasing demands for ICs with reduced power consumption as well as enhanced power efficiency. One method of reducing power consumption is lowering supply voltages. ITRS predicts that the operating supply voltage will be reduced to 0.43 V by 2026 [1]. However, designing analog and mixed-mode ICs with reduced supply voltages is a great challenge for many designers.

Since a PLL is one of the most important blocks for many wireline and wireless applications, realizing PLL circuits that can operate at ultra-low voltage (ULV) supplies is an important research topic. Although there have been many attempts to realize PLLs with ULV supplies [2-5], so far 0.5 V is the lowest supply voltage achieved for PLL. Further reduction is not easy due to the multi-stacked charge pump and the VCO voltage headroom.

In this paper, we propose novel solutions for above limitations and achieve 200 MHz PLL operating at 0.4 V. In addition, our PLL has much reduced reference spur. In Section II of this paper, the overall PLL architecture is described and details of each building block are given. Section III presents the measurement results, and conclusions is given in Section IV.

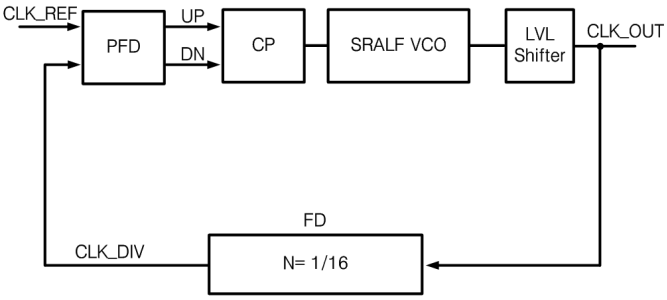


Fig. 1. Proposed PLL architecture.

II. PLL Architecture

Fig. 1 shows overall PLL architecture. It consists of a conventional DFF-based phase-frequency detector (PFD), a low-voltage charge pump (CP) and a supply-regulated active-loop filter VCO (SRALF VCO) [6]. SRALF VCO generates supply-variable output signal, which are processed for fixed clock output by a level shifter (LVL Shifter). The 1/16 frequency division (FD) is realized with two different types of dividers, 1/2 division with E-TSPC [7] which can operate faster, and 1/8 division with 2 stages of TSPC [8] which consumes less power.

A. Charge Pump

CP design with an ULV supply is especially challenging due to limitation in using multiple stacked transistors and non-ideal behaviors [9]. CMOS CPs usually have PMOS and NMOS switches which cannot produce perfect current matching characteristics due to output impedance mismatches. Moreover, as CMOS technology scales down, gate oxide thickness and the threshold voltages are also reduced, but undesirable leakage current is increased [10].

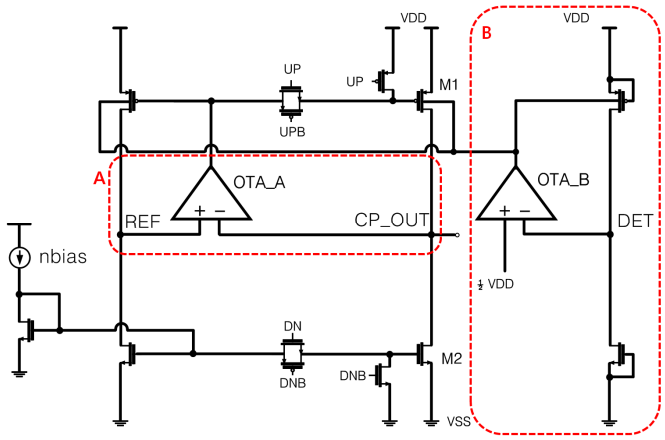


Fig. 2. Proposed charge pump circuit.

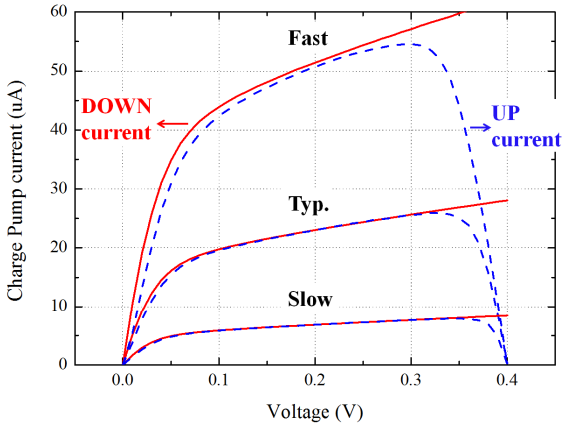
As a result, UP and DOWN current mismatch and leakage current cause substantial increase in PLL static phase offset and reference spurs. Several mismatch-free CPs have been reported [11, 12], but these cannot operate with ULV supplies. In [4], a modified gate-switching structure with 2-stacked transistors was used. Although this works well with ULV supply, it is vulnerable to the current mismatch problem. In [5], the DTCMOS structure was used to overcome the voltage headroom problem. However, this 4-stacked structure requires triple-well process. In order to solve these problems, we proposed a novel gate-switching CP which can compensate mismatch and leakage current.

Fig. 2 shows the proposed CP circuit. In Block A, with OTA_A, V_{REF} at REF node follows V_{CP_OUT} at CP_OUT node. In Block B, a feedback loop is implemented, which detects the off-path voltage V_{DET} at DET node and compensates the body-bias voltage of PMOS transistors. In this way, the charging and discharging transistor, M1 and M2, have same leakage current and V_{CP_OUT} is free from the difference in leakage current.

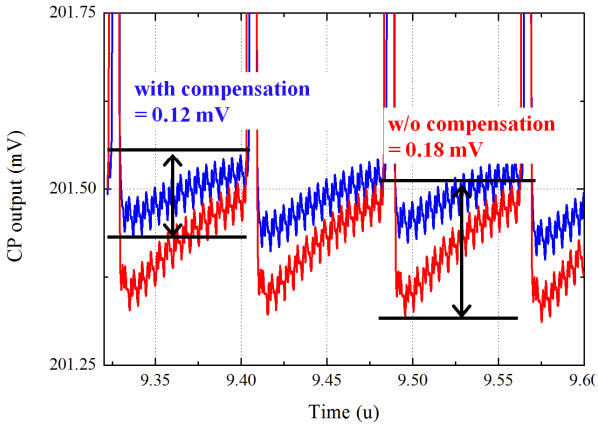
Fig. 3 shows the post-layout simulation results of our CP. Fig. 3(a) shows mismatch currents for different process corners. UP and DOWN currents are equal as long as the OTA maintains sufficient gain. Fig. 3(b) shows CP output variation after the PLL is locked. Output voltage variation due to the leakage current is reduced about 66 % with the compensation technique.

B. Supply-Regulated Active-Loop-Filter VCO

Inverter type full-swing delay cells can provide VCOs with lower-power consumption than fully differential delay cells. However, full-swing VCOs are very vulnerable to supply noises and, consequently, require good supply regulators. Moreover, because ULV CP provides a narrow control voltage range, the VCO output frequency is restricted to a narrow range. As a solution, we adopt a supply–regulated active-loop-filter VCO (SRALF VCO) [6]. With this, VCO circuit can be immune to supply noises and completely isolated from CP output and VCO



(a)



(b)

Fig. 3. Charge pump simulation result. (a) UP and DOWN current for different process corners, (b) Output variation with and without leakage compensation.

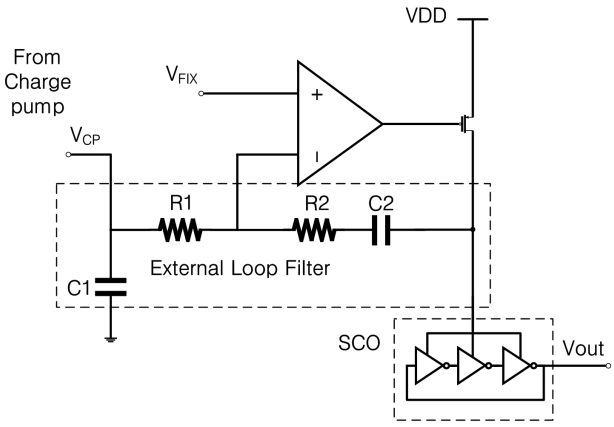


Fig. 4. SRALF VCO circuit.

input control voltages. Fig. 4 shows our SRALF VCO circuit having 3-stages of inverter-type SCO. The external loop filter is used in our implementation that allows loop filter optimization after the chip is fabricated.

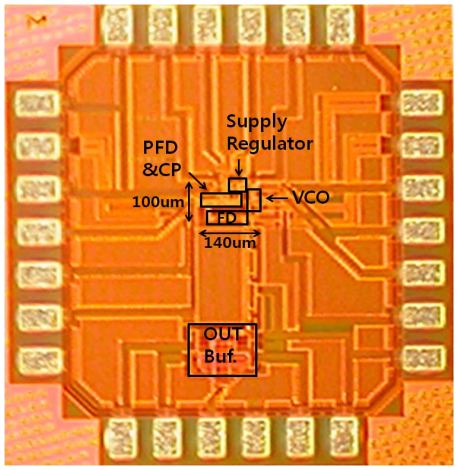


Fig. 5. Microphotograph of the proposed PLL.

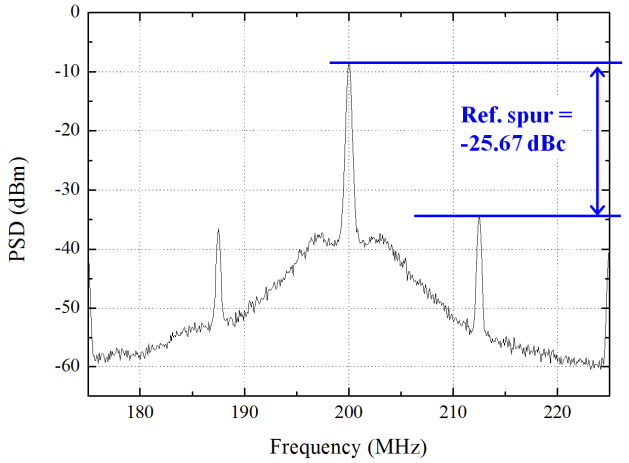


Fig. 6. Measured output specta: (a) without CP compensation, (b) with automatic CP compensation.

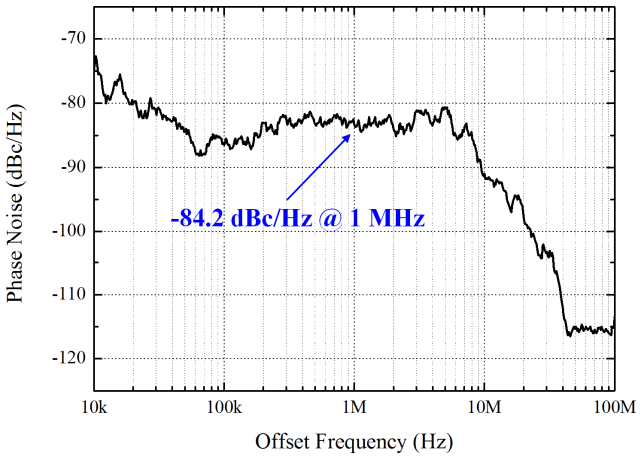


Fig. 7. Phase noise of the proposed PLL at 200 MHz.

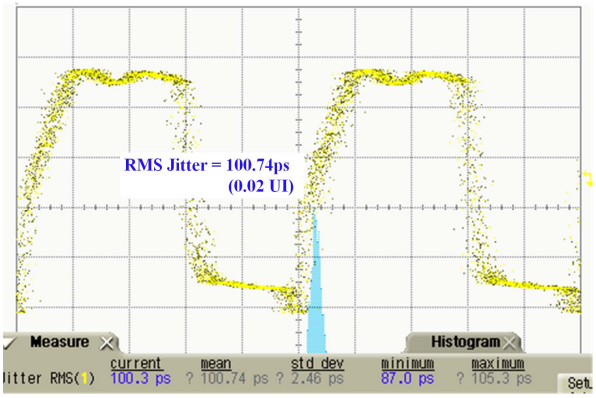


Fig. 8. Jitter histogram at 200 MHz with 0.4 V supply.

III. Measurement Result

A prototype PLL is fabricated with 130-nm standard CMOS technology and mounted on FR4 board for measurement. 12.5 MHz reference frequency is applied by a signal generator, and the PLL output is measured by an oscilloscope and a spectrum analyzer. Fig. 5 shows a die microphotograph. The core area is about 0.014 mm2 excluding the off-chip loop filter. Fig. 6 shows the measured PLL output spectra: (a) without CP compensation and (b) with automatic CP compensation. For both figures, the center frequency is 200 MHz with 50 MHz span. The reference spur is -25.67 dBc for (a) and -44.3 dBc for (b). This clearly shows that our CP mismatch and leakage current compensation technique successfully works.

Fig. 7 shows the measured phase noise of our PLL with 0.4-V supply voltage. It is -84.2 dBc/Hz at 1-MHz offset. Fig. 8 shows the measured jitter characteristics with 0.4-V supply voltage. The RMS jitter is 100.74 ps (0.02 UI). This poor jitter performance is

mainly due to the low-power SCO which has large gain of 4 GHz/V. OTAs consume 20-μW and the rest of the PLL 68-μW excluding the output buffer. This corresponds to 0.44 mW/GHz, which is the lowest among ULV PLLs reported so far.

IV. Conclusion

We demonstrate 200 MHz PLL operating with 0.4 V supply voltage in standard 130-nm CMOS technology. The charge pump in our PLL effectively reduces UP/DOWN current and leakage current mismatches, resulting in significantly reduced reference spur. It also has a SRALF VCO, which overcomes the narrow CP control voltage range and provides immunity to supply noises. This ULV PLL consumes only 88 μW and achieves record-low power efficiency.

Acknowledgment

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