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CDC Demo Session

09:00~17:00 Lobby
Chair: Kwang Hyun Baek (Chung-Ang University, Korea)
Kyoung Rok Cho (Chungbuk National University, Korea)

A 0.4-V 88-µW 200-MHz PLL with Reduced Reference Spurs.

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I. INTRODUCTION

There are increasing demands for ICs with reduced power consumption as well as enhanced power efficiency. One method of reducing power consumption is lowering supply voltages. For this reason, there have been many attempts to realize PLLs with Ultra-Low Voltage (ULV) supplies [1]. However, reducing supply voltages less than 0.5 V is not easy due to the multi-stacked charge pump and voltage headroom. We present a 200 MHz PLL operating at 0.4 V with reduced reference spurs.

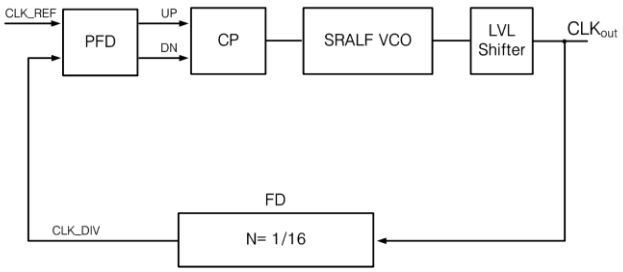

Fig. 1. Proposed PLL architecture

II. DESCRIPTION

Fig. 1 shows overall PLL architecture. It consists of a conventional DFF-based phase-frequency detector (PFD), a low-voltage charge pump (CP) and a supply-regulated active-loop filter VCO (SRALF VCO) [2]. The 1/16 frequency division (FD) is realized with an ETSPC and 3 stages of TSPC dividers. Fig. 2 shows the proposed CP circuit. In Block A, with OTA_A, V_{REF} at REF node follows V_{CP_OUT} at CP_OUT node. In Block B, a feedback loop detects the off-path voltage V_{DET} at DET node and compensates the body-bias voltage of PMOS transistors. In this way, CP circuit compensates charging/ discharging current and leakage current mismatches, which induce PLL reference spurs.

III. CHIP IMPLEMENTAION AND MEASUREMENT RESULTS

Fig. 3 shows the measured PLL output spectra with and without CP compensation. The center frequency is 200 MHz with 50 MHz span. The reference spur is reduced from -25.67 dBc to -44.3 dBc. This clearly shows that our CP mismatch and leakage current compensation technique successfully work.

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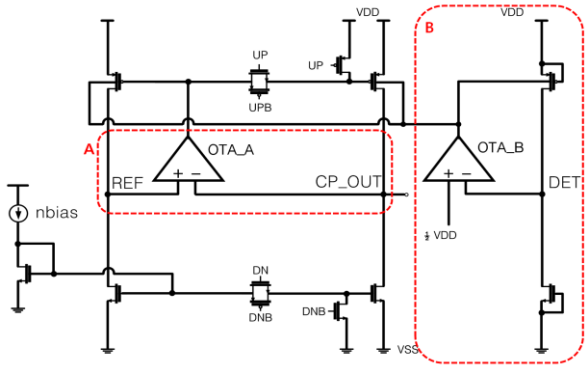

Fig. 2. Proposed charge pump circuit

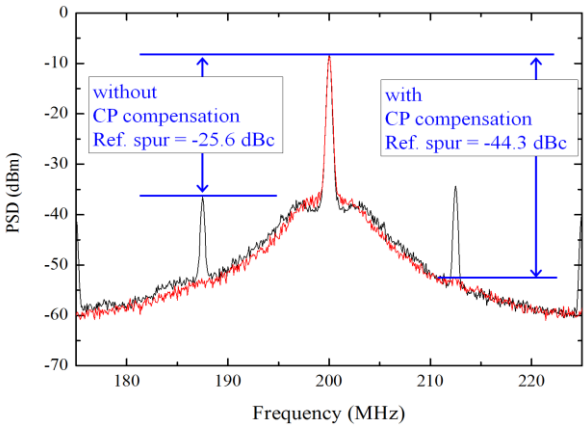

Fig. 3. Measured output spectrum with and without CP compensation

The prototype ULV PLL is fabricated with 130-nm CMOS technology. It consumes only 88 µW and achieves 0.44-mW/GHz of record-low power efficiency among ULV PLLs reported so far.

REFERENCE

[1] Wu-Hsin Chen, Wing-Fai Loke, and Byunghoo Jung, "A 0.5-V, 440-uW frequency synthesizer for implantable medical devices," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 8, pp.1896-1907, August 2012

[2] Kwang-Chun Choi, Sung-Guen Kim, Seung-Woo Lee, Bhum-Cheol Lee, and Woo-Young Choi, "A 990-uW 1.6-GHz PLL based on a novel supply-regulated active-loop-filter vco" *IEEE Trans. on Circuits and Systems II: Express Briefs*, vol.60, no.6, pp. 311-315, June 2013.