# 2013 International SoC Design Conference

Conference Information

Papers

Sponsors

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IEEE Catalog Number : CFP1369E-USB ISBN : 978-1-4799-1141-7

## Program at a Glance

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**Sunday~Monday, November 17~18, 2013**

| Time | | Sunday, Nov. 17 | | | | | Monday, Nov. 18 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | BEXCO Exhibition Center 1 | | | | | BEXCO Convention Hall | | | | | | | |
| From | Till | | 314 | 315 | 316 | 317 | APEC Hall (205) | 201 | 202 | 203 | 204 | 206 | 207 | Lobby |
| 08:30 | | | | | | | Registration | | | | | | | |
| 09:00 | 09:15 | | | | | | | | | | | | | CDC Demo & Panel / IPC Demo |
| 09:15 | 09:30 | | | | | | | | | | RS-1 | | CDC-1 | |
| 09:30 | 09:45 | | | | | | | | | | | | | |
| 09:45 | 10:00 | | | | | | Break | | | | | | | |
| 10:00 | 10:20 | | | | | | **Opening Ceremony** | | | | | | | |
| 10:20 | 11:10 | | | | | | Keynote - 1 | | | | | | | |
| 11:10 | 12:00 | | | | | | Keynote - 2 | | | | | | | |
| 12:00 | 13:30 | | | | | | Lunch | | | | | | | |
| 13:30 | 13:45 | | | | | | | | | | | | | CDC Demo & Panel / IPC Demo |
| 13:45 | 14:00 | | | | | | | | | | | | | |
| 14:00 | 14:15 | | | | | | | COSAR Workshop | RS-2 | SS-1 | SS-2 | RS-5 | CDC-2 | |
| 14:15 | 14:30 | | | | | | | | | | | | | |
| 14:30 | 14:45 | | | | | | | | | | | | | |
| 14:45 | 15:00 | | | | | | | | | | | | | |
| 15:00 | 15:30 | | | | | | Break | | | | | | | |
| 15:30 | 15:45 | Registration | | | | | | | | | | | | CDC Demo & Panel / IPC Demo |
| 15:45 | 16:00 | | | | | | | | | | | | | |
| 16:00 | 16:15 | | T2 | T3 | T4 | T5 | | COSAR Workshopp/ KORUS R&D by KETI | RS-3 | RS-4 | SS-3 | RS-6 | CDC-3 | |
| 16:15 | 16:30 | | | | | | | | | | | | | |
| 16:30 | 16:45 | | | | | | | | | | | | | |
| 16:45 | 17:00 | | | | | | | | | | | | | |
| 17:00 | 17:30 | | | | | | Break | | | | | | | |
| 17:30 | 19:30 | | | | | | Banquet | | | | | | | |

| Session No. | Session Title |
|---|---|
| RS-1 | Design Synthesis & Analysis |
| RS-2 | Emerging Technology 1 |
| RS-3 | Emerging Technology 2 |
| RS-4 | Multimedia SoC's |
| RS-5 | Analog Design Techniques |
| RS-6 | DC-DC and Data converters |
| SS-1 | Application Processor Technologies for Mobile |
| SS-2 | Mobile Multimedia Computing |
| SS-3 | Effective System and Architecture for Mobile Communication Devices |
| **Tutorial** | |
| T2 | High-Bandwidth Memory Interface Design? |
| T3 | Energy Harvesters and Energy Processing Circuits |
| T4 | Circuit Design using FinFETs |

| | |
|---|---|
| T8 | Wireless Transceiver System Design for Modern Communication Standards |

**Tuesday, November 19, 2013**

| Time | | Tuseday, Nov. 19 | | | | | |
|---|---|---|---|---|---|---|---|
| | | BEXCO Convention Hall | | | | | |
| From | Till | APEC Hall(205) | 201 | 202 | 203 | 204 | Lobby |
| 8:30 | | Registration | | | | | |
| 8:45 | 9:00 | | RS-7 | RS-10 | SS-5 | RS-12 | ETRI Demo/ Poster-1 |
| 9:00 | 9:15 | | | | | | |
| 9:15 | 9:30 | | | | | | |
| 9:30 | 9:45 | | | | | | |
| 9:45 | 10:00 | | | | | | |
| 10:00 | 10:20 | Break | | | | | |
| 10:20 | 11:10 | Keynote - 3 | | | | | |
| 11:10 | 12:00 | Keynote - 4 | | | | | |
| 12:00 | 13:30 | Lunch | | | | | |
| 13:30 | 13:45 | | RS-8 | SS-4 | SS-6 | RS-13 | ETRI Demo/ Poster-2 |
| 13:45 | 14:00 | | | | | | |
| 14:00 | 14:15 | | | | | | |
| 14:15 | 14:30 | | | | | | |
| 14:30 | 14:45 | | | | | | |
| 14:45 | 15:30 | Break | | | | | |
| 15:30 | 16:45 | | RS-9 | Rs-11 | SS-7 | | ETRI Demo/ Poster-2 |
| 15:45 | 16:00 | | | | | | |
| 16:00 | 16:15 | | | | | | |
| 16:15 | 16:30 | | | | | | |
| 16:30 | 16:50 | Break | | | | | |
| 16:50 | 17:30 | **Closing Ceremony** | | | | | |

| Session No. | Session Title |
|---|---|
| RS-7 | Reference Circuits |
| RS-8 | Amplifiers & Biomedical SoC |
| RS-9 | Clock and PLL |
| RS-10 | Communication SoC's |
| RS-11 | System IP's & Processors |
| RS-12 | SoC Testing & Verification |
| RS-13 | SoC Design Methodologies |
| SS-4 | Design Challenges in Ultra-low Power Energy Efficient Circuits and Systems |
| SS-5 | Advancements of Emerging CMOS Technologies |
| SS-6 | High-Performance ASICs/IPs Design for Communication Systems |
| SS-7 | Circuit Architectures and Methodologies for Emerging Applications |

## CDC Demo Session

**09:00~17:00 Lobby**
Chair: Kwang Hyun Baek (Chung-Ang University, Korea)
Kyoung Rok Cho (Chungbuk National University, Korea)

# A 5-Gb/s Adaptive Equalizer & Duty-Cycle Corrector Using Asynchronous Under-Sampling Histogram

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## I. INTRODUCTION

In the gigabit data rate single-ended I/O interconnects, inter-symbol interference (ISI) and duty cycle distortion (DCD) deteriorate the deterministic jitter and bit error rate (BER) performance [1]. We present an adaptive single-ended equalizer (EQ) and duty-cycle corrector (DCC), which automatically determines the optimal equalization and duty-cycle conditions based on asynchronous under-sampling histogram [2]. It can compensates 12-dB channel loss and 25 ~ 75% eye crossing level. For 5-Gb/s $2^{31}$-1 PRBS data transmitted over 80-cm FR4 PCB trace, our single-ended EQ and DCC achieves less than $10^{-13}$ BER and 53.2 ps peak-to-peak jitter.

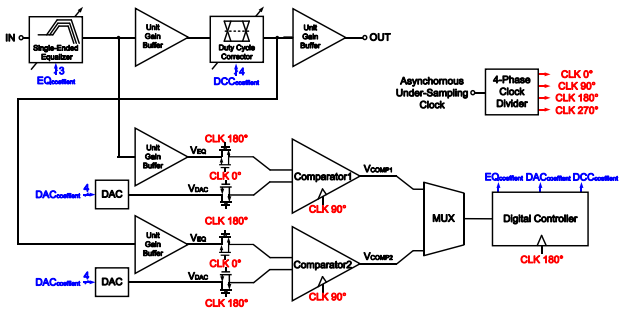


Fig. 1. Block diagram of adaptive single-ended EQ and DCC.

## II. DESCRIPTION

Fig. 1 shows the block diagram of the proposed adaptive single-ended EQ and DCC. It has a 3-bit single-ended EQ filter, a 4-bit DCC, four unit-gain buffers, a 4-phase clock divider, two 4-bit digital-to-analog converters (DACs), four track-and-hold circuits, two comparators, a multiplexer, and an integrated digital controller. The first comparator extracts histograms by comparing the 5-stage single-ended EQ filter output with the reference voltage of 16-level resister ladder DAC, and the digital controller selects the optimal equalization coefficient that produces the largest peak value in histograms. The second comparator extracts histograms by comparing the 6-stage digitally controlled loading DCC output with the reference voltage, and the digital controller chooses the optimal DCC coefficient that produces the smallest gap of peak values in histograms. Unit gain buffers provide isolation from clock feed-through. Track-and-hold circuits offer sufficient timing margin for the sampling process. The multiplexer adjusts sequential operation of equalization and duty-cycle correction.

This work [2012R1A2A1A01009233] was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST). The authors are very thankful to IC Design Education Center (IDEC) for EDA software support, and Samsung Electronics for chip fabrication.

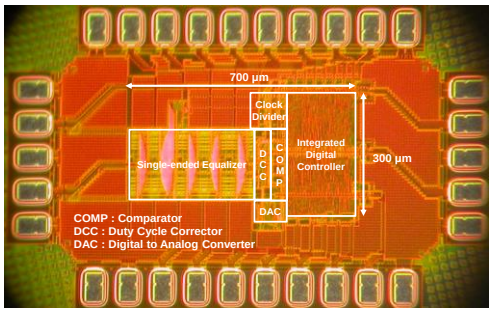


Fig. 2. Chip photograph of the adaptive single-ended EQ and DCC.

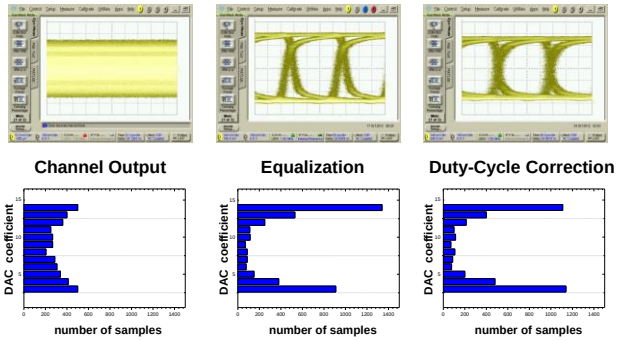


Fig. 3. Measured 5-Gb/s eye diagrams and corresponding histograms.

The clock divider generates 113-MHz quadrature clocks which are asynchronous to the date rate.

## III. CHIP IMPLEMENTAION AND MEASUREMENT RESULTS

Fig. 2 shows a chip photograph of our adaptive single-ended EQ and DCC fabricated in 0.13-μm CMOS technology. The core occupies 0.17-mm$^2$ die area. Fig. 3 shows measured eye diagrams and histograms for 80-cm FR4 PCB trace with 5-Gb/s $2^{31}$-1 PRBS data. The eye is clearly open after equalization and 50 % duty cycle is achieved after duty cycle correction. The BER is less than $10^{-13}$ and the maximum peak-to-peak jitter is 53.2 ps. Total power consumption is 25 mW.

## REFERENCE

[1] J.-D. Ihm et al., "An 80 nm 4 Gb/s/pin 32 b 512 Mb GDDR4 graphics DRAM with low-power and low-noise data-bus inversion," in *IEEE Int. Solid-State Circuits Conf. (ISSCC 2008) Dig. Tech. Papers.*

[2] W.-S. Kim, C.-K. Seong and W.-Y. Choi, "A 5.4-Gb/s adaptive continuous-time linear equalizer using asynchronous undersampling histograms," in *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 59, no. 9, pp. 553-557, Sep. 2012.