

PROGRAMME & ABSTRACTS

Photonics Global Conference

13 -16 Dec 2012

Singapore

Mid-Infrared and THz Photonics

Plasmonics & Metamaterials

Biophotonics

Photonic Materials and Devices

Photonic Nano-Structures

Optical Fiber

Optical Communication



Session 3-3 (Date: 16.12.2012)**Room Pisces 1****Session Name: Nanophotonics and Photonic Devices****Session Chair: Xiaohong Tang**

- 14:00--14:30 *Invited*
(c12a496) Oral 3-3A-1
Synthesis of Homogenous Tungsten Bronze Nanomaterials with Excellent Multi-functionality by a Water Controlled-Release Solvothermal Process
Shu Yin
- 14:30--15:00 *Invited*
(c12a760) Oral 3-3A-2
High Speed Optical Device Simulation
Soon Thor Lim , Ching Eng Png , Vivek Dixit
- 15:00--15:15 Oral 3-3A-3
(c12a646) Metal-assisted photonic mode for ultrasmall bending with long sub-wavelength propagation length
Chengyuan Yang, Ee Jin Teo, Tian Goh, Siew Lang Teo, Jinghua Teng, Andrew Bettiol
- 15:15--15:30 Oral 3-3A-4
(c12a397) Research on picosecond passively Q-switched microchip laser
Takuya Inoue, Toshiki Koike, Kazuyoku Tei, Shigeru Yamaguchi, Jun Enokidani, Shin Sumida

Room Pisces 2**Session Name: Bioimaging and Sensing VI****Session Chair: U. S. Dinish**

- 14:00--14:30 *Invited*
(c12a308) Oral 3-3B-1
Construction of macro scale structure based on nanosized structure units and study on its sensing properties to bio-/chem- environments
Xianfang Zhu
- 14:30--15:00 *Invited*
(c12a340) Oral 3-3B-2
Integrated optofluidics devices: dye sources and plasmonic nanosensors
Anne-Marie Haghiri-Gosnet, Sébastien Méance, Guillaume Aubry, Andrea Cattoni, Jean-Christophe Galas, Qingli Kou, Stéphane Collin
- 15:00--15:30 *Invited*
(c12a294) Oral 3-3B-3
Two-photon Fluorescence Nanothermometry in Bio-Photonics
Jaqueline Daniel
- 15:30--16:00 *Invited*
(c12a331) Oral 3-3B-4
A Spatiotemporal Approach to Coherent Control: Implications in Microscopy
Debabrata Goswami

Room Pisces 3**Session Name: Modulators and Detectors****Session Chair: Goran Mashanovich**

- 14:00--14:30 *Invited*
(c12a603) Oral 3-3C-1
High performance carrier depletion based silicon optical modulators
Dave Thomson
- 14:30--14:45 Oral 3-3C-2
(c12a371) Ge/Si Avalanche Photodetectors with High Gain-Bandwidth Product
Ning Duan
- 14:45--15:00 **Oral 3-3C-3**
(c12a698) **Bit-Error Rate Analysis of Integrated Optoelectronic Receiver**
Jin-Sung Youn, Myung-Jae Lee, Kang-Yeob Park, Holger Rucker, and Woo-Young Choi
- 15:00--15:15 Oral 3-3C-4
(c12a500) Performance Optimization of Waveguided Germanium pin Photodetector for Optical Communication Applications
Andy Lim

Bit-Error Rate Analysis of Integrated Optoelectronic Receiver

J.-S. Youn, M.-J. Lee, K.-Y. Park, and W.-Y. Choi

Department of Electrical and Electronic Engineering
Yonsei University
Seoul, Korea
wchoi@yonsei.ac.kr

Holger Rucker

Im Technologiepark 25
Innovation for High Performance Microelectronics (IHP)
15236 Frankfurt (Oder), Germany

Abstract—In this paper, we investigate a bit-error rate (BER) of an optoelectronic integrated circuit (OEIC) receiver. For this investigation, signal and noise characteristics of a Si avalanche photodetector and a high-speed electronic circuit are analyzed. Using the fabricated OEIC receiver, 12.5-Gb/s $2^{31}-1$ pseudo-random binary sequence optical signal is successfully detected with BER less than 10^{-12} at incident optical power of -7 dBm.

Keywords- Bit-error rate, optoelectronic integrated circuit, Si avalanche photodetector.

I. INTRODUCTION

Recently, there is a growing interest in optical interconnects for short-reach data links such as board-to-board, chip-to-chip, and intra-chip applications. With optical interconnects, the interconnect bottleneck of many high-speed electronic systems can be overcome. Moreover, optical interconnects can provide advantages of less EMI and smaller power consumption than copper-based electrical interconnects [1].

One challenge short-distance optical interconnects face is that they have to be realized in a much more cost-effective manner than solutions used for long-haul optical communications [2]. One attractive approach is realizing interconnect systems based on 850-nm vertical-cavity surface-emitting lasers and multimode fibers. This type of interconnect systems also allow the use of the Si optoelectronic integrated circuit (OEIC) receiver that monolithically includes 850-nm Si photodetector (PD) and receiver circuits. This type of OEIC receiver has advantages of low fabrication cost and high volume manufacturability and can provide higher performance by eliminating pad capacitance and bonding wire inductance that are unavoidable if the PD and receiver circuits are realized in separate platforms [3].

However, Si PDs have inherent drawback of the low detection efficiency due to narrow PN junctions in Si technology and large absorption length at 850 nm. Furthermore, the bandwidth can be limited by the slow diffusion current from a large charge neutral region. In order to overcome these problems, special Si technologies have been used such as a Si-on-insulator substrate [4] and a low-doped epitaxial layer [5]. However, these approaches can increase fabrication cost, and consequently, there are still requirements of high-performance

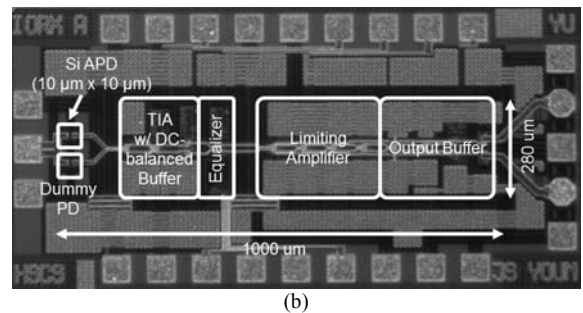
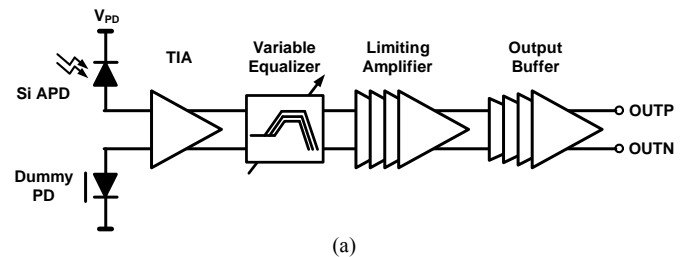


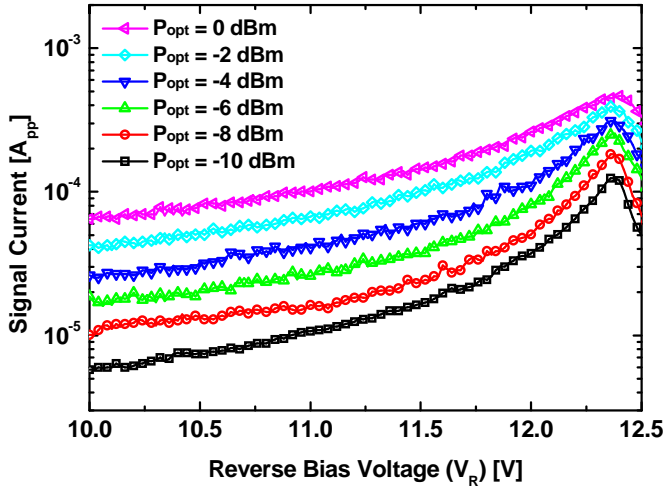
Fig. 1. (a) Block diagram and (b) chip photograph of the fabricated OEIC receiver.

PDs realization using standard Si technology without any process modification.

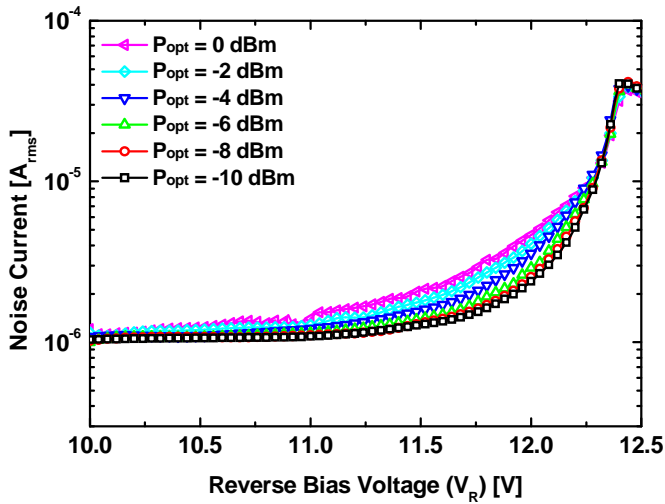
We have previously reported Si avalanche photodetectors (Si APDs) based on P⁺/N-well junction realized with standard CMOS technology [6]. In this paper, we report an OEIC receiver realized with standard SiGe BiCMOS technology. The OEIC receiver is composed of a Si APD with a dummy PD, a shunt-feedback transimpedance amplifier (TIA) with DC-balanced buffer, a variable equalizer, a limiting amplifier, and an output buffer. Fig. 1 shows the simplified block diagram and chip photograph of the fabricated OEIC receiver. Further details on the Si APD and OEIC receiver can be found in [7]. In addition, we investigate a bit-error rate (BER) performance of our OEIC receiver with signal-to-noise ratio (SNR) analysis.

II. SIGNAL-TO NOISE RATIO (SNR) ANALYSIS

We analyze SNR of the fabricated OEIC receiver for the goal of optimizing system performance. A SNR at TIA input



(a)



(b)

Fig. 2. (a) Signal current and (b) Noise current of the APD as a function of reverse bias voltage (V_R). The incident optical power is from -10 dBm to 0 dBm.

node can represent overall receiver performance, and it can be shown as Eq. (1)

$$SNR = \alpha_{total} \cdot \frac{I_{s,APD,pp}(V_R)}{\sqrt{I_{n,APD,rms}^2(V_R) + I_{n,circuit,rms}^2}} \quad (1)$$

In the above equation, $I_{s,APD}$ represents the peak-to-peak output signal currents of APD, and $I_{n,APD}$ and $I_{n,circuit}$ represent rms noise currents of APD and electronic circuits, respectively. Especially, $I_{s,APD}$ and $I_{n,APD}$ are dependent on the reverse bias voltage (V_R) of APD, and consequently, V_R needs to be carefully determined to achieve the optimum SNR.

A. APD Signal and Noise Current

Fig. 2 shows the measured signal and noise currents of APD at different V_R . These are measured a spectrum analyzer with V_R from 10.0 V to 12.5 V. The incident optical power (P_{opt}) is varied from -10 dBm to 0 dBm in increasing steps of 2

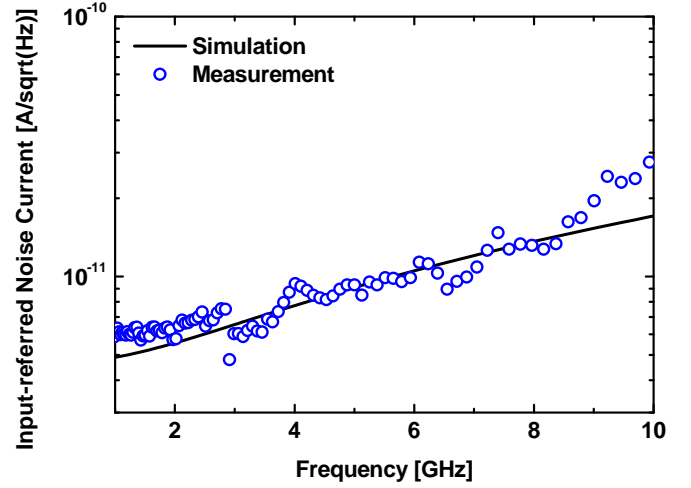


Fig. 3. The simulated and measured input-referred noise currents of the electronic circuits.

dBm. For signal measurement, a 1-GHz sinusoidal signal is modulated by an optical source, and the modulated signal is detected by APD. For noise measurement, a low-noise amplifier (LNA) is used at the output of the APD to overcome the limit of equipment noise floor. The measurement results are calibrated to exclude the effects of electrical cable and LNA, and converted to peak-to-peak signal current and rms noise current, respectively. With increasing V_R , the signal current increases because of avalanche multiplication. It is maximized at V_R of about 12.4 V. In addition, the measured noise current also increases due to increased avalanche noise.

B. Electronic Circuit Noise Current

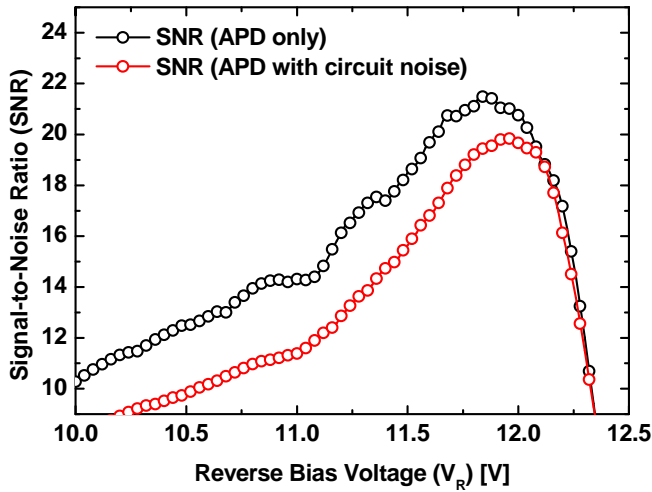
Fig. 3 shows the simulated and measured input-referred noise current of the electronic circuits. The output noise is measured using a spectrum analyzer with 50- Ω load. From the measurement results, rms input-referred noise current can be calculated from the average noise current using following Eq. (2).

$$I_{n,circuit,rms} = i_{n,circuit,avg} \cdot \sqrt{BW_n} \quad (2)$$

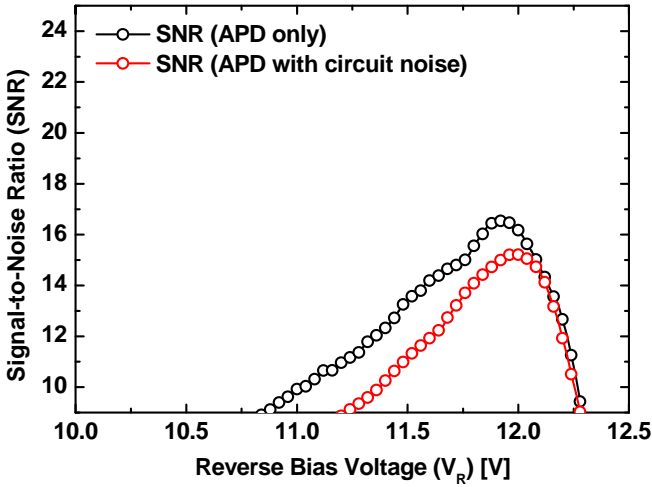
where BW_n is the noise bandwidth. Our electronic circuit has low input-referred noise current of about 0.83 μA_{rms} .

C. SNR of OEIC Receiver.

From the measured signal and noise currents of APD and electronic circuits, SNR can be calculated by using Eq. (1). The black curves in Fig. 4 show the calculated SNR of APD at the P_{opt} of -8 dBm and -10 dBm, respectively. It can be observed that the optimum V_R to achieve the best SNR is about 11.85 V which is different to the bias condition for the maximum signal swing of 12.4 V. For V_R below 11.85 V, the SNR is degraded because the signal current cannot have sufficient avalanche gain in spite of the small thermal noise. For V_R above 11.85 V, the signal current is sharply enhance, however, the SNR is also degraded due to the increased shot noise. The red curves in the Fig. 4 shows the calculated SNR of APD with the electronic circuit noise. The SNR is considerably degraded by the circuit



(a)



(b)

Fig. 4. The calculated signal-to-noise ratio of the fabricated OEIC receiver at incident optical power (P_{opt}) of (a) -8 dBm and (b) -10 dBm, respectively.

noise, and it can be observed that the optimum V_R for the best SNR shifts to about 12.0 V due to the electronic circuit noise.

III. BIT-ERROR RATE (BER) ANALYSIS

To verify SNR analysis, we measure BER performance by varying V_R as shown in Fig. 5. For these measurements, 6-Gb/s optical signal is detected by our OEIC receiver at P_{opt} of -8 dBm and -10 dBm. Fig. 5 also shows the estimated BER performance which is calculated from SNR with Eq. (3)

$$BER = \frac{1}{2} \cdot \operatorname{erfc} \left(\frac{SNR}{2\sqrt{2}} \right). \quad (3)$$

For data matching between the measured and estimated BER, we use a fitting parameter of about 0.88 which is derived using sum squared error function. It means that the measured signals have penalties of about 12%. As shown in Fig. 5, the best BER can be achieved at V_R of about 12.0 V, and consequently, these results indicate that our SNR analysis provides good estimation.

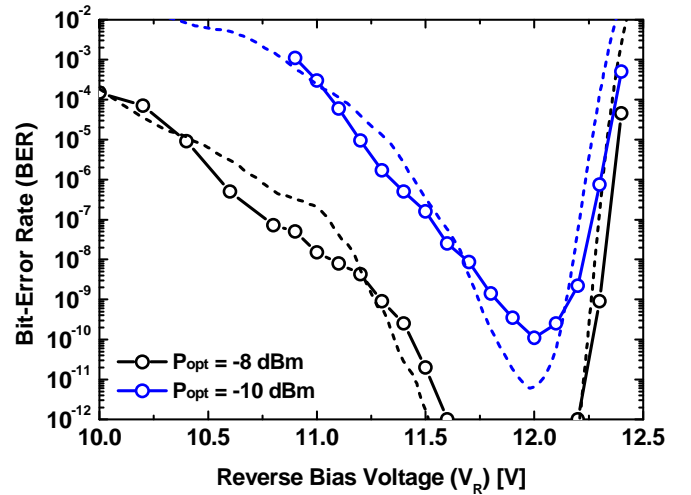


Fig. 5. The measured (solid line with circle) and estimated (short dash line) bit-error rate (BER) as a function of the reverse bias voltage (V_R) at different incident optical power (P_{opt}) of -8 dBm and -10 dBm, respectively.

IV. CONCLUSION

We investigate a BER of the fabricated OEIC receiver with SNR analysis. With this analysis, we can evaluate the OEIC receiver performance, and the optimum APD bias for the best BER performance can be verified.

ACKNOWLEDGMENT

This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MEST) [2012R1A2A1A01009233]. The authors are very thankful to IC Design Education Center (IDEC) for EDA software support.

REFERENCES

- [1] D. Miller, "Device requirements for optical interconnects to silicon chip," *Proc. IEEE*, vol. 97, no. 7, pp. 1166–1185, Jul. 2009.
- [2] N. Bamiedakis, J. Beals, R. V. Pentyl, I. H. White, J. V. DeGroot, and T. V. Clapp, "Cost-effective multimode polymer waveguides for high-speed on-board optical interconnect," *IEEE J. Quantum Electron.*, vol. 45, no. 4, pp. 415–424, Apr. 2009.
- [3] A. C. Carusone, H. Yasotharan, and T. Kao, "CMOS technology scaling considerations for multi-gbps optical receivers with integrated photodetectors," *IEEE J. Solid-State Circuits*, vol. 46, no. 8, pp. 1832–1842, Aug. 2011.
- [4] R. Li, J. D. Schaub, S. M. Csutak, and J. C. Campbell, "High-speed monolithic silicon photoreceiver fabricated on SOI," *IEEE Photon. Technol. Lett.*, vol. 12, no. 8, pp. 1046–1048, Aug. 2000.
- [5] A. Nemecek, G. Zach, R. Swoboda, K. Oberhauser, and H. Zimmermann, "Integrated BiCMOS p-i-n photodetectors with high bandwidth and high responsivity," *IEEE J. Sel. Topics Quantum Electron.*, vol. 12, no. 6, pp. 1469–1475, Nov. 2006.
- [6] H.-S. Kang, M.-J. Lee, and W.-Y. Choi, "Si avalanche photodetectors fabricated in standard complementary metal-oxide-semiconductor process," *Appl. Phys. Lett.*, vol. 90, no. 15, pp. 151118-1–151118-3, Apr. 2007.
- [7] J.-S. Youn, M.-J. Lee, K.-Y. Park, H. Rucker, and W.-Y. Choi, "A 12.5-Gb/s SiGe BiCMOS optical receiver with a monolithically integrated 850-nm avalanche photodetector," in *Proc. OFC 2012*, Los Angeles, CA, Mar. 2012, Paper OM3E.