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Conference Guide

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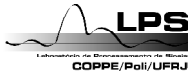

Signal Processing Laboratory

The Brazilian Development Bank

Nokia Technology Institute

A1L-M Oscillators

Time: Monday, May 16, 2011, 10:30 - 12:10
Place: SEGOVIA III
Chair(s): Orla Feely, *University College Dublin*
Jinhu Lu, *Chinese Academy of Sciences*

10:30
A1L-M.1 Low Phase Noise on-Chip Oscillator for Implantable Biomedical Applications
Fatemeh Aghlmand, Mojtaba Atarodi, Saeed Saeedi
Sharif University of Technology, Iran

10:50
A1L-M.2 On the Bias Noise to Phase Noise Conversion in Harmonic Oscillators Using Groszkowski Theory
Andrea Bevilacqua[2], Pietro Andreani[1]
[1]Lund University, Sweden; [2]Università degli Studi di Padova, Italy

11:10
A1L-M.3 A Phase-Noise Model for Nonlinear Piezoelectrically-Actuated MEMS Oscillators
Mauricio Pardo, Logan Sorenson, Farrokh Ayazi
Georgia Institute of Technology, United States

11:30
A1L-M.4 A Regulated 3.1-10.6 GHz Linear Dual-Tuning Differential Ring Oscillator for UWB Applications
Li Lu[1], Changzhi Li[1], Jenshan Lin[2]
[1]Texas Tech University, United States; [2]University of Florida, United States

11:50
A1L-M.5 Supply Noise Insensitive Ring VCO with on-Chip Adaptive Bias-Current and Voltage-Swing Control
Young-Seok Park, Woo-Young Choi
Yonsei University, Korea, South

Supply Noise Insensitive Ring VCO with On-Chip Adaptive Bias-Current and Voltage-Swing Control

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***Abstract*— This paper demonstrates a CMOS Ring Voltage Controlled Oscillator (RVCO) whose oscillation frequency is insensitive to supply noise. Our RVCO achieves this with on-chip adaptive bias-current and voltage-swing control. A prototype RVCO is fabricated with 0.13um CMOS technology and it achieves static supply voltage sensitivity of 0.013%-f_{vco}/1%-V_{dd} and dynamic sensitivity of 0.08%-f_{vco}/1%-V_{dd}.**

I. INTRODUCTION

Phase-Locked Loops (PLLs) are widely used for on-chip clock generation for many electronic circuits and systems. Designing a low-noise PLL is very important because low-noise clock signals are critical to the proper operation of digital circuits. Ring Voltage Controlled Oscillators (RVCOs) are widely used for PLLs due to their advantages such as easy integration, wide tuning range, and multi-phase clock generation capability. But RVCOs typically have high sensitivity especially on the external noise sources such as supply voltage noise. Consequently, design of low-noise RVCOs having low supply voltage sensitivity has received much research attention [1]-[7].

In [2], a supply voltage regulator was used to reduce the supply-induced jitters, but the regulator takes up a large die area with the need for a large capacitor and this limits their bandwidth of compensation. AC coupling supply and control voltages with a capacitor can reduce supply voltage sensitivity [3], but this also requires a large capacitor. Controlling bias-currents for supply noise can reduce RVCO's supply voltage sensitivity [4], but this requires an external current source and its compensation performance can be affected by process variation.

In this paper, we demonstrate a new on-chip adaptive compensation technique for reducing supply voltage sensitivity of RVCOs. Section II describes the proposed RVCO along with the compensation technique. Section III gives simulation and measurement results, and conclusion is given in Section IV.

II. THE SUPPLY NOISE COMPENSATION SCHEME

The oscillation frequency of a RVCO can be expressed as

$$f_{OSC} = \frac{I_{bias}}{N \cdot C_{tot} \cdot V_{swing}}, \quad (1)$$

where I_{bias} is bias-current, N is the number, and C_{tot} is load capacitance of a delay stage, and V_{swing} is the voltage-swing of a RVCO. Supply noise can affect V_{swing}, I_{bias} and C_{tot}. The influence of supply noise on V_{swing}, I_{bias}, C_{tot} can be reduced, if we first detect supply noise, and control V_{swing}, I_{bias}, C_{tot} accordingly. But controlling C_{tot} is difficult as compared to controlling V_{swing} and I_{bias} because of its large size. Therefore, our RVCO relies on voltage-swing and bias-current controllers in order to achieve supply noise compensation as shown in Fig. 1.

As shown in the figure, the RVCO is implemented with fully differential delay stages. V_{swing} control voltage (V_{load}) is applied to the gate voltage of load PMOS, and I_{bias} control voltage (V_{bias}) is applied to the gate voltage of bias NMOS in each delay stage. In designing controllers, their bandwidth should be wider than the natural frequency of the PLL that will employ the RVCO. This is because supply noise has band-pass characteristics with the center frequency at the PLL natural frequency [5], which is typically from 100 kHz to 10MHz.

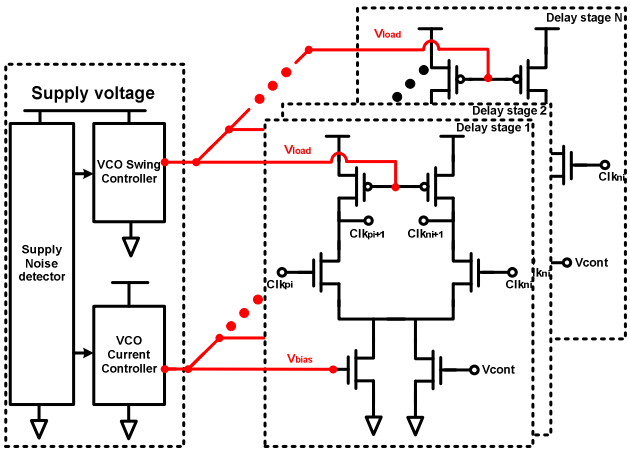

Fig. 1. Block diagram of RVCO with supply noise compensation.

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A. *RVCO bias-current controller*

Fig. 2 shows the circuit topology for RVCO bias-current controller. It has a feedback amplifier which can control the gate voltage of Mn2 (V_{bias}) to maintain the total current (I_{tot}) constant. Mp1 can determine I_{tot}. Mn1 and Mn3 are the replica of the differential pair delay stage shown in Fig. 1. Mn4 determines the amount of I_{sense} which can reduce I_{bias} fluctuation due to supply noise.

The supply noise causes fluctuations in V_{sg} of Mp1 as well as V_{sd} of Mp1 because of the channel length modulation effect of MOSFET. These voltage fluctuations cause I_{tot} variation. To prevent this problem, we design a current controller reference voltage generator and sensing NMOS gate voltage generator. Fig. 3a shows the simulation results of output voltages of each voltage generator with supply voltage changes. If supply voltage increases, output voltage of the current controller reference voltage generator (V1) also increases. It can reduce the fluctuations in the V_{sd} of Mp1 because feedback amplifier controls V_{bias} to equal the V1 and V3 value. Consequently, the variation in I_{tot} caused by channel length modulation can be reduced. Moreover, I_{sense} also increases if supply voltage increases because the output voltage of the sensing NMOS gate voltage generator (V2) increases. Because I_{bias} is subtraction of I_{tot} and I_{sense}, this helps maintaining the constant I_{bias} value even in a noisy supply voltage environment. The simulation results show that fluctuation of I_{bias} of RVCO bias-current controller is about 70μA when supply voltage varies ±5% as shown in fig. 3b. Without each voltage generator and sensing NMOS, I_{bias} fluctuation is about 276μA.

B. *RVCO voltage-swing controller*

Fig. 4 shows the RVCO voltage-swing controller circuit. It also has feedback amplifier to maintain V5 value same as V4 by using regulated gate voltage of Mp1 (V_{load}) even if V_{bias}, V_{cont} and supply voltage are varied. Because Mp1, Mn1, Mn2 and Mn3 are the replica of the delay stage, this circuit always keeps V_{swing} of RVCO from V_{dd} to V4.

In this controller, the output voltage of the swing controller reference voltage generator (V4) is independent of supply voltage. Thus, V_{swing} of RVCO is proportional to supply voltage. Because of this, the RVCO voltage-swing controller forces the oscillation frequency of RVCO to change in the opposite direction to the change in supply voltage. This reduces overall supply voltage sensitivity of RVCO because RVCO bias-current controller cannot perfectly maintain constant I_{bias} for each delay stage. Although RVCO bias-current controller reduces the slope of I_{bias} dependence on supply voltage, the current is still proportional to supply voltage as shown in Fig 3b. RVCO voltage-swing controller can compensate the effect of imperfection of RVCO bias-current controller.

C. *Overall-VCO design*

Using voltage-swing and bias-current controllers, a four-stage fully-differential RVCO was designed as shown Fig. 5. The bandwidth of these controllers is determined by the bandwidth of each feedback amplifier. Thus, the bandwidth of feedback amplifier should be wider than the natural frequency of PLL which employ the RVCO.

The only difference between this RVCO and a typical fully-differential RVCO is the bias-current and voltage-swing controllers. Because RVCO bias-current and voltage-swing controllers are entirely composed of active devices, the die area penalty is negligible.

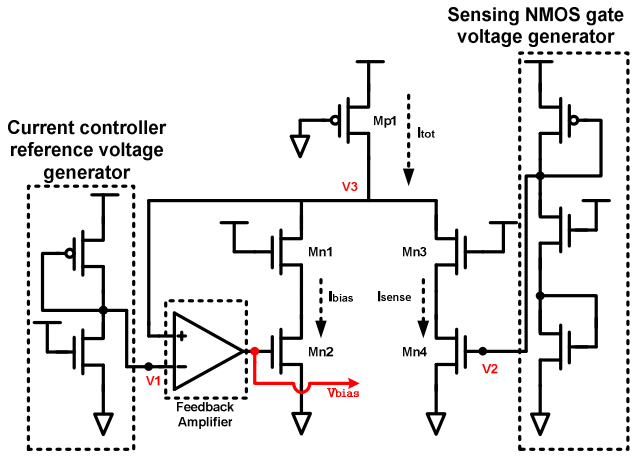
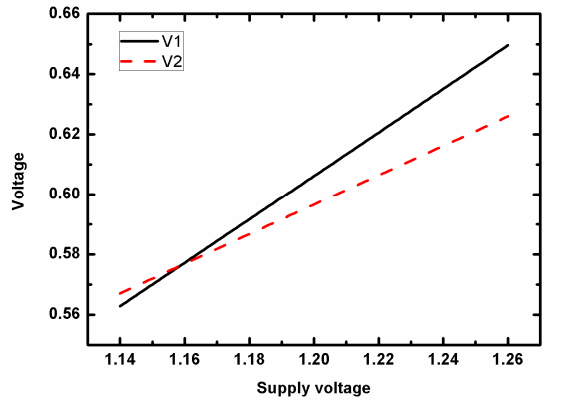
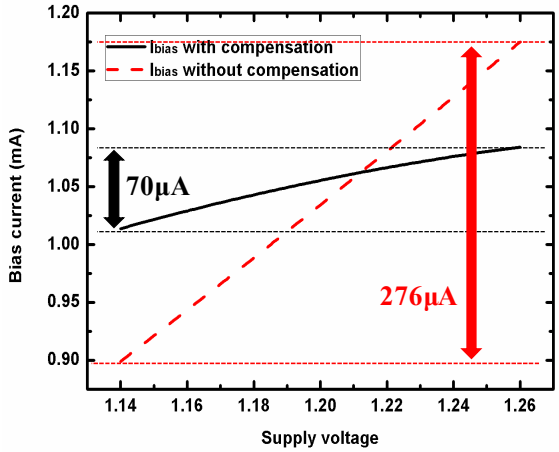


Fig. 2. RVCO bias-current controller circuit topology



(a)



(b)

Fig. 3. Simulation results of (a) output voltage of each voltage generators, and (b) bias-current fluctuation due to supply voltage.

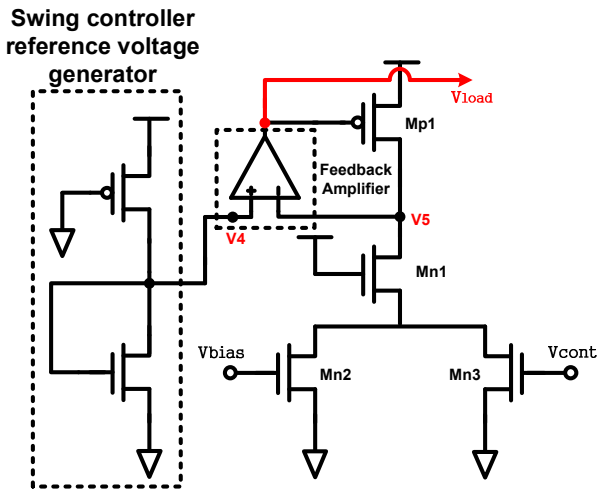


Fig. 4. RVCO voltage-swing controller circuit topology

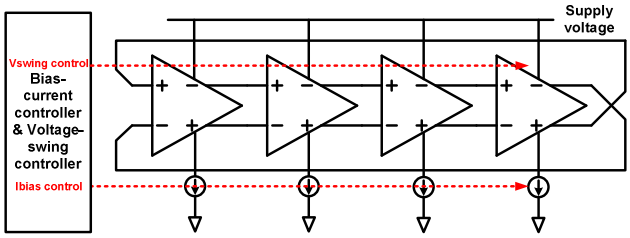


Fig. 5. Proposed 4-stage RVCO

III. Simulation and Measurement Results

Two types of RVCO have been designed and fabricated in 0.13µm CMOS technology. Type I RVCO includes controllers described above and Type II does not. Figure 6 shows a die that includes both RVCOs. The core area of Type I RVCO is 0.0066mm^2 (72µm × 92µm), and that of Type II is 0.006mm^2 (72µm × 84µm). The simulation result shows that the power consumption of Type I RVCO is 19.56mW and Type II is 15.36mW.

The simulated and measured static supply voltage sensitivity for both types is shown in Fig. 7. DC supply voltage is varied by ± 5% and the frequency variation of free-running VCOs with 0V control voltage is simulated and measured. The reason for setting the control voltage at 0V is because at this voltage each VCO has very small gain and therefore the influence of control voltage on the oscillation frequency can be eliminated.

In the figure, the measured supply voltage sensitivity is expressed in %-f_{vco}/%-V_{dd}. Measurement results indicate that Type I RVCO achieves 0.013%-f_{vco}/1%-V_{dd} as compared to 0.53%-f_{vco}/1%-V_{dd} for Type II RVCO. Simulation results agree well with measurement results.

Fig. 8 shows simulation results of dynamic supply voltage sensitivity for both types of RVCOs. The supply voltage is modeled as a sinusoidal source with 10MHz noise frequency, which is large enough compared to the natural frequency of a PLL. The amplitude of noise is 0.12V. Control voltage of each RVCO is selected so that both RVCOs have the same oscillation frequency.

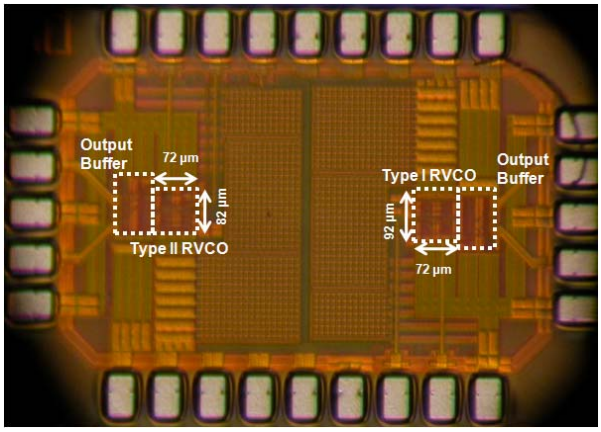


Fig. 6. Chip micrograph

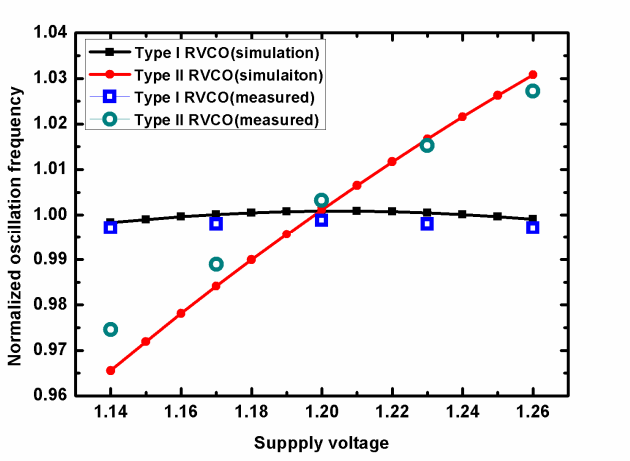


Fig. 7. Static supply voltage sensitivity of Type I RVCO and Type II RVCO

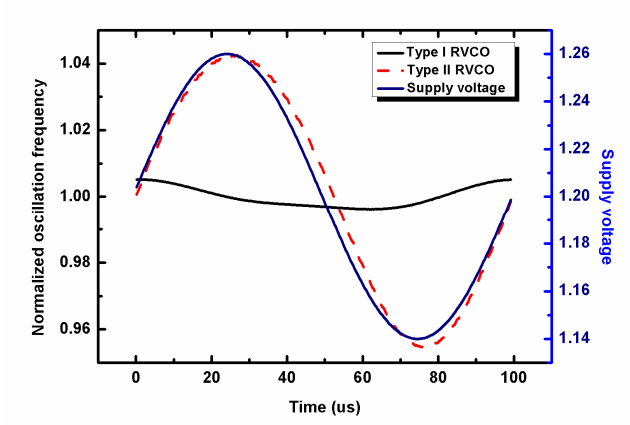


Fig. 8. Dynamic supply voltage sensitivity of Type I RVCO and Type II RVCO

The simulation result shows that the oscillation frequency of Type II RVCO changes following the supply voltage with dynamic sensitivity of 0.879%-f_{vco}/1%-V_{dd}. On the other hand, the oscillation frequency of type II RVCO has very little supply voltage dependency with dynamic sensitivity of 0.08%-f_{vco}/1%-V_{dd}.

IV. CONCLUSION

We demonstrate a supply noise insensitive RVCO with a new on-chip supply noise compensation technique. The RVCO has current-bias and voltage-swing controllers for supply noise compensation, The RVCOs implemented in 0.13μm CMOS technology show with controllers static supply voltage sensitivity is reduced by factor of 25 and dynamic supply voltage sensitivity by factor of 10 with a negligible die area penalty.

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