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Ramada Plaza Hotel, Jeju, Korea
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International SoC Design Conference (ISOCC) aims at providing the world's premier SoC design forum for leading researchers from academia and industries. Prospective authors are invited to submit papers of their original works. ISOCC 2011 is technically co-sponsored by **IEEE CAS** Society and accepted papers will be published on **IEEE Xplore**.

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Analog and Mixed-Signal Circuits	Communication SoCs
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Low Power Design Techniques	Microprocessor and DSP Architectures
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Important Dates

28 Aug. 2011	
• Deadline for submission of regular full paper;	~~**21 Aug. 2011**~~
• Deadline for submission of chip design contest ;	**21 Aug. 2011**
• Deadline for submission of special session full paper;	**14 Sept. 2011**
• Notification of acceptance (all submitted papers):	**01 Oct. 2011**
• Deadline for final paper submission;	**15 Oct. 2011**
• Deadline for author and early-bird registration;	**15 Oct. 2011**

At least one author of each accepted paper must register by October 15, 2011.

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• Design of Timing-Error-Resilient Systolic Arrays for Matrix Multiplication
Hsin-Chou Chi, Hsi-Che Tseng and Kun-Lin Tsai
National Dong Hwa University, Taiwan

08:20~09:50 Session 12 Room C

Regular Session

RF Techniques

Chair Yun Seong Eo
(Kwangwoon University)

• A 10.3Gbps TransImpedance Amplifier with Mutually Coupled Inductors in 0.18-μm CMOS
Shigekazu Miyawaki[(1)], Makoto Nakamura[(2)], Akira Tsuchiya[(1)], Keiji Kishine[(3)] and Hidetoshi Onodera[(1)]
[(1)]Kyoto University, Japan
[(2)]NTT Corporation, Japan
[(3)]University of Shiga Prefecture, Japan

• A Study on Wide-band Frequency Synthesizer for Advanced Wireless Communication
Nakyoon Kim and Yong Moon
Soongsil University, Korea

• A 5-Gb/s Low-Power Transmitter with Voltage-Mode Output Driver in 90nm CMOS Technology
Jinsoo Rhim and Woo-Young Choi
Yonsei University, Korea

• A 34 dBm $IP_{0.1dB}$ SOI SP3T Switch with an Integrated Negative-Bias Switch Controller at 2.4 GHz
Sunwoo Yoon, JuYoung Jung and Dong-hyun Baek
Chung-Ang University, Korea

• Design Considerations for Cognitive Radio Based CMOS TV White Space Transceivers
Jongsik Kim and Hyunchol Shin
Kwangwoon University, Korea

A 5-Gb/s Low-Power Transmitter with Voltage-Mode Output Driver in 90nm CMOS Technology

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Abstract— **A 5-Gb/s low-power transmitter having an output impedance calibration circuit and a voltage-mode output driver is implemented for high-speed serial link applications. The output impedance calibration circuit matches the output impedance of output driver to the characteristic impedance of the channel. This transmitter includes 32:1 serializer based on voltage-mode logic which operates successfully at 5-Gb/s. In addition, on-chip parallel PRBS7 (2^7-1) generator is implemented for testing. The transmitter consumes 8.6mW with 300mVp-p output swing and occupies 60 µm X 70 µm of area.**

Keywords - voltage-mode output driver; output-impedance calibration; low power; transmitter

I. INTRODUCTION

For many interface applications, high-speed serial interface is widely used instead of parallel interface since it requires less area and power due to the reduced number of I/O pins and it suffers less from crosstalk noise and data-clock skew [1-3]. Furthermore, the need for power consumption reduction in high-speed serial interface circuits has greatly increased.

In this paper, a 5-Gb/s transmitter in 90nm CMOS technology is presented that has been designed for low-power consumption in mind. It employs voltage-mode output driver with output impedance calibration circuit in order to reduce the power of the transmitter while maintaining the output impedance matched to the channel. On-chip parallel PRBS generator and 32-to-1 serializer are also implemented.

Section II describes the overall design of the transmitter and the details of implemented circuits are shown in Section III. Section IV shows the experiment results.

II. LOW POWER TRANSMITTER

A. Overall structure

Figure 1 shows the overall block diagram of the transmitter. The PRBS generator produces 32 parallel PRBS-7 data streams of 156.25 Mb/s which are converted to 5-Gb/s serialized data by 32:1 serializer. Required multiple-rate clocks for the serializer are provided by the clock tree by dividing the external clock. The voltage-mode output driver consists of pre-driver and output driver with regulated supply voltage from output impedance calibration circuit. This calibration circuit

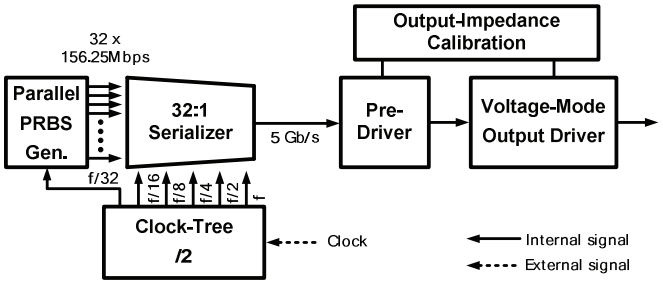

Fig. 1. Overall block diagram of transmitter

controls the output impedance of the output driver in order to minimize the reflection due to the impedance mismatch between output driver and the channel. All of the circuits including the output driver are designed based on voltage-mode logic to reduce the power consumption. The parallel PRBS generator is digitally synthesized.

B. Voltage-mode logic and current-mode logic

The operation speed of voltage-mode logic has increased with the advanced CMOS technology. Compared to current-mode logic, which consumes constant power when the supply voltage is provided, voltage-mode logic consumes power only during data transitions. Since the amount of leakage current is less than the dynamic current for over 65nm CMOS technology, the power consumption of the voltage-mode logic is much less than that of current-mode logic. Moreover, the transistor size for voltage-mode logic can be smaller than that of current-mode logic due to its smaller current usage, which consequentially reduces the overall circuit area.

C. Voltage-mode output driver

Output driver designed with current-mode logic is shown in Figure 2. It can easily match the output impedance by controlling the load resistor or bias voltage applied to PMOS transistors. Furthermore, the maximum operation speed of current-mode logic is larger than that of voltage-mode logic. However, it consumes a considerable amount of power in order to drive the load resistor, particularly at the last stage of the output driver where the load resistance is the characteristic

impedance of the channel. Usually, output driver based on current-mode logic consumes over 10mW of power, which is much more than desired for low-power interface systems. The output driver based on voltage-mode logic consumes much less power and occupies less area as well. The difficulty of using voltage-mode logic for output driver is matching the driver output impedance to the channel. In this case, the output impedance is determined by the supply voltage and the gate voltages applied to the composing transistors. Consequently, regulation of the supply voltage as well as pre-driver is necessary.

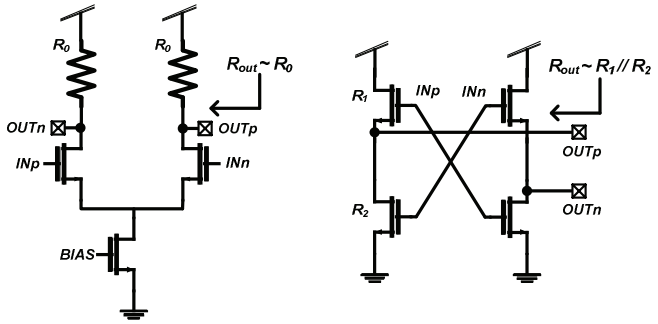

Fig. 2. Current-mode logic (left) and voltage-mode logic (right)

III. CIRCUIT IMPLEMENTATION

The voltage-mode logic adopted in this work is based on clocked inverter and pass-gate multiplexer as shown in figure 3. The clocked inverter keeps the data if the pass gates are turned off and inverts the input data if otherwise. The pass-gate multiplexer chooses its output according to the clock input.

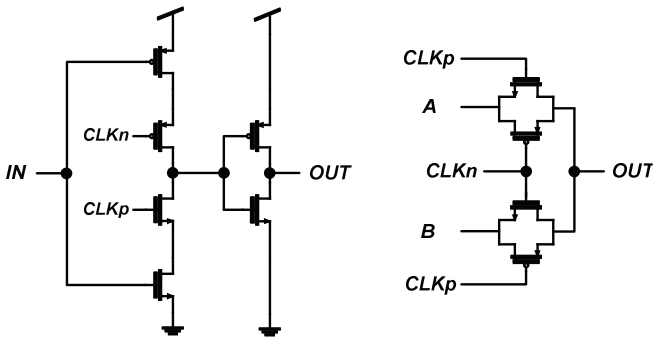

Fig. 3. Clocked inverter (left) and pass-gate multiplexer (right)

A. 32:1 Serializer

As shown in the figure 4, 32:1 serializer includes several 2:1 serializers, and each 2:1 serializer is composed of two latches and 2:1 multiplexers (MUXs). The dividers are used for the clock tree in order to provide proper clock signals to 32:1 serializer. Figure 5 and 6 show the schematic of the 2:1 serializer. Each 2:1 serializer is based on a double-edge triggered flip-flop [5], including 2 latches and 1 multiplexer, and one additional latch is inserted to generate half-period delay. Two latches keep the data alternatively by using the opposite clock. The 2:1 multiplexer finally serializes two input data using both edges of the clock.

In order to generate differential signal for output driver, the last stage of 32:1 serializer uses the pseudo-differential signaling scheme. Figure 6 shows the schematic of the pseudo-differential 2:1 serializer, which occupies additional 2:1 multiplexer with cross-coupled input data at the end of the stage.

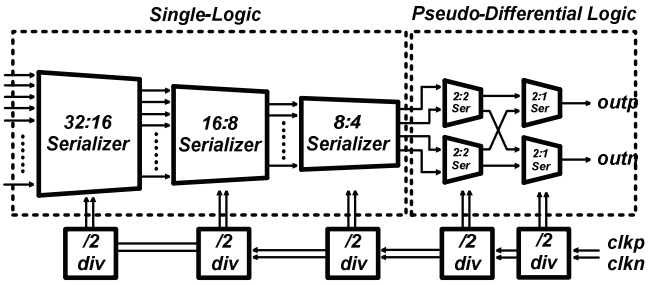

Fig. 4. 32:1 Serializer

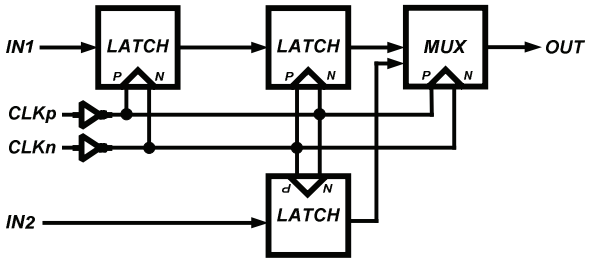

Fig. 5. 2:1 Serializer

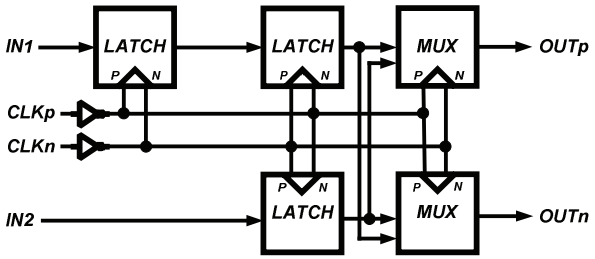

Fig. 6. 2:1 Serializer with pseudo-differential output

B. Impedance Calibration of Voltage-mode Output Driver

The voltage-mode output driver with output impedance calibration circuit is implemented. As mentioned above, the voltage-mode output driver uses less power compared to the output driver based on current-mode logic. Output driver based on current-mode logic should be able to drive relatively low impedance in order to match the characteristic impedance of the channel. Meanwhile, it is difficult to match the output impedance to the characteristic impedance of the channel. Therefore, the output impedance calibration circuit is also designed for this transmitter.

The voltage-mode output driver consists of two parts: the pre-driver and the output driver. The pre-driver is an inverter stage with regulated supply voltage which matches the output impedance of the driver to the characteristic impedance of the channel. The output driver has two complementary pairs of NMOS transistors.

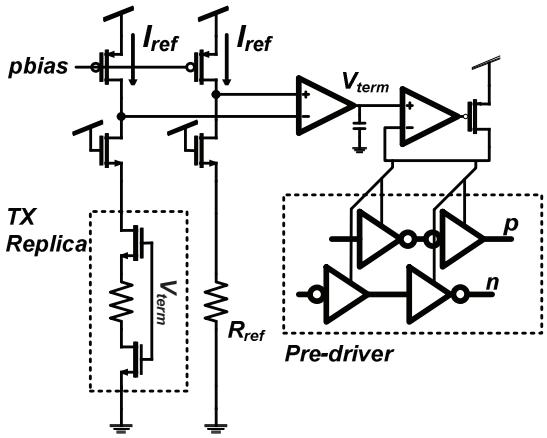

Fig. 7. Supply regulation on pre-driver

The impedance calibration circuit for the pre-driver is shown in figure 7. It is a negative feedback loop including reference resistor (R_{ref}), which represents the characteristic impedance of the channel, and a replica output driver. Two PMOS transistors drive the same amount of current (I_{ref}) to R_{ref} and the replica of output driver. The feedback loop forces the gate voltage of the output driver replica (V_{term}) in order to make the impedance of the output driver replica equal to R_{ref}. Thus, the output impedance of output driver becomes R_{ref} by regulating the supply voltage of the pre-driver to V_{term}.

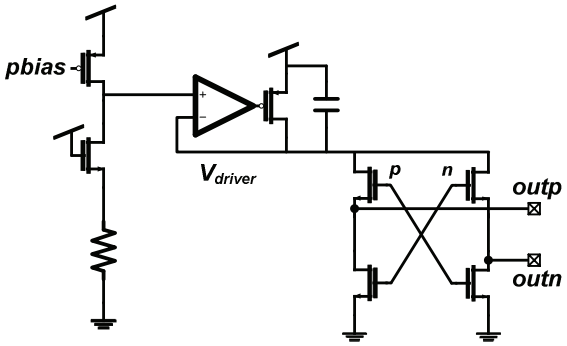

Fig. 8. Supply regulation on output driver

The power of output driver should be also regulated to match the output impedance to Rref as shown in figure 8. The second regulator, which generates the supply voltage of output driver (V_{driver}), is designed by adopting the same structure used for pre-driver supply regulation. With the regulated supply voltage (V_{driver}) and pre-driver input (V_{term}), the output impedance of the output driver can be matched to R_{ref}.

IV. Measurement Results

The transmitter is implemented with 90nm CMOS technology and measured with on-wafer probing. The microphotograph of the fabricated chip is shown in figure 9. The area of the transmitter core is 60 μm X 70 μm. It produces 5-Gb/s data with 17.73ps_{p2p} of jitter under 1.2V supply voltage and consumes 8.5mW of power. The measurement setup is shown in figure 10 and the eye-diagram of the data is show in figure 11.

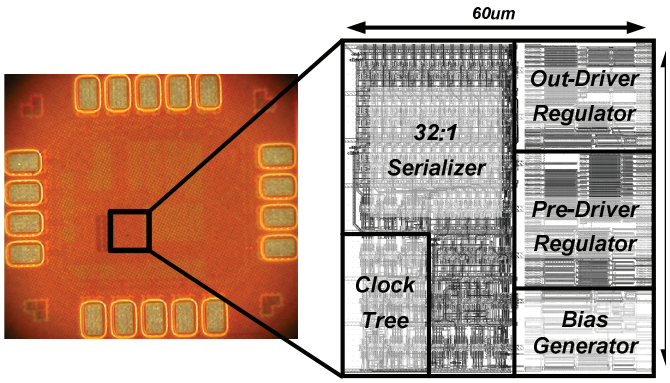

Fig. 9. Microphotograph and layout of fabricated chip

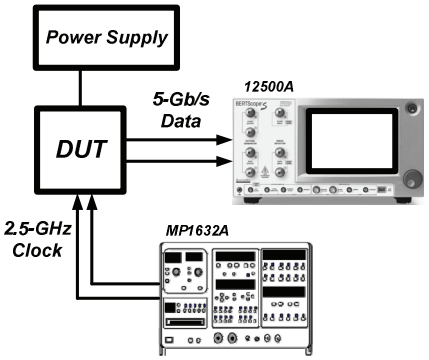

Fig. 10. Measurement setup

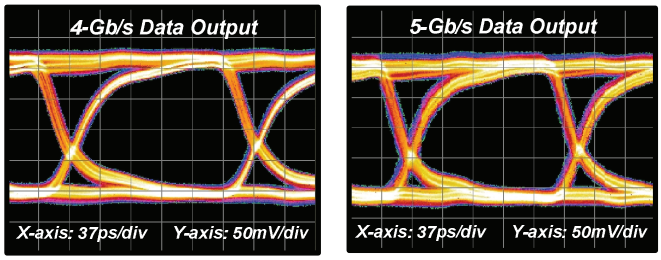

Fig. 11. Eye-diagram of output data: @ 4-Gb/s (left) @ 5-Gb/s (right)

The operation of output-impedance calibration circuit is verified by measuring the reflection coefficient of the transmitter and the output impedance. The S11 parameter in figure 12 is lower than -30dB at 2.5GHz and the output impedance in figure 13 is located at the center of the Smith chart. Table 1 summarizes the performance of designed transmitter

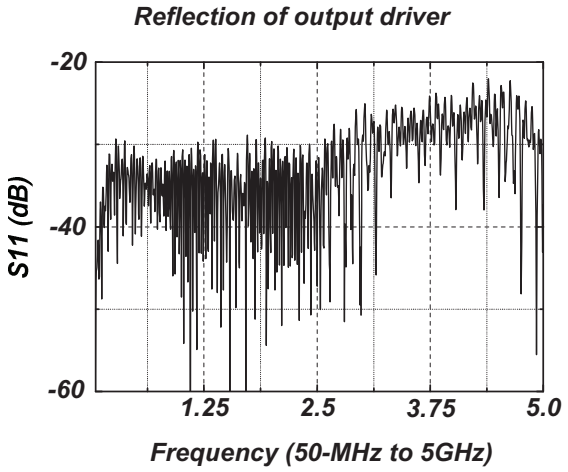

Fig. 12. Measured reflection of voltage-mode output driver

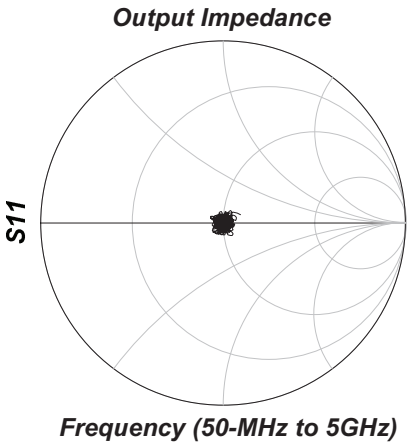

Fig. 13. Measured output impedance of voltage-mode output driver

TABLE I. PERFORMANCE SUMMARY

Low Power Transmitter	
Technology	90nm CMOS
Supply Voltage	1.2 V
Data-rate	Max. 5-Gb/s
Power Consumption	8.5mW @ 5-Gb/s
Power Efficiency	1.72 mW/Gb/s
Area	60um X 70 um (Excluding capacitor)
Jitter	17.73psp2p (0.088UI)

V. CONCLUSION

A 5-Gb/s transmitter with voltage mode output driver is presented in this paper. This transmitter includes PRBS generator, 32:1 serializer and output impedance calibration circuit. It is fabricated in 90nm CMOS technology based on voltage-mode logic. It consumes 8.5mW of power at 5-Gb/s of data-rate and occupies 60 μm X 70 μm of area. The transmitter generates 5-Gb/s data with 17.73ps of jitter. The operation of output impedance calibration circuit has been verified by measuring the reflection and the output impedance of the output driver.

ACKNOWLEDGMENT

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